DESIGN AND CONSTRUCTION OF A DIGITAL ELECTRONIC CLOCK

BY

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93/3693

A PROJECT REPORT SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE DEPARTMENT OF ELECTRICAL/COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGERIA

MARCH, 2000

DECLARATION

I hereby declare that this project report design and construction is the result of my own handiwork. It was conducted under the supervision of ENGR. Dajuma Isa in the department of Electrical and computer Engineering of Federal University of Technology, Minna, Niger State, Nigerian.



06/04/2000

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CERTIFICATION

This is to certify that this project titled "DESIGN AND CONSTRUCTION OF A DIGITAL ELECTRONIC CLOCK" was carried out by SALAMI RAFIU AYODELE under the supervision of Engr. ISSA DANJUMA and submitted to Electrical and Computer Engineering Department, Federal University of Technology, Minna, in partial fulfillment of the requirements for the award of Bachelor of Engineering (B. ENG) degree in Electrical and Computer

ENGR. ISSA DANJUMA — 06/04/2000

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EXTERNAL EXAMINER — Sign & Date

DEDICATION

This project is dedicated to my beloved parents Allhaji K. Salami and Mrs. A. Salami.

ACKNOWLEDGMENT

Praise be to Almighty Allah the Lord of the world who spares my soul up to this moment and make this project a successful one, my special thanks goes to my beloved parents Alhaji K. Salami and Mrs. A. Salami for their moral and financial support rendered on me.

My profound gratitude to my supervisor ENGR. ISSA Danjumah, particular my HOD Engr. (Dr) Y.A. Adediran for their contributions, toward the success of this project and first degree programme..

My special appreciation goes to my brother Mr J. K. Salami, Mrs Muibat Suleman, Ossen Azeses, Abibu Usman, Kamaru-deen Yusuf, Kehinde Ige, David Ariyo, Yusuf Wumi, Adebisi T. A., Osowale Ganiyat Yetunde, Ramat Belo and E.P.C. members for a word of advice and encouragement given to me when at school. May Almighty Allah be with each and every one of them.

Salami R. A.

ABSTRACT

A Digital Electronic clock is an Interconnection of Integrated circuits and logic gate which operates with a d.c voltage of 5V produced from the output of its power unit. It uses the 555 timer as the pulse/timer generator for the frequency/oscillatory source of the project circuit. The frequency generated was processed Via the frequency divider circuit; counter accumulators, J. K. Flip – flop and the decoder section of the system. The project also incorporated light emitting diodes at its output to obtain the time in hours, minutes and seconds simultaneously.

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CHAPTER ONE

INTRODUCTION

1.0 INTRODUCTION

Digital clock is a device that display the exact time of the day in a discrete form. It has been a long time when we have been under the ages of analogue materials, but this computer age has brought innovations into technological systems. Many aspect of life have experienced changes. The big cumbersome instruments had been replaced with combination of gates and transistors fabricated on a very small chip.

This innovation is now being brought to us to produce a digital wall clock. Unlike before, the common clock that have been around is the analogue clock in which some calculation had to be done before one can know, the exact time. It has been observed that the calculation might not always be precise and takes some period before the brain could comprehend what the time is.

The digital clock eradicate these problems, and display exactly and precisely at a glance the time. The following diagram shows the block diagram of the digital clock and gives the general ideas of those units in the digital clock.

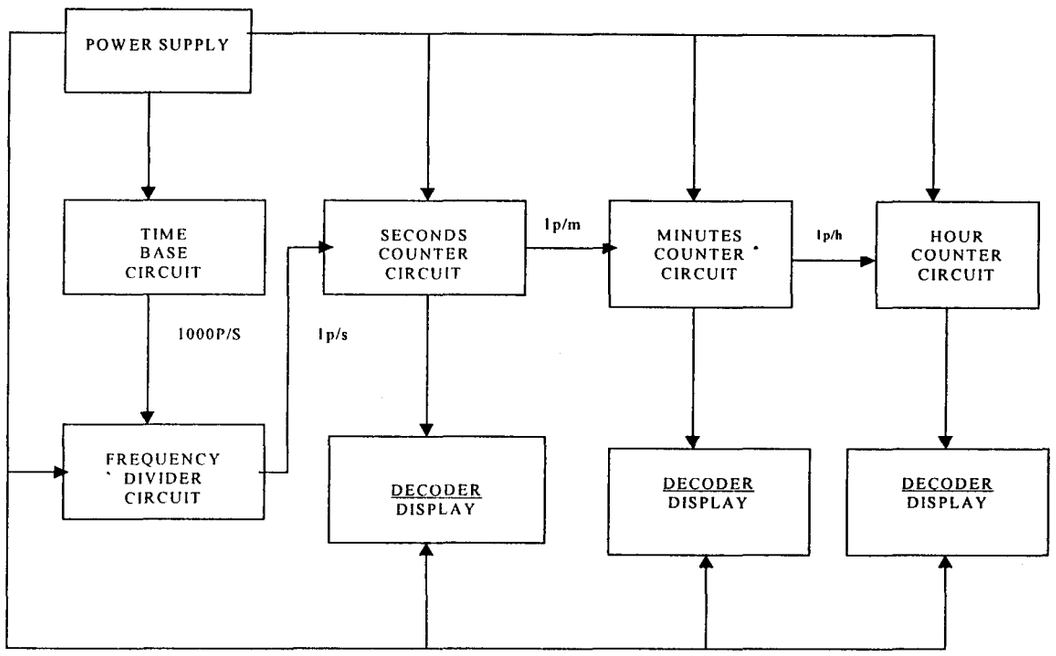


Fig. 1.0 A BLOK DIAGRAM OF DIGITAL ELECTRONIC CLOCK

Block diagram representation of a digital clock.

The power supply unit gives out d.c. voltage supply to all the other units. Digital system normally makes use of two possible states denoted a "HIGH" and "LOW", and "I" and "O", "OFF" and "ON", "TRUE" and 'FALSE' and have said to operate in a binary manner. In addition the semiconductors are based to operate only in low logic state. By this mode of operation, problem such as thermal run away maintaining a fixed quiescent point etc. common with analogue system are made void. Therefore a clock constructed based on these principles will be more accurate and efficient such a clock is said to be a DIGITAL DISPLAY CLOCK.

A digital display clock is a simple electronics device which makes use of logic circuits to count and display the hours, minutes and seconds the day. The clock cirkcuit consist of time base count accumulator, decoder and display circuits. Most digital display clock finds its application and use in all aspects of life due to the fact

that a high level of accuracy is guaranteed in what ever it is used are;

a. Electronics systems: It is used to determine the time taken to complete on operation such as formatting a disk.

b. Laboratories: In a number of Laboratories, digital clocks are used to find the time taken for a particular event to occur. Sometimes it is used to determine the time required to confirm the results of a particular experiment.

c. In sports: It is used to determine when the time schedule for a match.

d. In military Weapons: It is used in making timing bomb and missiles.

In order to understand the report more, the first chapter throws some light on the importance of the project and corporative of the project with primitive one, the second chapter deals with project design and theory, the third chapter also deals with construction, testing, trouble shooting, and costing while the last chapter deals with discussion and suggestion, maintenance and conclusion of the project.

1 .10 AIMS AND OBJECTIVES

The aims and objectives of this project are:

(i) To design and construct a" DIGITAL ELECTRONIC CLOCK "that will counts from 0 1 hour 12 hours and resets to 01 hour.

(ii) To design a clock of a high degree of accuracy less tedious in its use for measurement, consumption, high speed of operation and very cheap

1.2.0 METHODOLOGY

The basic timing for the clock was provided by a time base circuit. A source of an accurate, will defined pulse is required. This will ensure a continues train of pulses of a given frequency to be generated. In some application, the power line frequency of 50Hz or 60 Hz is used as input, crystal oscillator can be used and are, infact, the most reliable due to their stability and accuracy. However, for frequencies

between 8 KHz and 5 MHz, crystal oscillations and watches are usually very cost. The relatively high cost of a quartz crystal clock and complex frequency divider circuit would prevent their use in this project. IC 555 timer was therefore used for this project. The frequency divider section performs the division operation by dividing the output frequency of the 555 timer down to one pulse per second or one hertz. This is the basic count of the clock and the counters will be used for the purpose of frequency division. The decoder IC- SN7490 is also used.

The counter accumulator section has counters that keep the track of the number of seconds starting from 00 through 59 and then re-sets itself to the original position of 00. This will be received by the minutes counter its input. It then counts the number of minutes from 00 through 59 and re-sets to 00 again. The one pulse per hours and later re-sets to 01 hour. These counters used in the seconds and minutes to count the accumulators of each to 59 counts consist of a decade with a 0-1 counter which is a flip-flop. Thus, the decode counter is coupled to the 1's place of the display while the flip-flop is connected to the 10's place of the display.

1.2.1 LITERATURE REVIEW.

Time:- one fact of human consciousness, is awareness of "Time Human being feel the passage of time in their personal experiences and also observe it in their physical environment. It has being experienced, as a one-way flow at pace to show enough to be perceptible. People feel, think and act in consciousness of time flow.

However the familiar sub-division of day into hours, hours into minute, minute in seconds taken note of the fact that, 24 hours make a day. All these facts, originates from ancient origin but has come into general usage, since 1600 AD. Going down the memory lane, there have being different types of method used in the early generation in determine time of the day in which some of them are discussed below:

Early artificial clock: The first device for indicating "Time" of the day is "SHADOW CLOCK SUNDIALS", when people observed that tree and other objects cast shadows with more with sun. In 1500 B.C, the Egyptians constructed shadow clock. A vertical polelike object, or obslist, cast shadows on marked areas of the ground as the sun moved. The sundial ancient Egyptian solved the problem of telling time at night or on a cloudy day with the use of a water clock. The water clock operates by measuring water that trickles regularly from one container to another. In A.D 725 the chins had an elaborath water wheel clock, and later they built a 40 - foot (12-meter) high, pagoda-like observatory water clock like the sundial, the water clock. Saxons in Europe also used water clock like the sundial, the water clock had its disadvantages, it would freeze in colder climates and could not easily be used on moving objects, such as ships.

Construction of mechanical clock; such as our modern ones, begain in the 14th century, although there were some primitive versions as early as 200 B.C. The first mechanical clock were sound clocks. They had no feces or hands to look at but a bell that rang a number of times each day. More advanced, versions of bell clock were driven by a wight attached to a cord that was wrapped around a cylinder. The weight pulled down the cord to ring the bell, such clocks were hot very regular or efficient.

Pendulum clock: In 1656, Christian Huggen, a Duch scientist, built the first pendulum clock while in 1675, he built another clock power by a spring that regularly carried and uncoiled. Watches; in 1500 AB, Peter Helein made the first watches in Germany. They were elaborate, expensive toys of the rich that kept time quite poorly.

Modern Artificial clocks: The early clock were affected by gravity, location,

movement, wear, and temperature, and they needed castanet concentration. A pendulum clock would be of little use in a tossing ship at sea. The movements of such things as a shadow, sand, water, fire, sun, moon, and stars are not sufficient to measure the changes of atomic particles or the movement of bodies in outer space. For these purposes, scientists needed a steady and detailed standard that also was affected as little as possible by external influences. They eventually found the answer in atoms themselves. Scientists determined that the regular, predictable vibrations (also called wares, cycles, oscillations and resonations) of certain elements could function as a time standard.

The number of oscillations of the element cesium in one second is 9,192,631, 770. In 1967 this number of oscillations was adopted in the international system of unit (SI) as the definition of one second. Years are now officially measured in second, which at one time was based on astronomical observation, was given up, although it is still used for certain purposes.

The atomic clocks; is only inaccurate by one second in many thousands of years. This is quite good, but we have not seen the end of clocks. New ones are already being developed clock will change with new discoveries and needs. No one clock can meet all the needs of everyone. There is no perfect clock or absolute time.

Moreover, the increase in technological date back to 1937, which led to the development of the digital computer from the work of a small group of practical thinkers like Howard Aiken of Havard University on the design of a full Automatic calculating Machines in coka bration with International Business Machines corporation (IBM) and a paper presented by E. J. Mc dusky in 1973 at New York which he pointed that between the year 1952 and 1964, the transistor developed at Bell laboratories and its incorporation into digital computing technology. He further

stressed that the period 1964-1971 witnessed the development of 'Integrated circuit'. The development of integrated circuit culminating in the implementation of several logic functions on a single chip and introduction for LSI (Large Scale Integrated) chip in 1970, which witnessed the fourth generation of computing technology unshared into the modern day the "Digital electronic clock".

The "Digital Electronic Clock" eliminates all the problems encounter by early clocks and it has a high degree of accuracy, less power consumption and very cheap. This report assumes that the reader has basic knowledge of both digital and power. A basic knowledge of combinational and sequential circuit section of the project. Also little knowledge of power will help him or her understand the power section.

CHAPTER TWO

PROJECT DESIGN AND THEORY

2.0 INTRODUCTION/PRINCIPLE OF OPERATION

The most basic representation of an electronic clock is shown below in fig. 2.0

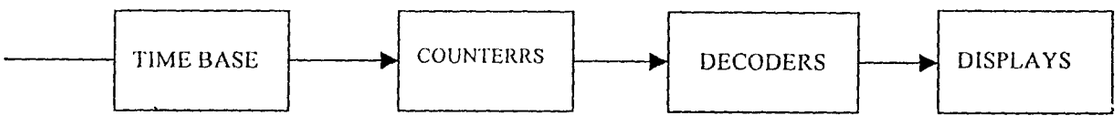


Fig. 2.0

2.1.0 SYSTEM OVERVIEW

The digital clock is a system consisting of logic gates, flip-flop and subsystems. The input of the system is the frequency source or the oscillator circuit. The processing takes place in the frequency divider, count accumulators and decoder sections. Storage takes place in the count accumulator. The control section is the time set control. The output is the digital time display. There is a power supply also to keep the system running. In fig. 2.1.0 is shown a block diagram of the digital clock. The various sections are discussed in the following sections.

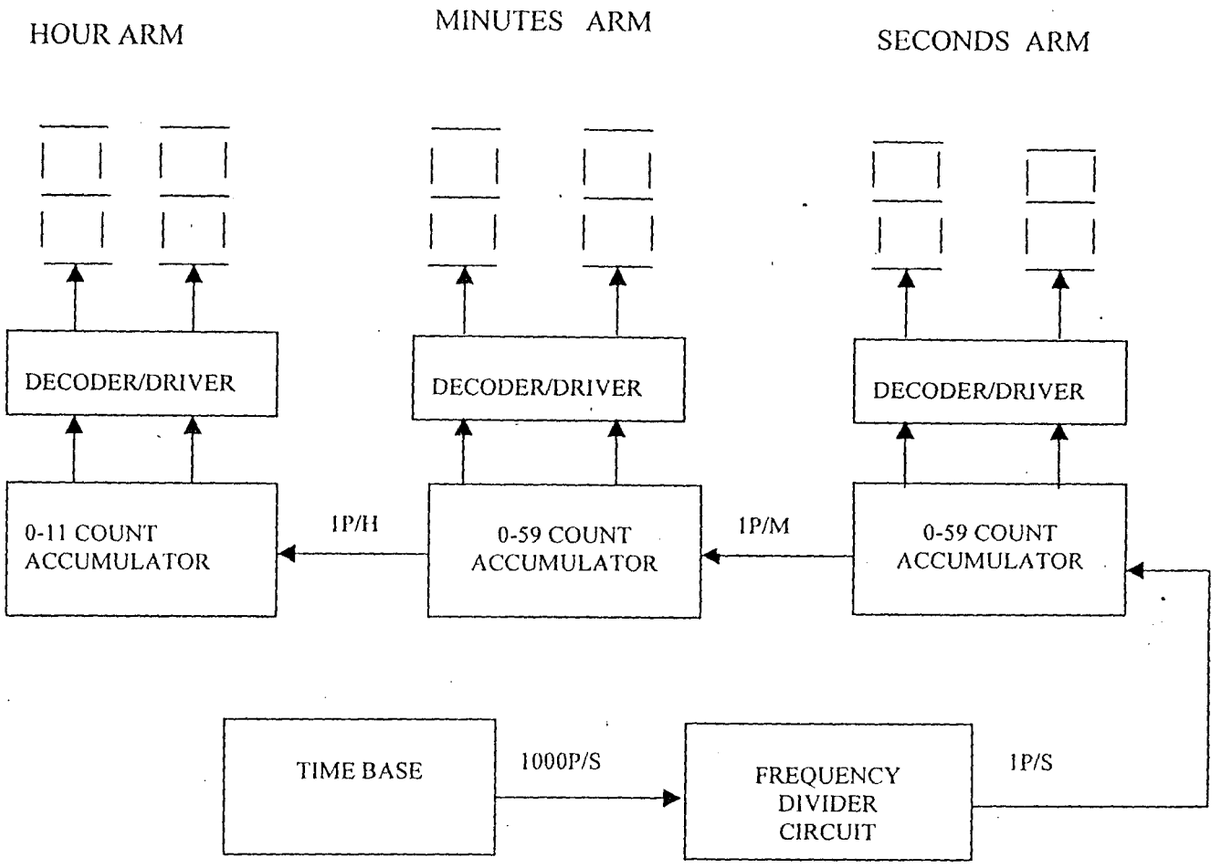
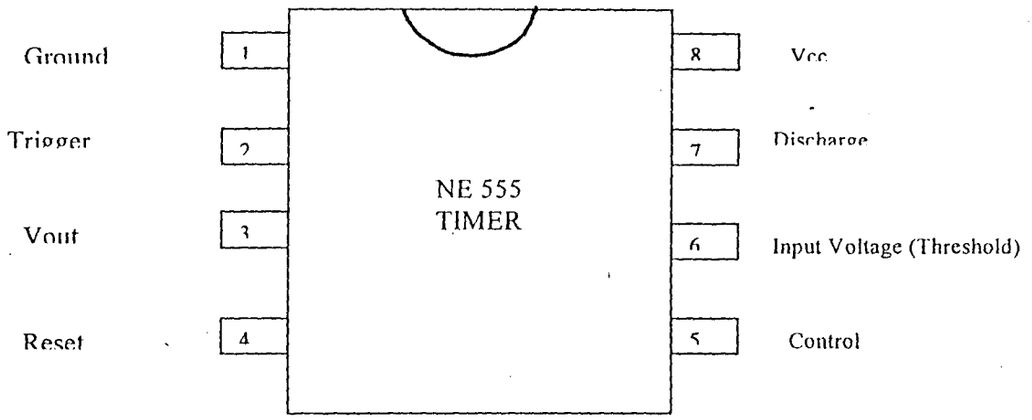


Fig. 2.1.0

2.1.1 TIME BASE SECTION

The time base circuit provides the basic timing for the clock. A source of accurate, well defined pulses is needed. In this case, the requirement is for a continues train of pulses of given frequency. In some applications, the power line frequence of 50Hz or 60 Hz is used as input. Crystal oscillators can be used and are infact the most reliable due to their stability and accuracy. Crystal sillators and watches are usually cut for frequency between 8kHz and 5MHz. The relatively high cost of a quartz crystal clock and complex frequency divider circuit it would require prevented its use in this project. IC timer was then used for this project. (555 timer IC).

The pins layout, internal circuitry, basic operation and the realization of the used frequency for this project are shown below.



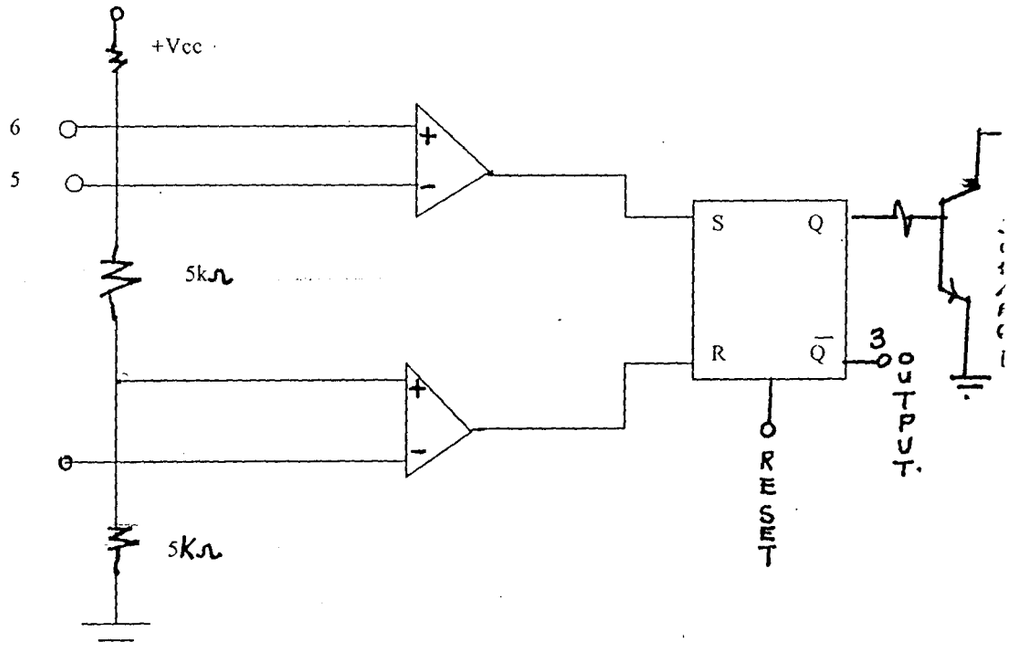


Fig. 2.1.1

Fig. 2.1.1

(i) 555 TIMER IC (ii) INTERNAL CIRCUITRY OF 555 TIMER IC

BASIC OPERATION OF 555 TIMER

As shown in Fig. 2.1.1 (iii), the inverting input of the cooperator is biased at a voltage of 10v i.e [10/(5+10] 15 = 10v through a potential divider. The non-inverting input voltage of the comperator is refered to as THRESHOLD VOLTAGE and the inverting input voltage as the CONTROL VOLTAGE. When the RS flip-flip set, i.e with a voltage equal to the supply voltage at output Q and output $\bar{Q}$ at Ov, the high voltage at Q drives the transistor into saturation and this causes capacitor C which was earlier charged through resistor R to discharge through the transistor to the ground since at saturation, the transistor causes a short circuit across the capacitor. This brings the threshold voltage to OV since this is now the voltage across the capacitor C as a result of the short circuit. The comperator output is now inverted since the control input voltage is more than the threshold voltage. If a signal is applied to input R, output $\bar{Q}$ is reset to OV and output Q to 15V. Since Q output is now OV, this causes the transistor to cut-off giving way to the capacitor increase exponentially as shown in fig. 2.1.1 (iv) above and this is the same as the threshold voltage. As the capacitor charges up towards the supply voltage, immediately the voltage is slightly greater than 10V, the output of the comperator switches state leaving S input high i.e 15V. This sets the flip-flop and output Q now becomes high (15V). This process is repeated so long as the supply voltage remains. The output waveform is as shown in fig. 2.1.1 (iv).

It is important to note that the rate at which the output voltage switches state depends on the rate of charging and discharging of capacitor C. Therefore, R and C in series determine the frequency of the output waveform. The threshold voltage is exponential in nature as it is the same voltage across the capacitor.

2.1.2 REALIZATION OF FREQUENCY USED WITH 555 TIMER CONNECTED AS ASTABLE MULTI VIBRATOR. (CLOCK FREQUENCY CALCULATION)

The frequency formula for the NE555 timer is given as

$$F = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

For a frequency of 1000Hz, a capacitive value of 0.1μF is chosen

$$1000 = \frac{1.44}{(R_1 + R_2)(0.1X10^{-6})}$$

$$(R_1 + 2R_2) = \frac{1.44}{1x10^3 x0.1x10^{-6}}$$

$$= 1.44 \times 10^4$$

R1+2R2 = 14400

A standard resistive value of 680Ω is chosen for R1

∴ 2R2 = 14400 - R1

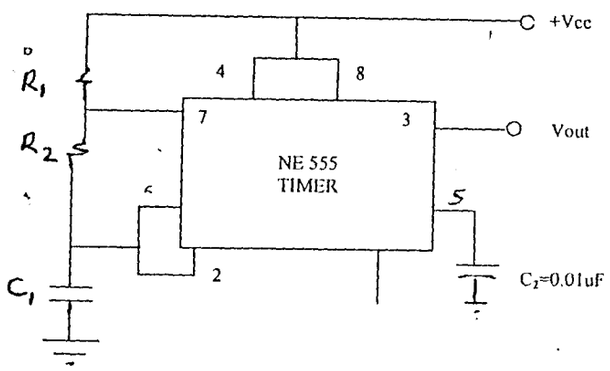
= 14400 - 680

= 13720

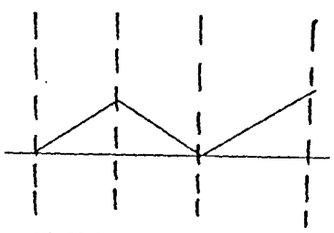
$$R2 = \frac{13720}{2}$$

= 6860Ω ≈ <u>6.8k Ω</u>

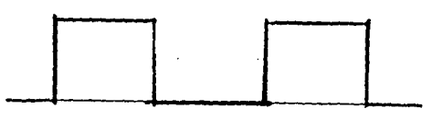
2.1.3 OPERATION OF 555 TIMER CONNECTED AS ASTABLE MULTIVIBRATOR



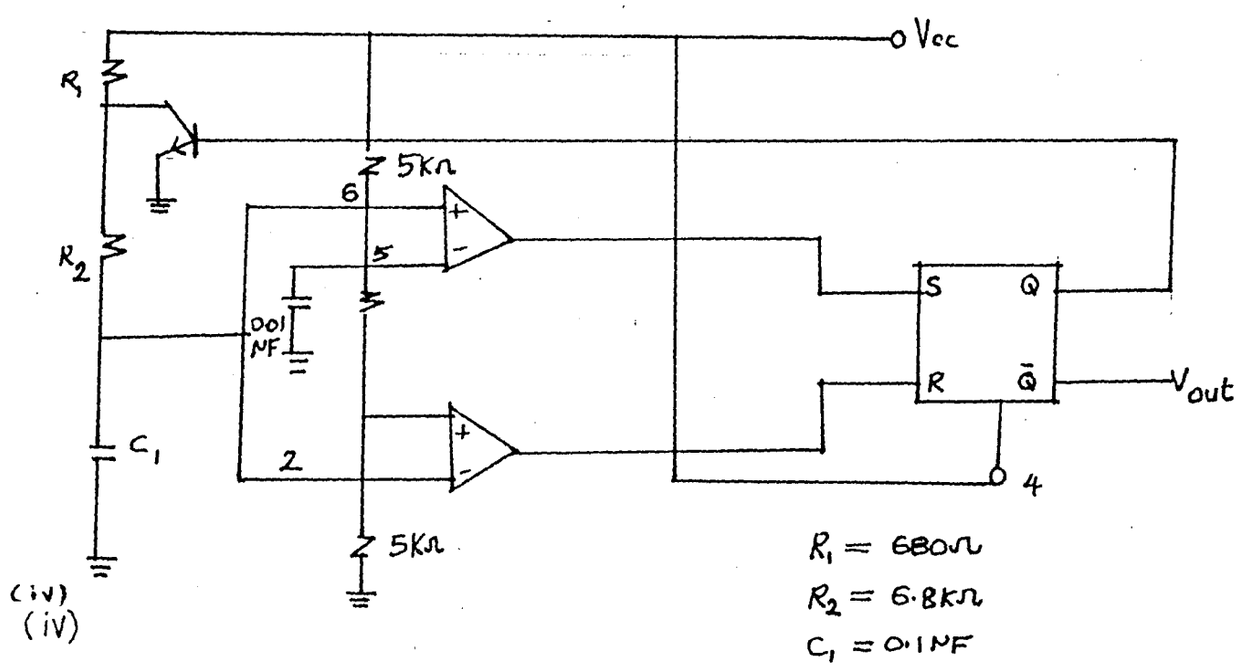
(i)



(ii) Voltage waveform of capacitor C1



(iii) Waveform of charging and discharging of capacitor C.



$R_1 = 680\Omega$

$R_2 = 6.8K\Omega$

$C_1 = 0.1NF$

$C_2 = 0.01NF$

fig 2.1.3

The figure shown above fig. 2.1.3 (iv) is a 555 timer connected as an astable multi vibrator (free running multi vibrator). The inverting input called the trigger (pin2) of lower comparator is connected to the threshold input (pin 6) and these two points are now connected across capacitor C. When the voltage at pin 2 is a little lower than one third of Vcc, the output of the lower comperator becomes high and this resets the flip - flop leaving Q at logic zero. This forces the discharge transistor to its cut-off region and as the collector of this transistor is connected across R2 and capacitor C at pin7, no current flows though the transistor and all the current from the supply flows through R1 and R2 to charge up capacitor C. As this capacitor charges up, the voltage across it rises first to ⅓ Vcc. When this voltage rises slightly above this value, the voltage at the inverting input of the lower compositor is greater than the voltage fixed at the non-inverting input and the output of the comparator goes low. This has no effect on Q output. The voltage across C continues to increase until it is slightly above ⅔ Vcc. Then, the threshold voltage is slightly greater than the voltage at pin 5. This turns the output of the flip-flop high and sets the flip-flop which implies that Q = Vcc. This voltage drives the discharge transistor into a saturation and then short circuits pin 7 to the ground as explained on its basic operation. The voltage at pin 7 is grounded meaning that capacitor will now discharge through R2 and via the discharge transistor to ground. The voltage across the capacitor begins to fall until it gets to ⅔ Vcc and slightly below this, the upper comparator output is switched low. But this does not affect the output Q. The voltage across C fails to ⅓ Vcc and slightly below it, the output of the lower comparator then switches high. The Rs latch is then reset and the process is repeated. The continues charging and discharging of capacitor C results in the rectangular waveformed at the output pin (3) as it is shown in fig.2.13b (iii) The wave form of the

voltage across capacitor C also decreases and increases exponentially as shown in the fig. 2.1.3. (ii). The capacitor changes up to ⅔ Vcc and discharges up to ⅓ Vcc. The by-pass capacitor (0.01μf) connected to pin 5 is just to provide noise filtering for the control voltage. If the reset terminal (pin4) is connected to the ground, it will not inactivate the whole circuit and hence it is always connected to the supply terminal as shown in the figure above.

However, having calculated the values of R1 ≈ 6.8KΩ with chosen values of a standard resistor R1 = 680Ω and a capacitive value of 0.1μF for a frequency of 1000 Hz, this NE 555 timer is able to function as determined. Besides, in order to generate one pulse/second (1Hz) the output of this astable multi vibrator is connected to three decade counters in cascade for frequency division.

2.2.0 FLIP-FLOPS

Sequential logic circuit are derived from various inter connection of FLIP-FLOPS. They are circuit with the ability to retain present state at the output when the input states are charged. Such circuits are COUNTERS, REGISTERS, PULSE GENERATOR etc.

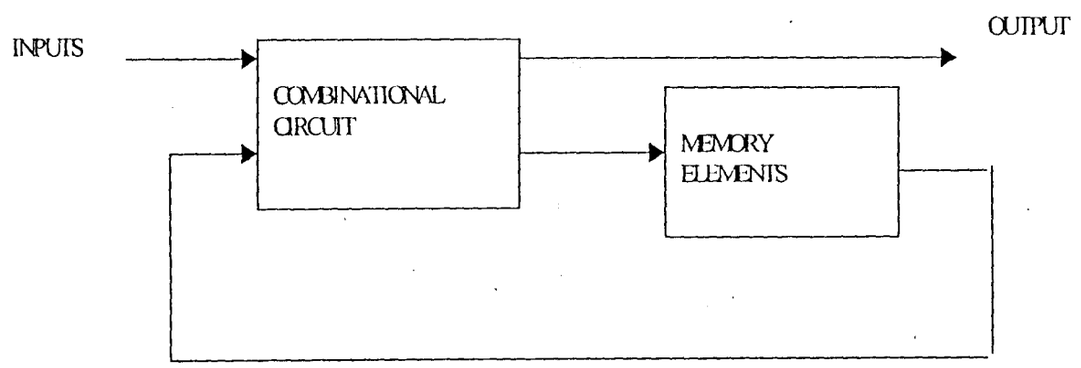


Fig. 2.2.0

The are two types of sequential circuit and they are:

(i) **ASYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT SYSTEM:** Is a system which depends upon the other in which its input signals charge and can be affected at any instance of time.

(ii) **SYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT SYSTEM:** Is a system which has a behaviour that can be defined from the knowledge of its signals at discrete instants of time.

The sequential logic circuits which consists of memory element are called FLIP-FLOPS. There are different kinds of flip-flops such as J.K flip-flops, D-flip-flops etc., but we will limit ourselves to the types used in this project (J-K flip-flops).

Flip-flops have the following basic characteristics.

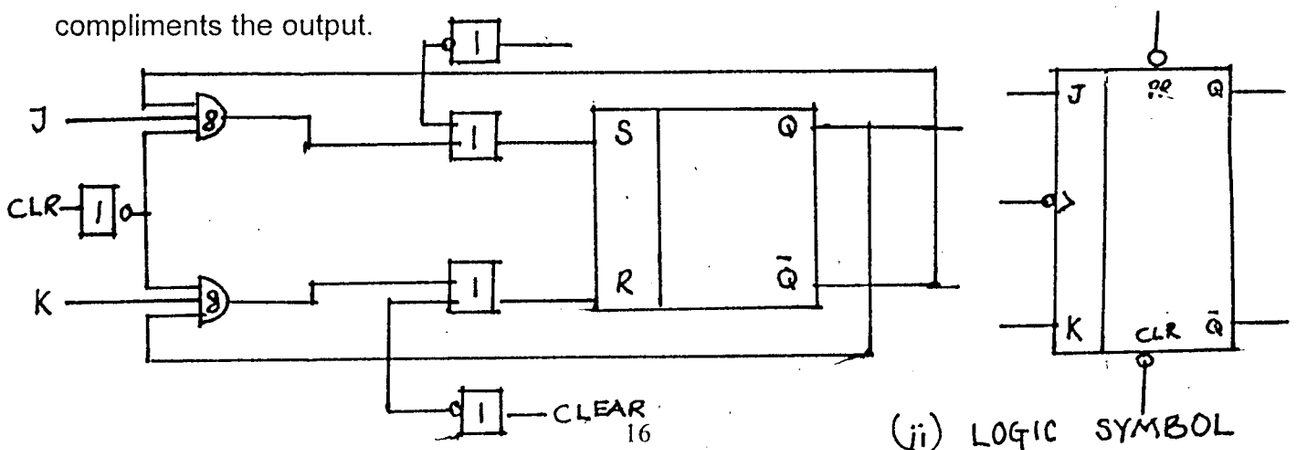
(i) They have the ability to store one bit of binary information.

(ii) They have two outputs which are complementary i.e one for the normal value and the other for the complementary value of the bit stored in it.

A flip-flop circuit can maintain a binary states indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch state.

2.2.1 J-K FLIP-FLOPS

J-K flip-flops is one of the memory elements used for counters. This is a refinement of the R-S flip-flops in that the indeterminate state of the R-S flip-flop is defined in the J-K flip-flop. When this occurs, i.e J = 1 and K = 1, the circuit toggles and compliments the output.



(i) LOGIC DIAGRAM

(ii) LOGIC SYMBOL

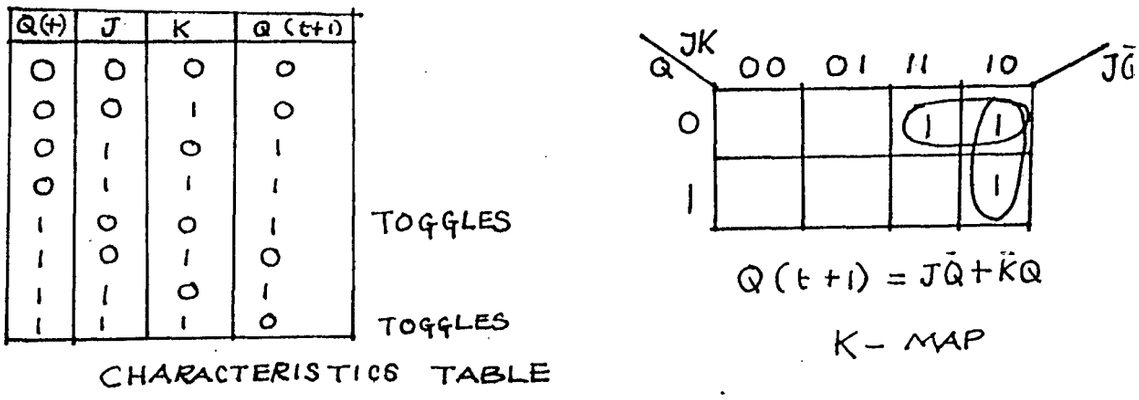


Figure 2.2.1 Negative Edge Triggered J-K Flip-Flop with inverted preset and clear inputs.

As shown fig. 2.2.1 (i), the PRESET and CLEAR input are said to be asynchronous input. This implies that through these inputs, the J-K flip-flop can be activated independent of the clock pulse. Therefore, the J and K inputs are said to be synchronous inputs since they can be used to activate the flip-flops only then when the clock pulse occurs. When power is first applied, the flip-flop comes up in random states and also to get some computer started, on operator has to push a reset button. This sends a clear as reset signal to all flip-flops. It also necessary in some digital systems to preset (synonymous with set) certain flip-flops. The effect of the clear signal and preset signal can be further observed in the following table below (functional table).

Inputs				Outputs		Inputs				Outputs	
Clear	Clock	J	K	Q	Q	Preset	Clock	J	K	Q	Q
0	x	x	x	0	1	0	x	x	x	1	0
1	1	0	0	no change		1	1	0	0	no change	
1	1	0	1	0	1	1	1	0	1	0	
1	1	1	0	1	0	1	1	1	0	1	
1	1	1	1	toggle		1	1	1	1	toggle	

The table 2.2.1 (i) describes the behaviour of various inputs of the J-K flip-flop. (Functional table)

As it can be seen from table 2.2.1(i) the two asynchronous inputs are considered with other inputs separately because they (asynchronous inputs) are not operated simultaneously. The two asynchronous inputs affect the flip-flops independent of the clock and the two synchronous inputs i.e J and K. for example, when CLR =O, irrespective of what CLK, J or K inputs, the output is maintained at Q = O. Also when PR = O, Q = 1 irrespective of CLK, J and K inputs.

STATE OR TRANSITION TABLE: This is also one of the important table of a J - K flip - flops. The time sequence of inputs, outputs and flip-flop states are being enumerated. It consist of three section Viz, the present state, the next state and the output. The state table for the J-K flip-flop is shown in the table below.

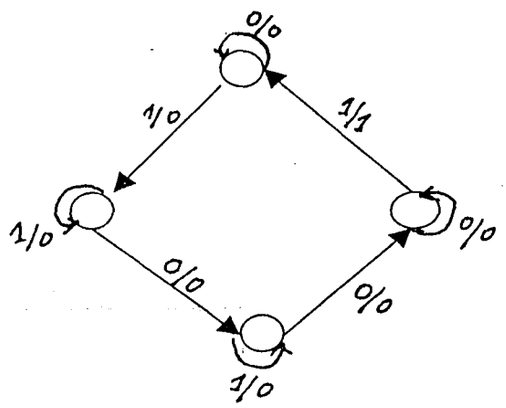
Present State of the Output	Next state of the output	Inputs	
Q	Q (t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Table 2.2.1 (ii) THE EXCITATION TABLE OF A J-K FLIP-FLOP

From the table shown above, it can be seen that when J = 0, K can either be 0 or 1 and yet, it will not affect the state of the output i.e Q = 0, Q (t+1) = 0 meaning that the J input determines the output. This is also the case when J = 1. When K = 1, J can either be 1 or O. This will make no difference at the output since K now determines the state of the output. Hence, x represents the "DON'T CARE" condition i.e it can be either 0 or 1 implies that it really makes no difference.

The present state on the table represents the state before the occurrence of the clock pulse, while the next state is the state of the output of the flip-flop after the occurrence of the clock pulse.

STATE DIAGRAM: This is a graphical representation of information on the state table. It also describing the behaviour of the logic states of a flip-flop. In this diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles. An example of this is shown in fig. 2.2.1 (ii) representing the state diagram of a particular sequential logic circuit.



STATE 2.2.1 A STATE DIAGRAM OF A LOGIC COUNTER

The binary number inside each circle identifies the state it represents. The direct lines are labeled with two binary numbers separated by a slash (/). The input value causes the state transition is labeled first, the number after the symbol/gives the value of the output during the present state eg. The direct line from the state 00 to 01 is labeled 1/0 meaning that the sequential circuit is in a present state 00 when x = 0 and Y = 0 and that on the termination of the next pulse, the circuit goes to the next state, 01, and x and Y are inputs. A direct line connecting with itself indicates that no change of state occurs.

Besides, the state diagram provides the same information as the state table. There is no difference between a state table and a state diagram except in the manner of representation. The state diagram gives a pictorial views of a state transition and in a form suitable for human interpretation of the circuit operation. It is often being used as the initial design specification of a sequential circuit.

STATE EQUATION: This is also known as an application equation. It is also used to describe the behaviour of the logic state of a flip-flop. It is an algebraic expression that specifies the condition for a flip-flop state transition. The equation is obtained from the k-map. A state equation is similar in form to a flip-flop characteristics equation, accept that it specifies the next state condition in terms of external input variable and other flip-flop values. The left side of the state equation denotes the next state of a flip-flop, and the right side, a Boolean function that specifies the present state condition that makes the next state. An example of a state equation is

$$A(t+1) = (AB + AB + AB)\,X + ABX$$

The equation is obtained from say flip-flop A. A (t+1) represents the next state of A when the condition representing the present states of the right hand state

of the equation is met after the occurrence of the clock pulse. The time t in A (t+1) shows that it is applicable only in clock sequential circuits.

2.2.2 COUNTERS

Counter circuit is a sequential circuit which goes through a prescribed sequence of states when input pulses are applied. These input pulses are called "COUNT PULSES".

Counters generally obey the rule 2^n when n represents the number of flip-flops needed to implement a counter that will count through 2^n n number of states in binary. The largest binary number counted by n cascaded flip-flops has a decimal equivalent of 2^{n-1}. It should be noted that counters can be designed to skip some states depending on what is in the mind of the designer. Such counters are called "TRUNCATED COUNTERS".

There are two major categories of counters namely, synchronous and Asynchronous counters.

SYNCHRONOUS COUNTERS: This is the type of the counter when the flip-flops are connected in such a way that they are triggered almost at the same time by the same clock pulse (parallel connection).

ASYNCHRONOUS COUNTERS: These are obtained from serial connection of flip-flops. The disadvantage of this connection is the speed which is low since the output of one flip-flop is used to trigger the other and so on, which results in a cumulative setting time.

With all the necessary information on J - K flip-flops in the previous section, therefore we proceed to design counter (mod-10 counter) Decade counter used for this project.

2.2.3 DETAIL ANALYSIS OF DECADE COUNTER (MOD-10 COUNTERS)

The mod-10 counter is designed using J-K flip-flops. Mod number = 2^n. where n = number of flip-flops in the arrangement.

Hence,

2^n = number of state the flip-flop will pass through or undergo before it resets.

To design a decade counter n must be equal to 4.

2^4 = 16 states

Therefore, it implies that there are four basic flip-flops in this arrangement.

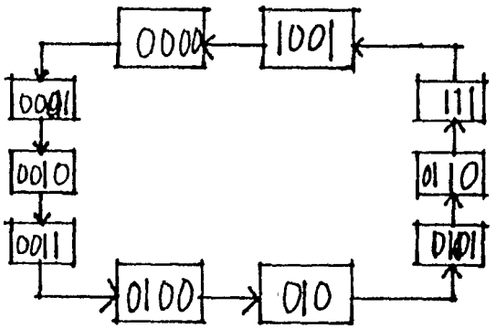
The most economical way of designing this counter is by a "HIGHER MOD TECHNIQUE". This method is adopted because it does not require additional gates and therefore reduce cost of production.

HIGHER MOD TECHNIQUE: This is a method of deriving a counter of mod-m by the combination of counters of mod equal to factors of m e.g mod - 10 counter required, a combination of a mod-2 and a mod-5 (i.e 2x5).

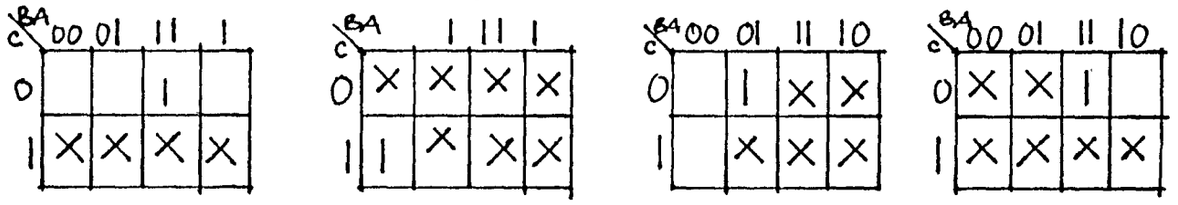
MOD - 5 COUNTER DESIGN

PRESENT STATE	C	B	A	NEXT STATE	C	B	A	J2	K2	J1	K1	J0	K0
0	0	0	0	1	0	0	1	0	x	0	x	1	x
1	0	0	1	2	0	1	0	0	x	1	x	x	1
2	0	1	0	3	0	1	1	0	x	x	0	1	x
3	0	1	1	4	1	0	0	1	x	x	1	x	1
4	1	0	0	0	0	0	0	x	x	0	x	0	x
5	1	0	1	?	x	x	x	x	x	x	x	x	x
6	1	1	0	?	x	x	x	x	x	x	x	x	x
7	1	1	1	?	x	x	x	x	x	x	x	x	x

(i) State table 2.2.3

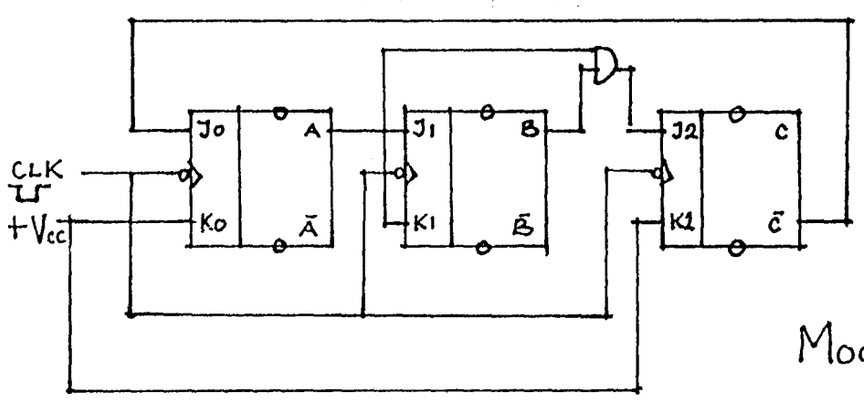


State diagrams (Mod-10 counter)

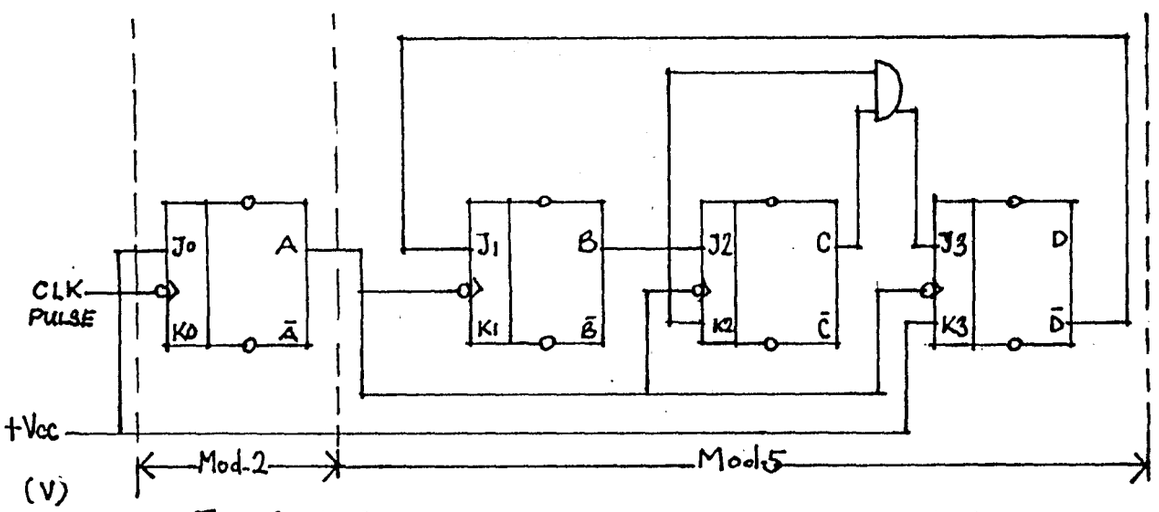


(iii)

K-maps to implement the state table



(iv) Mod-5 counter



(v)

Fig 2.2.3 Mod-10 Counter

fig 2.2.3 (i) shows the state of mod-5 counter in which it changes state from 0-3 and reset to 0 on 4.

Fig 2.2.3 (ii) is the k- map used to reduce the state table.

Fig. 2.2.3 (iv) is the implementation of the K -map to design mod 5 counter.

Fig. 2.2.3 (v) is the final design of mod - 10 counter which is the combination of mod - 2 and mod - 5 counter.

Fig. 2.2.3 (ii) is the state diagram of mod- 10 counter.

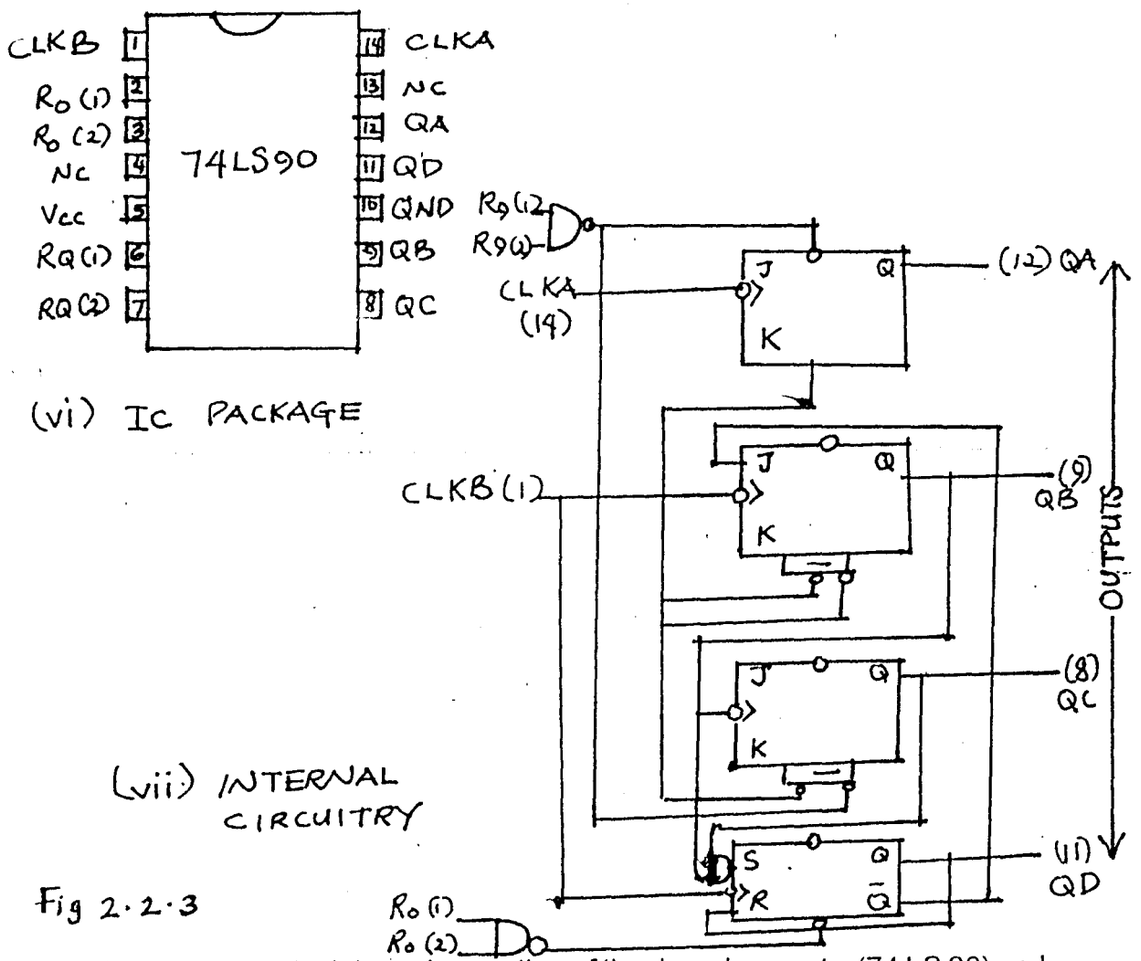


Fig 2.2.3

Having understand the principle and operation of the decade counter(74 LS 90) and its configuration is understood fully therefore this counter is used for many purposes in this project.

2.3 FREQUENCY DIVIDER SECTION

The purpose of the frequency divider section is to divide the output frequency of the 555 timer (1000Hz) down to one pulse per seconds or 1Hz which is the basic count of the clock. The counters used for this purpose decade counters (74 LS 90)

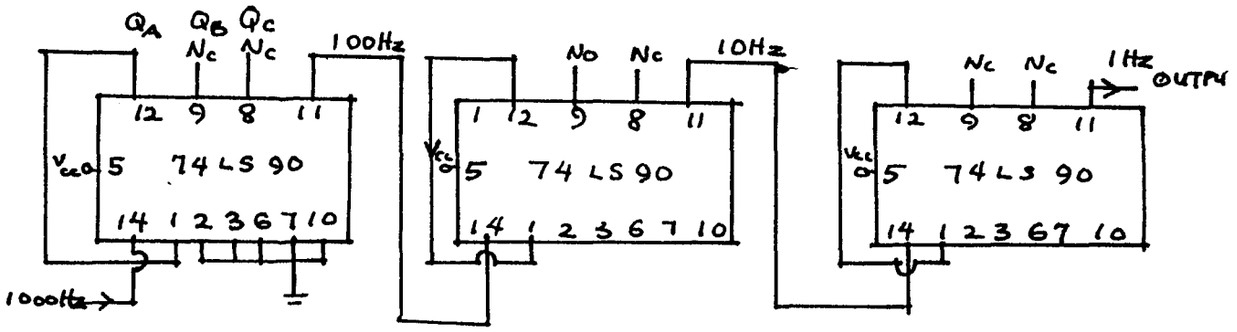


Fig. 2.3 Frequency divider circuit

2.4 THE COUNT ACCUMULATOR SECTION

This consists of counters (74 LS 90) that keep track of the number of seconds from 00 through 59 and then resets to 00 with an output of one pulse per minute. The minutes counter receives the one pulse per minute output pulse from the seconds counter as its own input and then counts the number of minutes from 00 to 59 and then resets to 00. The output of this circuit is one pulse per hours. The one pulse per hours counter counts from 01 hours to 12 hours and then resets to 01 hours.

The counters used in the seconds and minutes count accumulators (0-59 counter) consists of a decade counter. Cascaded with a 0-5 counter (i.e module - 6 counter). The decade counters are coupled with 1's place of the display. The modulo - 6 counter is coupled with the 10's place of the displace. In like manner,

the hours count accumulator is a decade counter cascaded with a 0-1 counter which is a flip in this case. The decade counter is coupled to the 1's place of the display while the flip-flop is connected to the 10's place of the display.

2.4.1 SECONDS AND MINUTES COUNTER

The seconds counter is two 7490 IC counters. The first is wired for a decade count to provide the units seconds. These two counters effectively carry out a count of 0-59 and then resets. The output is one pulse per minute which is applied to the minute counter. The minutes counters are exactly the same with an output of one pulse per hour. The seconds and minutes counter, circuit is shown below in fig. 2.4.1.

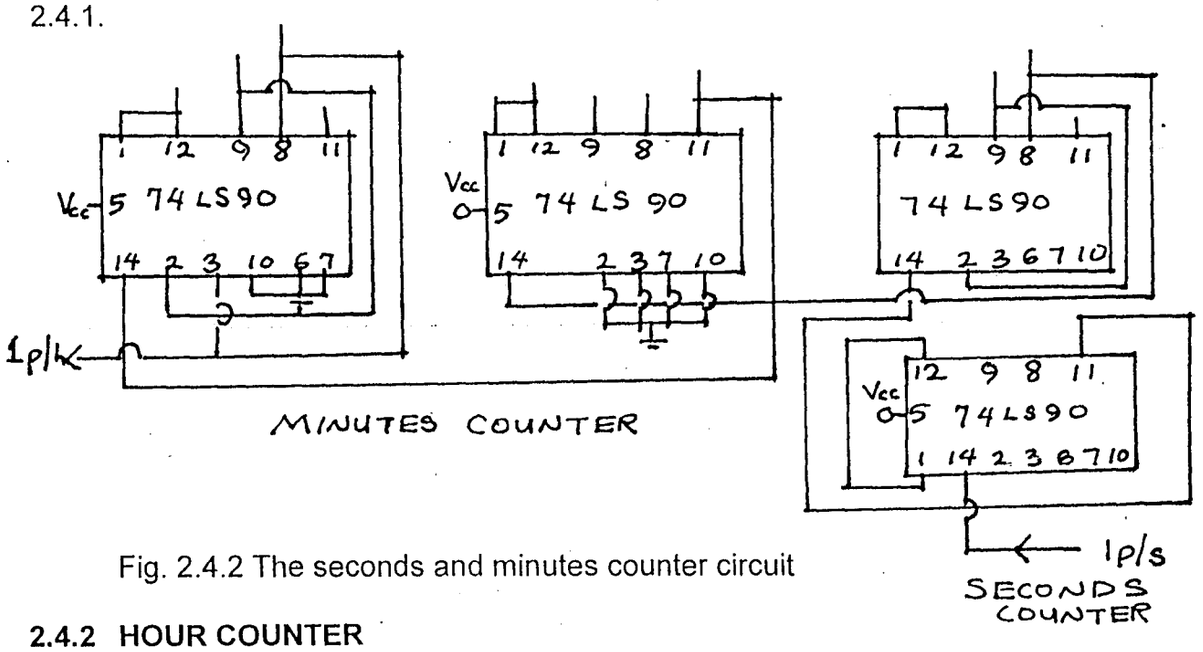


Fig. 2.4.2 The seconds and minutes counter circuit

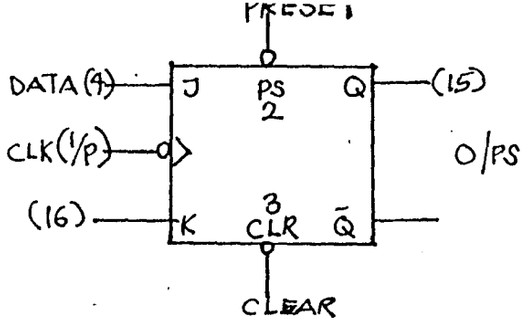
2.4.2 HOUR COUNTER

The hours counter is slightly different. It has the 7490 IC as a decade counter in the units position. The output of this counter is inverted by an IC inversion, to provide the unit hours reset so that at 12:59:59, the clock resets to 01:00:00. In the tens of hours position however, instead of the 7490 IC previously used, a J K flip - flop (7476) is used. Since it is a 12 hour clock, this digit is only a 0 and 1. These two output states can easily be obtained using the 7476 IC which

is discussed below.

7476 IC

(i) Logic Symbol



MODE OF OPERATION	INPUTS					O/PS	
	ASYNCHRONOUS		SYNCHRONOUS				
	PS	CLR	CLK	J	K	Q	Q
Asynchronous set	0	1	x	x	X	1	0
Asynchrònous reset	1	0	x	x	x	0	1
Prohibited	0	0	x	x	x	1	1
Hold	1	1	⎍	0	0	No change	
Reset	1	1	⎍	0	1	0	1
Set	1	1	⎍	1	0	1	0
Toggle	1	1	⎍	1	1	Opposite set	

(ii) Truth table X - irrelevant +ve clk pulse

Fig. 2.4.2

The logic symbol is in fig. 2.4.2 (i) above, showing the two asynchronous input (preset and clear) and the synchronous input J and K data clock inputs and the customary Q and Q outputs. Also the detailed truth table is shown in fig. 2.4.2 (ii). The asynchronous inputs are activated in the first three lines of the truth table overiding the synchronous inputs. When both asynchronous inputs (PS and CLR) are disabled with a 1, the synchronous inputs can be activated. W a 0 is applied to the clear input, the flip-flop resets. This feature is used in resetting the hour counter.

2.4.3 THE HOURS COUNTER

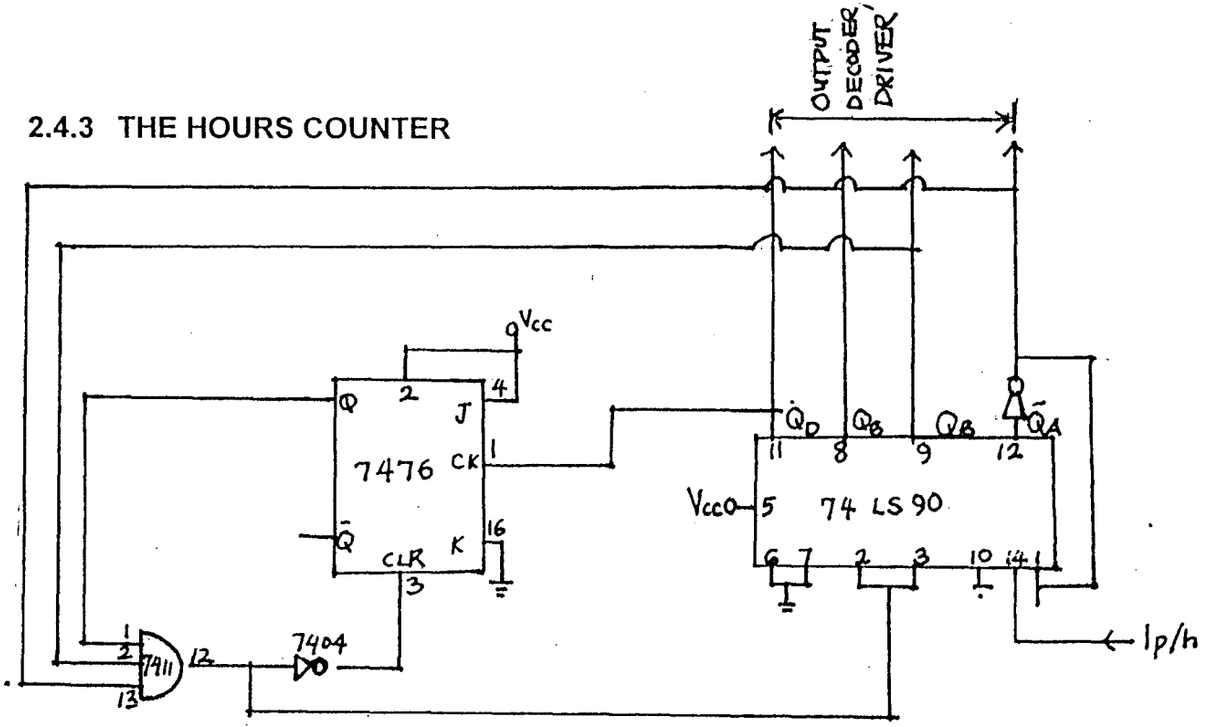


Fig. 2.4.3 The logic circuit of the Hour counter.

RESETTING THE HOURS COUNTER

When the digital clock reads 12:59:59, the minutes and seconds will automatically reset to zero. The hour however must rest to 01 hours. Three Ics are used to achieve this shown in the diagram of fig. 2.4.3 above. The Ics are 7411, 7404d and 7476. The 7411 and 7404 provides decode logic to reset the clock. The exact operation is as follows.

When the clock reads 12:59:59, the output of the 7476 is a logic 1. This output and the output QB and $\bar{Q}$ A of the 7490 which are also logic 1 are passed to the 7411 AND gate to give a logic 1 output. This output is passed through the 7404 inverter to give a low output. This low output of the 7404 is connected to the clear input of the 7476. The clear input is active low and therefore the flip-flop resets to give a 0 output at the Q output of the 7476. The reset input of the 7490 are also connected to the output of the 7411 AND gate to give a logic 1 output this output is passed through 7404 inverter to give a low output the low output 7404 is

connected to the clear input of the 7476 the clear input is active and therefore the flip-flop reset to give a 0 output at the Q output of the 7476.. This reset input of the 7490 are also connected to the output of the 7411 which is at logic 1 this reset the 7490 counters back to 00. However, there is an active low inverter at the QA output which is activated and therefore there is a count of 1 on 7490. The hours counter therefore resets from 12hous to 01 hours.

2.5 THE DECODER SECTION

In digital electronics, all operations are carried out in binary from. The information at the output of the counter are in binary form therefore, it is necessary to find a way of converting this information in binary to a form suitable for a man to interpret and a circuit required for this purpose is known as a "DECODER".

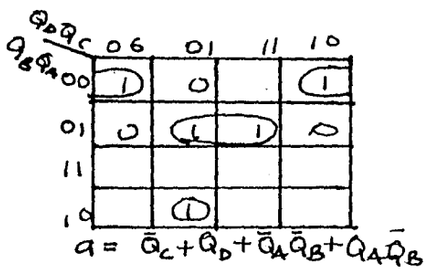
A DECODER: A decoder is a combinational logic circuit that converts binary information from n-input lines to a maximum of 2^n unique output lines. If the n-bit decoder information has unused combinations as is the case with the special decoder used for this project, the decoder output will have less than 2^n outputs. This decoders are refered to as n – to - m line decoders where m is less than or equal to 2^n.

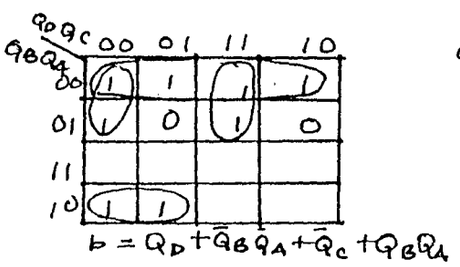
A seven segment decoder is used for this project. It is a 4 - to - 7 lines decoder. It has four inputs and seven outputs. These outputs are used to drive a seven segment display.

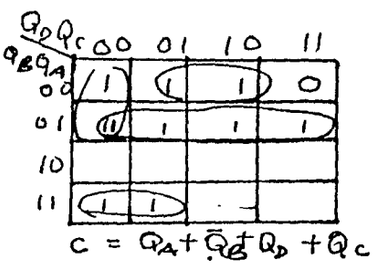
2.5.1 DESIGN OF A SEVEN SEGMENT DECODER

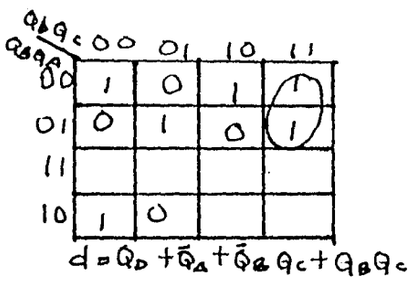
DENARY DIGIT	INPUTS				SEGMENT (ON=1)						
	Q0	Qc	QB	QA	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	1	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1 0
6	0	1	1	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

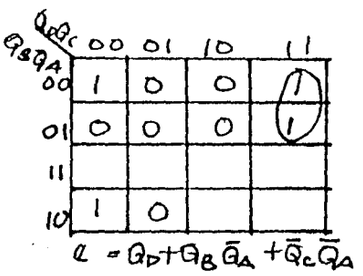
Table 2.5.1 Truth table for the seven segment Decoder

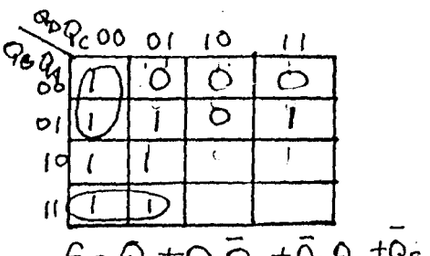












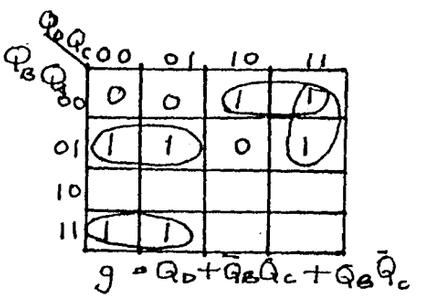


Fig · 2.5.1

K - maps implementation of seven segments outputs.

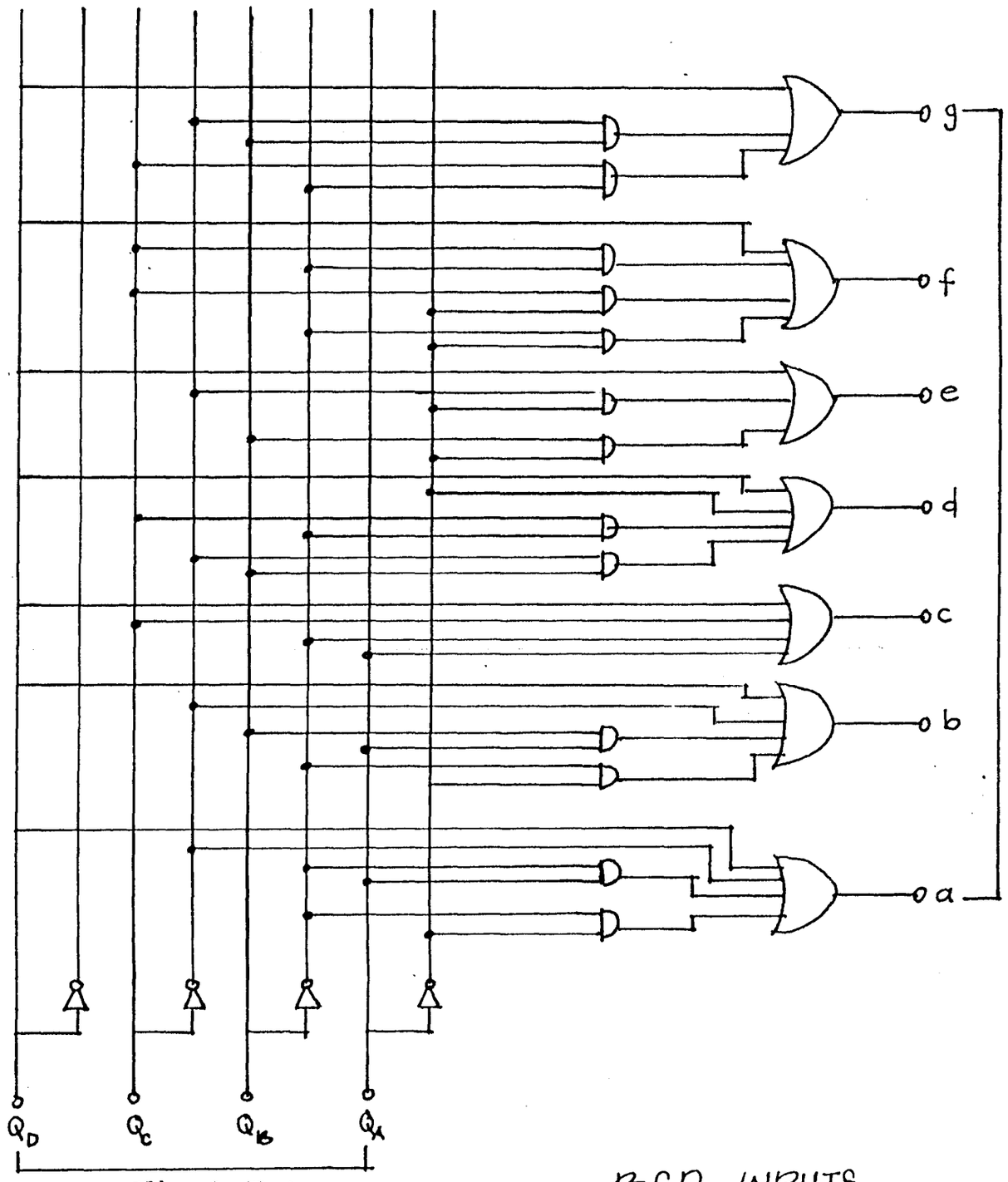


Fig 2·5·1

(iii) IMPLEMENTATION OF THE K-MAP

COMBINATIONAL LOGIC CIRCUIT OF THE SEVEN SEGMENTS DECODER/DRIVER

2.5.2 CHOICE OF DECODER/DRIVER IC

As it can be seen in fig. 2.5.1, if one is able to implement this circuit using single scale integrated circuit, the number of components required is enormous. For example, this project required six seven segment decoders. If six of such circuit are to be implemented at the end of the day, the cost of production would be very high. Therefore, it would be wiser to go for circuit that is less costly and most effective and such circuit comes in a medium scale integrated circuit e.g 74LS47 decoder. It is a decoder/driver used to drive a seven segment display in this project.

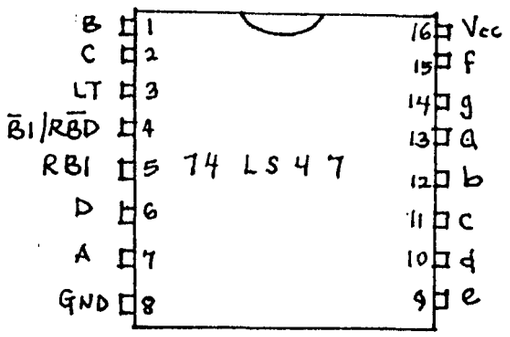


Fig.2.5.2 A seven segment Decoder (74LS 47)IC.

The figure shown above 2.5.2 is a 4 - to - 7 line decoder. It has four data inputs, A., B, C and D and seven active low outputs a, b, c, d, e, f, and g. These outputs. If a binary seven, A = 1, B = 1, C= I and D = O are present at the data inputs the output a , b, c and g would be at an active low since the display used in this project is a common-anode, only the segments to which these outputs are connected (a,b,c and g) are turned ON, therefore a decimal seven is then displayed.

2.6 DIGITAL DISPLAY OR READOUT

The display employed in this project is the seven segment display which is widely used as a readout for modern digital equipment.

There are three types of seven-segment display. These are

(i) Light emitting diode (LED)

(ii) Liquid Crystal display (LCD) and

(iii) Gas discharge display (GDD).

However, the seven-segment indicators in this project are basically Red light emitting diodes (LED) constructed on a veroboard in a geometrical pattern, dipicting the shape of decimal numbers from 0-9 depending on which segment is selectively illuminated as shown in the figure 2.6 below. The LED was chosen because it was cheap and available in the market.

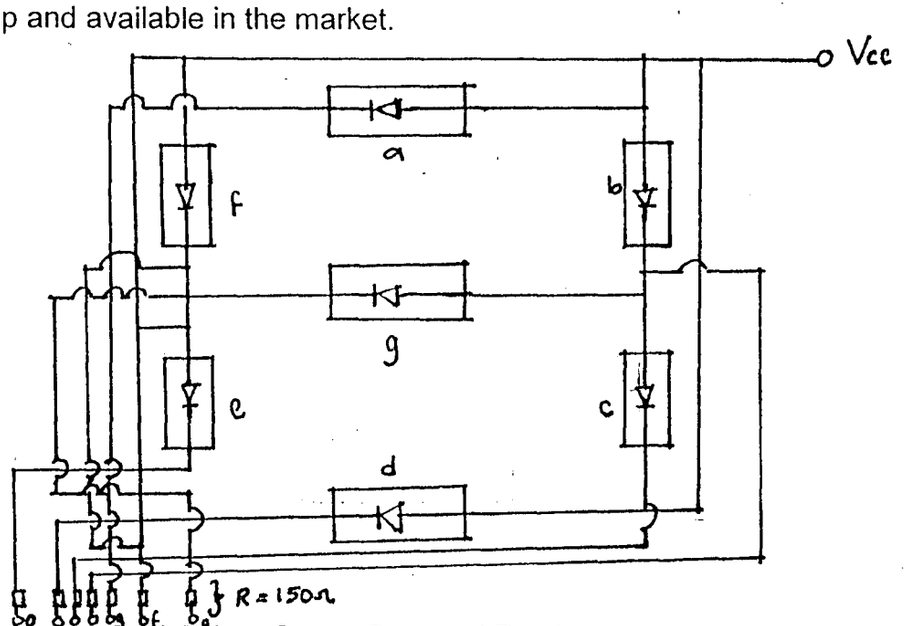


fig. 2.6 Red Colour Seven Segment Display.

The LED seven -segment is a common-anode display in which all anodes are connected together while the cathodes are independent as it is shown in fig 2:6.

To operate the LED display, all anode terminals must be supplied with positive voltage. The current flowing through each diode must be limited to about 20mA which is the maximum amount of current that must pass through each for safety. Therefore, in order to prevent current passing through these diodes, a current limiting resistor must be introduced in series with each diode at their respective cathode.

2.6.1 CALCULATING THE VALUE OF THE CURRENT LIMITING RESISTOR FOR THE SEVEN SEGMENT, LED DISPLAY

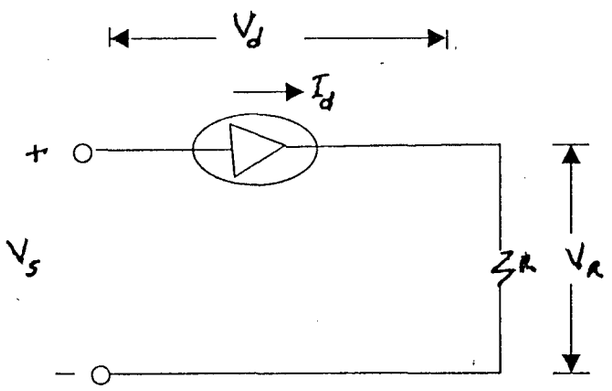


Fig.2.6.1(ii)

As it is shown in the circuit above (fig 3.6.1(ii)). The range of the voltage drop in the diode is $1.0 \leq Vd \leq 3.0$

Where Vs (supply voltage) = 5V

Id (diode current) = 20mA.

(a) For Vd (min) of 1.0V

from,

$$V_s = V_d + V_R$$

$$V_R = V_s - V_d$$

$$= (5-1)V$$

$$= \underline{4V}$$

Thus,

$$V_R = I_d R_1$$

$$R_1 = \frac{V_R}{I_d} = \frac{4}{20 \times 10^{-3}}$$

$$= \underline{200\Omega}$$

(b) For V_d (max) of 3V

from,

$V_s = V_d + V_R$

$V_R = V_s - V_d$

$= (5-3)\ V$

$= \underline{2V}$

Thus,

$V_R = Id\ R_2$

$$R_2 = \frac{V_R}{I_d} = \frac{2}{20x10^{-3}}$$

$= \underline{100\Omega}$

Therefore, the range of the value of limiting resistor is

$R2 \leq R \leq R1$

$100\Omega \leq R \leq 200\Omega$

$\therefore$ $R = 150\Omega$ was chosen.

2.7.0 THE POWER SUPPLY UNIT

In order to remove the stress from the power supply unit, this project design requires a dual voltage supply of + 5v. This was done because the total current consume by the whole circuit is more than IA and therefore two 5V, IA (7805) regulator were connected in parallel so that the two of them now share the total current being drawn by the circuit together according to the Kirchoff's current law. The connection of the power supply is as shown in fig. 2.7.

The circuitry consists of a 220v/12v transformer whose outputs are fed into the diode rectifier to produce a dc voltage output. Some capacitors of specified capacitance values were used to remove ripples by way of fluttering. The two 7805

Ic voltage regulators were connected in parallel and used to produce constant dc voltage supply of +5v and +5v respectively which one of them is required to power display, decoder and accumulator sections while the second + 5v is used to power time base and frequency divider sections.

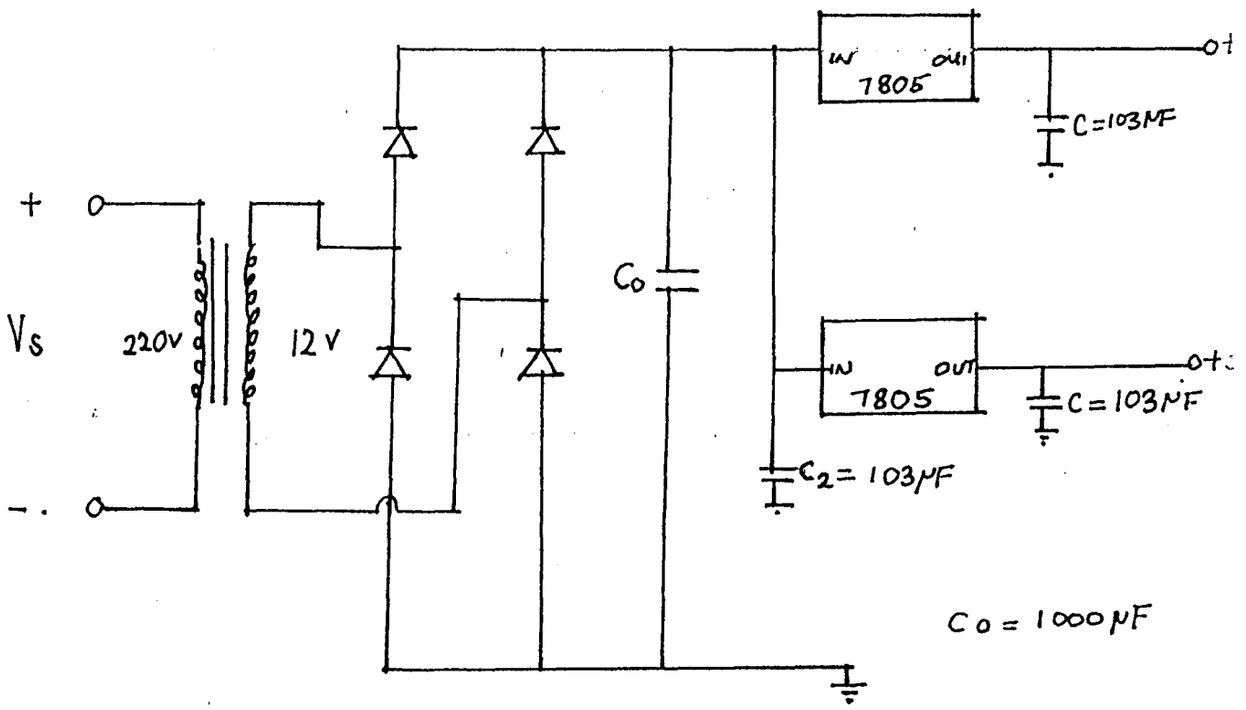


Fig 2.7.0

THE POWER CIRCUIT

CHAPTER THREE

CONSTRUCTION, TESTING, TROUBLE SHOOTING AND COSTING.

3.1 CONSTRUCTION

The design specifications are greatly considered when constructing each of the sections that comprises the DIGITAL CLOCK. The logic family employed in this project is, therefore, limited to a particular type of logic. Thus, after taking into consideration the problems associated with the interfacing of different logics, the Transistor Transistor Logic (TTL) was chosen for use. The construction of each of these sections are then elaborated in the subsequent paragraphs below.

A regulated power supply section constructed on a vero-board with the transformer rating of 220v, 500mA (Primary) and 9 volts on the secondary side which feeds the bridge rectifier that was constructed by four 1A general purpose diode. The output of the diode is now filtered by the capacitor C_1 having a value of 1000 micro µf. Two 5V, 1A regulator are used in the power construction and the connection was in parallel since the total current consumed by the circuit is greater than 1A. In accordance with the kirchoff's current law, the current will be shared by the two regulators. One of the outputs would supply both the light Emitting Diode (LED) and the decoder whilst the other output is for the rest sections. For smoothing stage in the circuit, the capacitors, C_1, C_2, and C_3 are however used.

The pulse generator was constructed using a 555 timer, as an ASTABLE MULTI-VIBRATOR. The resistors R_1 and R_2 and capacitor, C_1, with the values of 680 ohms, 6.80 Kilo-ohms and 0.1µf respectively. In chapter two, this was calculated as 1000 pulse per second as the output.

Three decade counters connected in series with the final output of 1 pulse per second was used in the construction of the frequency divider section.

Besides, the count accumulators were also constructed with the help of decade counters.

The seconds and minutes units are constructed by inputting it to pin 14, supply side, and output it from pin 11. The others pins numbered 2,3,6,7 and 10 were all grounded. The tens of seconds and minutes are constructed by inputting it to pin 14 and output it from pin 8 with pins 6,7 and 10 grounded. The pins 2 and 9 are connected together as shown in chapter two.

In the construction of the unit of I hour, a decade counter with inverted at pin 12 output was used and the tens of hour was realized using an inverter, a flip-flop (FF) and an AND gate. The decoder or driver, and display units were constructed using the output of the count accumulator as its inputs. The limiting resistors of 150 kΩ were used to reduce the output current from the decoder to the seven -segment display which was constructed by via the light emitting diodes, LED.

The states were therefore inter-linked in such an arrangement so that one stage output serves as the other stage input and so on until the stages were completed.

3.2 TESTING

Each of the units was first tested on a bread-board and each module under test was given a sizeable time to respond to test in order to ensure of their reliability. The modules were then disconnected from the bread board and transferred to the vero-board for permanent soldering using the soldering techniques. Hence, the entire circuits was tested sectionally in order to ensure that they are perfectly soldered and functioning as expected.

3.3.0 TROUBLE - SHOOTING

It is pertinent that one should be able to rectify some simple faults which might develop in the digital clock in improving the maintenance culture of the clock. Some common faults that could develop easily in the digital clock are, to this end, enumerated and useful suggestions on how to rectify them are enlisted in the table below.

FAULT (S)	POSSIBLE CAUSE (S)/ SUGGESTION	TOOLS/EQUIPMENT TO USE
Supply mains ON. power supply unit not working.	Fuse might have got burnt. Transformer or any of the components in the power supply section damaged. carry out an appropriate check on any of these components.	Lead/sucker, Multimeter, oscilloscope, soldering Iron.
Supply mains ON. power supply unit working but the clock not functioning	seven-segment LED indicator might have been burnt, counter, clock generator IC might have failed. Study the detail circuit diagram and carry out fault tracing.	Plier, IC extractor, lead/sucker, soldering Iron, oscilloscope, multimeter.

Table 3.3

3.4 COST ANALYSIS

This table gives the part list for the Digital Electronics clock and their cost. The list includes only those components used in the final production and excludes those that burnt or damaged during the course of production.

NO	DESCRIPTION OF COMPONENTS	QTY	UNIT PRICE (₦)	TOTAL COST (₦)
1.	Limiting resistors RI = 150Ω	42	7.00	294.00
2	Resistor RI = 680 Ω	1	8.00	8.00
3	Resistor R2 = 6.8kΩ	1	8.00	8.00
4	Capacitor C0 = 1000 μF	1	60.00	60.00
5	Capacitor C1 = 0.1 μF	1	40.00	40.00
6	Capacitor C2 = 0.01 μF	1	35.00	35.00
7	$C_1 = C_2 = C_3 = 103\mu F$	4	50.00	200.00
8		1	150.00	150.00
9	Transformer 220v/12v	1	100.00	100.00
10	500mA	1	80.00	80.00
11	7402 IC	5	100.00	500.00
12	7404IC	8	120.00	960.00
13	74LS47 IC	1	100.00	100.00
14	74 LS 90 IC	1	80.00	80.00
15	74 76 IC	2	100.00	200.00
16	7411 IC	2yrds	30.00	60.00
17	78 05 IC	6yrds	10.00	60.00
18	Connecting vires	4	20.00	80.00
19	Soldering lead	2	100.00	200.00
20	General purpose diode (1A)	1	30.00	30.00
21	Veroboard	2	30.00	60.00
	Push - button			
	Plastic casing			
			TOTAL	**3,305.00**

CHAPTER FOUR

4.0 DISCUSSION, SUGGESTION AND CONCLUSION

4.1 DISCUSSION AND SUGGESTION:

The design and construction of this project is aimed at obtaining accurate and less tedious

measurement of time. This was enhanced alongside some technical problems in the project design and construction. Some of these problems were enumerated below.

One of the problems encountered was in the production of pulse frequency as a 555 timer IC. To obtain a pulse pers second became a problem via the 555 timer, then the time base was used to generate 1000 pulse per second which was later divided by using three decade counter. The total output of these counter produce the required 1 pulse per second by the accumulator.

Another problem was in the power unit when the regulator output could not sustained the power consumed by the circuit. This was overcome by connecting two regulators in parallel such that one will be serving both decoder and display and the other serving the remaining part of the circuit. Also is the use of heat sink which conduct away the heat produced by the regulator. The LED are connected in numerical order for the display circuit.

Besides, at the time of construction some components were burnt. This becomes difficult and consume money in their course of their replacement as well as posing delay in the process of construction.

However, below are some suggestions for future improvement on the project:

i. There should be an incorporated mode select on the project so as to reset

the display hour and minute digit.

ii. A clear reset button may also be incorporated.

iii. Incorporation of alarm circuit which will operate on hourly bases.

Also to make the design and construction of this project easy the following suggestions were made:

The department or university should renter certain assistance to students either in cash or in kind to obtain the required components for the project.

More laboratory practical should be incorporated into the syllabus as well as some documentaries to aid electronics knowledge on campus.

Also, students could be introduced to minor project in the early levels to expose and prepare them for the challenges of the final year project.

4.3 MAINTENANCE

For reliable performance and durability of this project work, the design and constructed digital clock should be maintained properly. Thus would go a long way to reduce continuous repair on the project. Hence the digitally constructed clock should be maintained as follows:

- It should be placed in a dry, cool, well ventilated area so as to percent over heading and dirt from the clock.
- proper care should be taking when changing location of the clock so as to avoid felling or disrupting the clock.
- The power cord should be well protected to prevent open or short circuit on it.

4.3.0 CONCLUSION

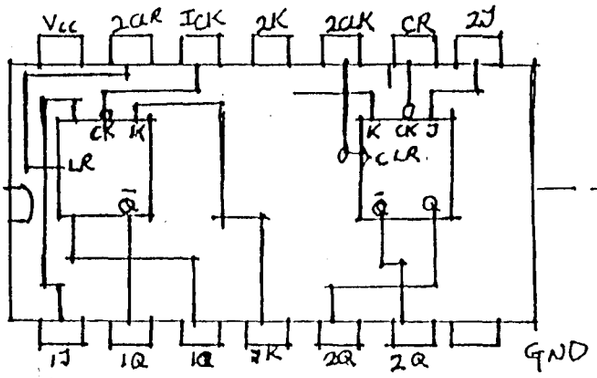
The [illegible] practical experience gained while on industrial training and the theoretical knowledge acquired from the Digital and Electronic courses offered in

the department have helped a great deal in the design and construction of this project work.

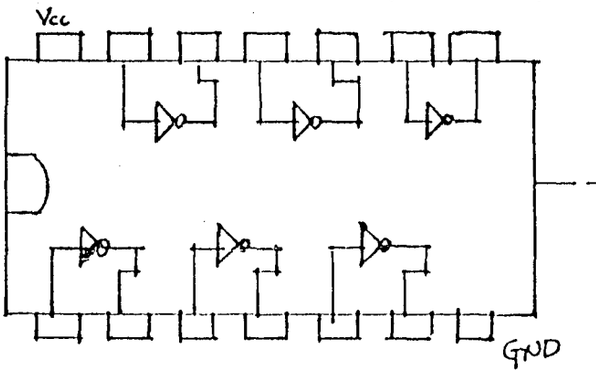
It should be noted that some discrepancies always take place when the clock is connected to the power supply. This is mainly due to the false triggering of the digital integrated circuit, IC, used. If the system is however allowed to attain a steady state, the abnormalities could be eradicated.

Thus, the required digital circuit which was the aim of this project is achieved in accordance with the desired objectives. It is, therefore, satisfactorily functioning as expected.

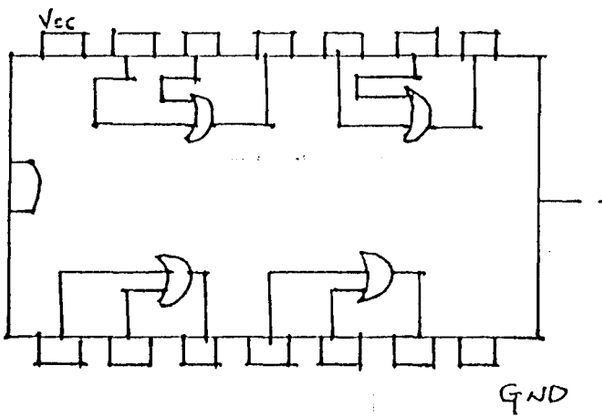
APPENDIX A



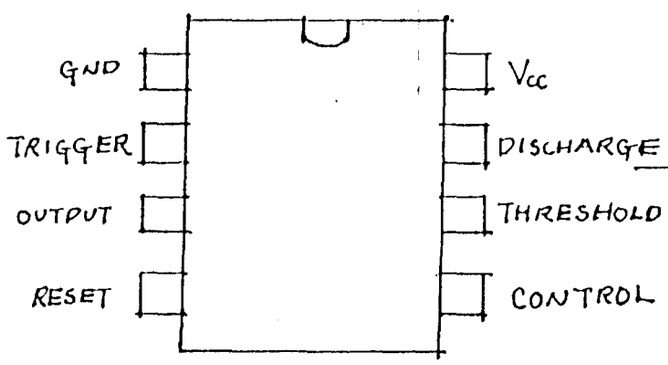
7476 JK F-IP-FI



7404 INVENTOR

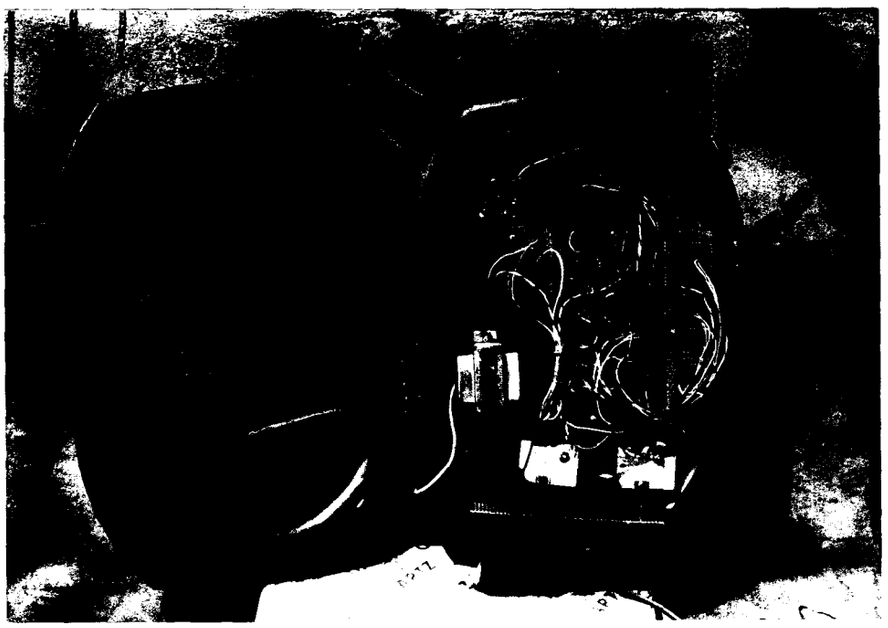


2-INPUT 7402



NE 555 TIM

APPENDIX A (II)



INTERNAL CIRCUIT OF A DIGITAL ELECTRONIC CLOCK.



A CONSTRUCTED DIGITAL ELECTRONIC CLOCK.

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