

FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA
SCHOOL OF SCIENCE AND TECHNOLOGY EDUCATION
DEPARTMENT OF INDUSTRIAL AND TECHNOLOGY EDUCATION
SECOND SEMESTER EXAMINATION 2019/2020 SESSION

COURSE TITLE: DIGITAL ELECTRONICS
COURSE CODE: ITE 562
TIME ALLOWED: 2HOURS

INSTRUCTION: ATTEMPT A TOTAL OF FOUR QUESTIONS, QUESTIONS ONE AND TWO ARE COMPULSORY

Q1a. State the main stages to creating a logic expression using karnaugh map.

b. Develop a truth table for each of the following expressions: (i) $X = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC$.
(ii) $X = \bar{A}BC + A\bar{B}C$.

c. use karnaugh maps to minimize the following expressions

(iii) $G = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BCD + A\bar{B}\bar{C}D + AB\bar{C}D + ABCD$

(iv) $F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D}$

Q2a. Prove the following Boolean expressions

(i) $A + \bar{A}B = A + B$ (ii) $A + AB = A$ (iii) $(A+B)(A+C) = A + BC$

b. prove the expression in question 2a(iii) above by means of truth table

c. simplify the following expressions

(i) $AB + A(B+C) + B(B+C)$ (ii) $AB + AC + ABC$.

Q3a. Convert the following binary numbers to hexadecimal

(i) 1100101001010111 (ii) 111111000101101001

b. Convert the following hexadecimal numbers to binary

(i) $10A4_{16}$ (ii) $CF8E_{16}$ (iii) 9742_{16}

Q4a. Implement the following circuits (i) $X = AB + CDE$ (ii) $X = AB(CD + EF)$ (iii)
 $X = \bar{A}BCD + A\bar{B}EF$ (iv) $X = \bar{A}BC + \bar{A}\bar{B}C + A\bar{B}\bar{C}$

b. Construct logic circuits using AND, OR and NOT gates for the following expressions

(i) $X = (ABC)C + ABC + D$ (ii) $X = \bar{A}BCD + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D + ABC\bar{D}$

Q5. Explain the following terms

(a) Logic probe (b) Flip-flop (c) Transistor-transistor logic (d) Complementary metal oxide semiconductor (e) The set-reset latch (f) Min-term (g) Max-term