DESIGN AND CONSTRUCTION OF A PROGRAMMABLE TIMER

BY

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Department Of Electrical And Computer Engineering School Of Engineering And Engineering Technology Federal University Of Technology Minna, Niger State.

In Partial Fulfillment Of The Requirement For The Award of A Bachelor Of Engineering (B.ENG.) Degree.

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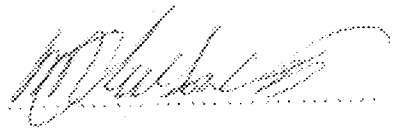
CERTIFICATION

This is to certify that this project titled design and construction of a programmable timer, was carried out by Kolawole Nurudeen under the supervision of Mr.S.N. Rumala and submitted to the department of Electrical and Computer Engineering, Federal University Of Technology Minna in partial fulfillment of the requirement for the award of a Bachelors of Engineering (B.ENG) Degree in Electrical and Computer Engineering.

Engr. S.N. Rumala

Project Supervisor

Signature & Date



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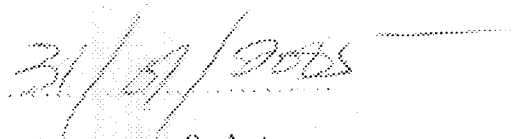

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External Supervisor

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Signature & date

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I first wish to give thanks to Almighty ALLAH, for His loving, kindness, and exceedingly great mercies that have kept me.

Also, I wish to express my profound gratitude to my parents ALHAJI & ALHAJA ABDUL-RAHEEM KOLAWOLE for the opportunity given to me to have a taste of Education in life.

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DEDICATION

This project is dedicated to the God Almighty Allah who has given me the wisdom, knowledge, spiritual and physical strength to achieved my aims on this project work. Also, to my parents ALHAJI & ALHAJA ABDUL-RAHEEM KOLAWOLE whose great love, sacrifice, and infinite courage in the midst of seeming insurmountable odds has inspired and energized me all the way.

ABSTRACT

The programmable timer is a simple, user-friendly device that can be programmed with respect to time to turn ON or OFF a supply to a device. When interfaced with a device, for example bulb, the user can afford to set the count-down timer to the require minutes (or seconds) and can hence enjoy the luxury and security of attending to some other needs knowing fully well that the circuit will cut-off main supply after the desired minutes (or seconds).

The need for such a design cannot be overemphasized since its applications are increasing from day-to-day activities both for the industrial and domestic usages.

However, the timer circuit is based on the application of counting pulses generated by means of quartz crystal which vibrates at a frequency of 32768HZ, divided by a 14 stages ripple carry binary counter/divider/oscillator (4060B) to give a clock pulse at 2 pulse per second, then divided by a flip-flop.

A relay, which is a sort of "electrical brain", performs the function of automatically triggering the timer ON or OFF when a preset number of pulses have occurred.

It incorporates basically; decoders, counters, an oscillator, the control unit, relay, and seven segments LED display.

TABLE OF CONTENT

CHAPTER ONE

GENERAL INTRODUCTION

1.1 INTRODUCTION

This chapter introduces the project titled the "programmable timer" and identifies the characteristics of its major component parts. Components parts will be introduce and the functions they perform in the timer will be described. However, there is need to determine exactly what the term programmable timer is all about.

The programmable timer is intended to provide controls for processing or manufacturing needs, or in domestic appliances based on an exact timing base, where the measurement of timer and timer-interval control are critical to successful operation without intermittent human input.

Since time is the reciprocal of frequency, any frequency standard can be used to generate a time standard, or clock. All clocks require the following elements: a power source, a governing mechanism and some form or method of read-out.

The timer circuit is divided into six major units. These are; the power supply unit (PSU), the clock generator, the counters, the seven-segment display unit, the control unit, and the relay trigger unit.

The power supply unit receives an input 9v alternating current supply from N.E.P.A., which drives the crystal. The 12V required by the CMOS used in this design to function effectively is gotten by the conversion of 220V from N.E.P.A. to 12V; the step-down transformer located in the power section does this.

The clock generator generates clock pulses. The crystal-controlled clock generator used in the design employed highly stable and accurate components called Quartz crystal. It oscillates at an accurate frequency. This particular clock generator was chosen because of the stability of its output frequency

compare with the Schmitt-trigger oscillator, the 555 timers, and RC-crystal oscillator.

The seven-segment display unit outputs decimal characteristics. The seven-segment display consists of seven lines, which are connected in common-cathode. BCD enables the display of binary numbers as decimal characters to decimal decoder/drivers. It takes a four-bit BCD input and provides an output that drives an appropriate segment of the display.

The counters are designed to work on the principle of connecting a separate set of decoder/driver and display to each counter rather than the multiplexing technique. The counters used in this project are down counters (synchronous counters). They count from a user input value down to zero. Down counters are most suitable for this particular since it is designed to know the number of input pulses that occurs.

The control unit consists of logic gate in form of ICs, flip-flops, and switches. The major functions of this unit is to preset the counters to a desired starting number which is then count down to zero.

The relay trigger unit, takes care of the execution and control operation of the external load apply. The task is executed when the 4-input OR-gate sensor indicates that the preset number of pulses has occurred and thus enables the relay to trigger OFF or ON as desire. The pull switch control of the relay opens or closes when a control current passes through the coil and an electromagnetic field is formed. Incorporated also in this unit is the transistor driver circuit for relay coil, used to control direct current from logic levels and, a diode will smoothen and protects the relay operation.

1.2 LITERATURE REVIEW

Not until somewhat recently (that is, in terms of human history) did people find a need for knowing the time of day. As best we know, 5000 to

6000 years ago great civilizations in the Middle East and North Africa began to make clocks to augment their calendars. With their attendant bureaucracies, formal religions, and other burgeoning societal activities, these cultures apparently found a need to organize their time more efficiently. [5].

The history of time keeping is the story of the search for ever more consistent actions or processes to regulate the rate of clock. Some of the earliest timekeepers include the following:

The Sumerian culture was lost without passing on its knowledge, but the Egyptians were apparently the next to formally divide their day into parts something like our hours. Obelisks (slender, tapering, four-sided monuments) were built as early as 3500BCE. The moving shadows formed a kind of sundial, enabling people to partition the day into morning and afternoon. An Obelisk also showed the year's longest and shortest days when the shadow at noon was the shortest or longest of the year. Later, additional markers around the base of the monument indicate further subdivisions of time [5].

Another Egyptian shadow clock or sundial, possibly the first portable timepiece, came into use around 1500BCE. This device divided a sunlit day into 10 parts plus two "twilight hours" in the morning and evening. When the long stem with 5 variably spaced marks was oriented east and west in the morning, an elevated crossbar on the east end cast a moving shadow over the marks. At noon, the device was turned in the opposite direction to measure the afternoon "hours" [5].

The merkhet, the oldest known astronomical tool, was an Egyptian development of around 600BCE. A pair of merkhets was used to establish a north-south line (or meridian) by aligning them with the pole star. They could then be used to mark off nighttime hours by determining when certain other stars crossed the meridian [5].

Water clocks were among the earliest timekeepers that didn't depend on the observation of celestial bodies. One of the oldest was found in the tomb of

the Egyptian Pharaoh Amenhotep I, buried around 1500BCE. Later named Clepsydras ("water thieves") by the Greeks, who began using them about 325BCE, these were stone vessels with sloping sides that allowed water to drip at a nearly constant rate from a small hole near the bottom. Other Clepsydras were cylindrical or bowl shaped containers designed to slowly fill with water coming in at a constant rate. More elaborate and impressive mechanized water clocks were developed between 100BCE and 500BCE by Greek and Roman horologists and astronomers. Some water clocks rang bells and gongs while others opened doors and windows to show little figures of people [6].

In the 14th century, large mechanical clocks appeared in the towers of larger Italian cities. Large and expensive, these clocks were integrated as communal timepieces and were weight-driven, regulated by a vergs-and-foliot escapement. Verge and foliot mechanisms predominated for more than 300years with variations in the shape of the foliot. The mechanism experienced a fundamental problem; the period of oscillation depended on the amount of driving force and friction in the drive. Like water flow, the rate was difficult to regulate [6].

Peter Henlein of Nuremberg invented spring-powered clocks between 1500 and 1510. Replacing the heavy drive weights permitted smaller, ultimately portable, clocks and watches. They slowed down as the mainspring unwound, but were popular among wealthy individuals. Because of their reduced size they could be put on a shelf or table instead of hanging from the wall [6].

Although Galileo Galilee is sometimes credited with inventing the pendulum, having studied its motion as early as 1582, Christiaan Huygens, a Dutch scientist, made the first pendulum clock in 1656. Huygens' pendulum clock was accurate to less than 1 minute a day, the first time such accuracy had been achieved. Later refinement reduced his clock's error to less than 10

seconds a day. Huygens developed the balance wheel and spring assembly around 1675. It is still found in some of today's wristwatches. This advance permitted 17th century watches to maintain an accuracy of 10 minutes per day. In 1671, William Clement of London began building clocks with the new "anchor" or "recoil" escapement. This yielded an improvement over the verge because it offers less interference to the motion of the pendulum.

By 1721, George Graham had improved the pendulum clock's accuracy to one second per day. The improved accuracy was achieved by compensating for changes in the pendulum's length due to temperature variations.

By 1761, John Harrison, a carpenter and self-taught clock-maker, refined Graham's temperature compensation techniques and added new methods of reducing friction. Building a marine chronometer with a spring and balance the British wheel escapement, he won government's 1714 prize equivalent to over $2,000,000 in today's currency by providing a mechanism capable of determining longitude to within one-half degree after a voyage to the West Indies. His chronometer maintained time on board rolling ships to about one-fifth of a second a day[6].

A century of refinements led to Siegmund Riefler's clock in 1889 with a nearly free pendulum. It attained an accuracy of a hundredth of a second a day becoming the time standard in many astronomical observatories.

The 1921 W.H. Shortt mechanism consists of two pendulums; a slave and a master. The slave pendulum pushes the master pendulum to maintain its motion, and also drives the clock's hands.

Quartz crystal clocks were developed in the 1930s and 1940s, improving time measurement technological performance far beyond the capability of mechanical arrangements. Quartz clocks are based on the piezo electric property of Quartz crystals. When an electric field is applied to a crystal, it changes its shape, conversely it generates an electric current when squeeze. When inserted into a suitable electronic circuit, the piezoelectric

inter-action between mechanical stress and electric field causes the crystal to vibrate and generate a constant frequency electric signal that can be used to operate an electronic clock display, drive a mechanical steeping motor, or provide internal clocking frequencies for electronic devices such as radios, televisions, VCRs, and computers. Quartz clocks swept the market place because their performance is excellent and they are inexpensive. They continue to dominate the market inside culturally correct timepieces.

In 1967, the 13th General Assembly on weights and measures defined the International System (SI) unit of time, the second, in terms of atomic time rather than the motion of the Earth. The second was defined as the duration of 9,192,631,770 cycles of microwaves light absorbed or emitted by the hyper fine transition of Cesium-133 atoms in their ground state undisturbed by external fields. This definition, which moved primacy from the Earth's motion to the inherent frequency of Cesium 133 atoms lead to problems which were resolved by the development of Coordinated Universal Time (UTC) in 1972. Recent improvements in Cesium time measurement technology include replacement of the state-selection magnets with laser beams, which can detect, select and measure electron transitions with greater efficiency and less noise from the radiating atoms. Cesium is the best choice of atom for such a measurement because all of its 55 electrons but the outermost are confined to orbit in stable shells. Hence, the outermost electron remains relatively undisturbed by the other electrons. The Cesium atoms are kept in a very low vacuum amounting to approximately 10 trillionths of an atmosphere. This insures that the Cesium atoms are little affected by other particles. Consequently, the Cesium atoms radiate in a narrow spectral line whose wavelength or frequency can be accurately determined[6].

In the 1840s a railway standard time for all of England, Scotland, and Wales evolved, replacing several "local time" systems. The Royal Observatory in Greenwich began transmitting time telegraphically in 1852 and

by 1855 most of Britain used Greenwich time. Greenwich Mean Time (GMT) subsequently evolved as an important and well-recognized time reference for the world [5].

In 1830, the US Navy established a depot, later to become the US Naval Observatory (USNO), with the initial responsibility to serve as a storage site for marine chronometers and other navigation instruments and to "rate" (calibrate) the chronometers to assure accuracy for their use in celestial navigation. For accurate "rating", the depot had to make regular astronomical observations. It was not until December of 1854 that the secretary of the navy officially designated this growing institution as the "United States Naval Observatory and Hydrographic office". Through all of the ensuring years, the USNO has retained timekeeping as one of its key functions.

With the advent of highly accurate atomic clocks, scientists and technologists recognized the inadequacy of timekeeping based on the motion of the earth, which fluctuates in rate by a few thousandths of a second a day. The redefinition of the second in 1967 had provided an excellent reference for more accurate measurement of time intervals, but attempts to couple GMT (based on the Earth's motion) and this new definition proved to be highly unsatisfactory. A compromise time scale was eventually devised, and on January 1, 1972, the new Coordinated Universal Time (UTC) became effective internationally.

UTC runs at the rate of the atomic clocks, but when the difference between this atomic time and one based on the Earth approaches one seconds, a one second adjustment (a "leap second") is made in UTC. NIST's clock systems and other atomic clocks located at the USNO and in more than 25 other countries now contribute data to the international UTC scale coordinated in Paris by the International Bureau of Weights and Measure (BIPM). As atomic timekeeping has grown in temperature, the world's standard laboratories have become more involved with the process, and in the United

States to day, NIST and USNO cooperate to provide official US time for the nation [6].

Interestingly, the standard timekeeping system related to this arrangement of time zones was made official in the United States by an Act of congress in March some 34 years following the agreement reached at the international conference. In an earlier decision prompted by their own interests and by pressures for a standard timekeeping system from the scientist community-meteorologist, geophysicists and astronomers-the US rail road industry anticipated the international accord when they implemented a "Standard Railway Time System" on November 18,1883. This Standard Railway Time, adopted by most cities, was the subject of much local controversy for nearly a decade following its inception [6].

Over the years, numerous models of timer devices have been used by man to achieve a reliable and accurate time reference base for scheduling one or more domestic and industrial events with reference to time. However, with man's quest to make life more comfortable and safe, effort is being made to move from old methods to inventing the best method.

However, the technology advancement in this era has brought us to situations in industries where timer-interval control are critical to the successful operation of certain processing or manufacturing operation which may not permit human intervention or supervision, hence, programmable timers will play a very vital role in controlling such events [3].

CHAPTER TWO

DESIGNS AND ANALYSIS

2.1 PRINCIPLES OF OPERATION (Figure 2.1).

(i) Oscillator/Divider

Oscillator/Divider holds mainly the 4060B and 4027B. The 4060B is Oscillator/Divider CMOS integrated circuit, which generates 32768Hz from a crystal. And, provides a precision frequency of 2Hz from one of its pins (pin 3 to be specific).

The 4027B toggle flip-flop divides the output frequency one more time and the result of a 1Hz (1 second period) frequency output is obtained, which is controlled to the counter stage.

(ii) Counter

This stage embodies two groups of counters, one for the minutes and the other for the seconds. The maximum count for second is 59 and at that point it triggers the minute counters, whose maximum count is 99.So, the timer operating limit is 99minutes 59 seconds (roughly one hour and forty minutes).

(iii) Display Logic

The display merely converts the binary codes from the counters into visual information. Through the use of 4511B (BCD to seven- segment decoder) and common cathode display.

(iv) Control

The control is used to presets the aimed time into the counters. It involves switching ON of some particular soft buttons for minutes, seconds, and preset modes. After then the start button activates the counters to decrement down to zero from the initial preset time.

(v) Zero detectors

This is made up of OR gates, which indicates the zero code at the counters output. This detects the preset time and fed the result to the output loading for external switching.

(vi) Output loading

This involves a transistor and a 10A, 12V relay. The transistor is controlled by the zero detectors and cuts off the relay switch whenever zero is detected or the preset time has been reached.

The block diagram of the principle of operation of the timer is given in figure 2.1

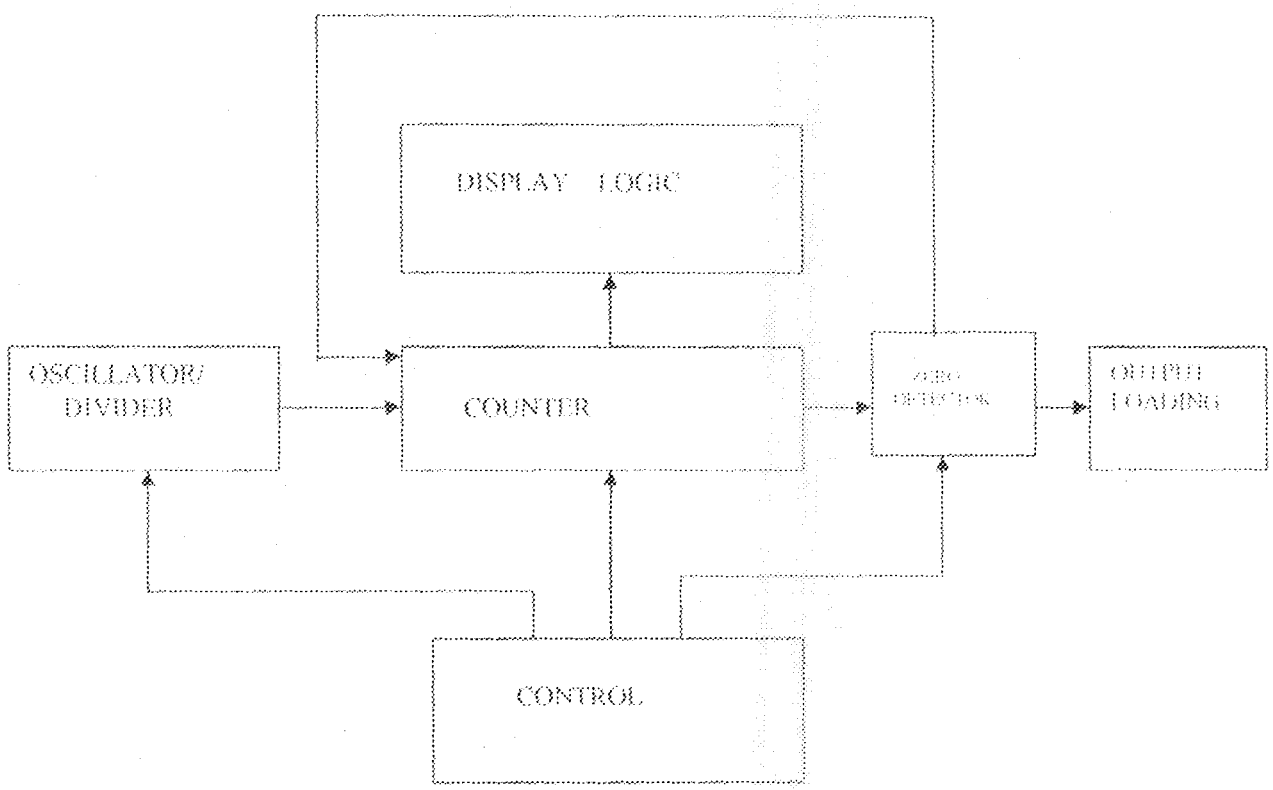

Fig. 2.1 Block Diagram Of The Timer.

2.2 DESCRIPTION OF CIRCUIT OPERATION (Figure 2.2).

The timer uses one of the common applications of counters, which counts pulses coming out of a pulse generator at a frequency of 1HZ(i.e. one pulse per second 1PPS). This clock signals are generated by a highly stable and accurate components called a quartz crystal, which vibrates (resonate) when excited at a precise frequency.

The oscillator/divider consists of 4060B and 4027B. These CMOS (complementary metallic oxide semi conductors) integrated circuits operate a crystal at 32.768KHZ. The I.C has 14JK flip-flop inside in which the frequency is divided 14 times down to 2HZ(0.5 second). Further division through addition toggle flip-flop 4027B produces 1HZ(1 second) pulse required for the effective counter operation.

The four counters are divided into two groups. One group (2 counters) for seconds counting from 0 to 59 (e.g. 60 seconds) and the other group for counting minutes from 0 to 99 (e.g. 99minutes). Therefore, maximum timing is 99.59 minutes. The pin 5 of the first group (counter) holds the control configuration for starting counting and stopping further counting after zero is detected. This is done by the feedback from the zero detector back to the OR gate which disables the pin5 (clock enable of the timer), the feedback signal is (s).

The SR flip-flop in the circuit for controlling the time setting holds Q and $\overline{Q}$. These two are the main control terminals. When the counter is at the set mode i.e. to input a value (e.g. 30seconds), which then counts down, Q is 1 and $\overline{Q}$ logic 0. For Q is 1 at AND gate1, it disables the clock enable pin5 because, the other terminal of the AND gate is already logic1.

Therefore, to set the counters, pressing switch1 (SW1) makes AND gate1 output logic0 and, then pin5 is logic0. Logic0 enables the counter

point(s), the feedback is then logic0. The same thing for switch2 (SW2). OR gate 4 is used for cascading.

4029B 2 should have a maximum of digit5, so that, 4029B 1 and 2 have 59 maximum output. Therefore, OR gate 2 and AND gate 6 are used to make this possible. They help to clean off the counter through pin 1 whenever code six (6) is detected.

The speed selector is designed to select speed 2Hz(e.g. 0.5 second) when setting a number and 1Hz (e.g. 1 second) when in the counting down mode. The speed selector is just a simple 2-1 multiplexer, 1Hz and 2Hz are both fed to its outputs. Q and $\overline{Q}$ are the control logic, which select which frequency to be at the common clock to the counters at a specific time.

The output holds OR gate1 (4-inputs), which detects zero at the output, points to the counters. The output at the OR gate is inverted through NOT gate1 e.g. from logic0 when zero is detected to logic1.

AND gate 5 is used to control the output so that the zero detector can only effects the output load only when the system is in the countdown mode. Output (s) switches the transistor, which drive the relay for external switching OFF and ON as desired. The signal(s) is fed back to OR gate 3 so that when zero is detected the system or counting stops.

The display is associated to 4511B (7-segments decoder). It turns the 4-bit outputs from the counters into 7 driving outputs that power each 7-segment display.

The relay circuit embodies a transistor, resistor, and 12v relay. The transistor-resistor circuit drives/switches the relay ON or OFF through the logic at the control output. When the logic is 0, the relay is cut-off. But when logic is 1, the relay is energized. At this point, the display is 0000 because the counters have counted down to the ground (zero).

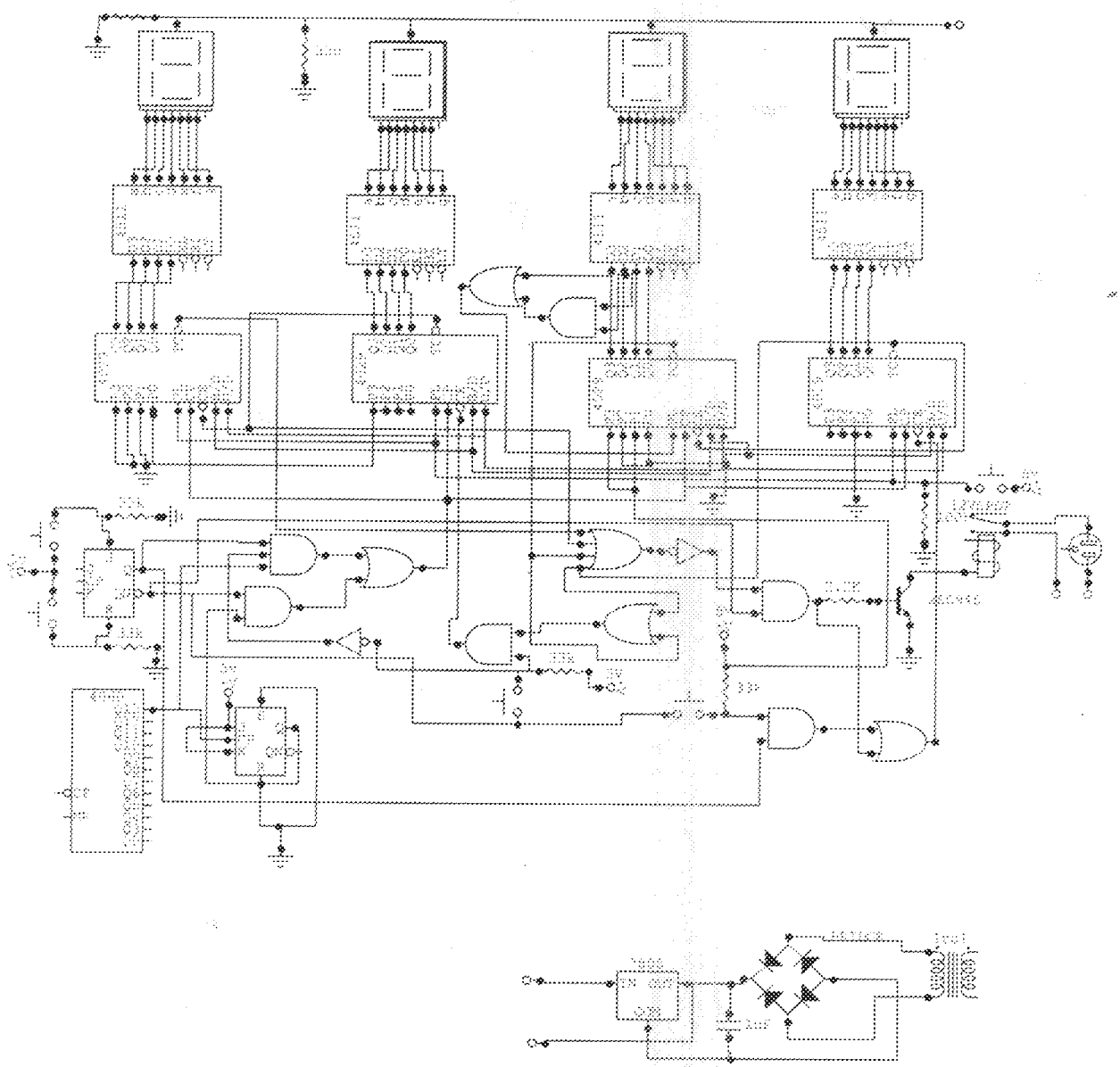

Fig.2.2: The programmable Timer Circuit

2.3.0 LOGIC FAMILY SELECTION

The CMOS family is widely used in this design because it has very low power consumption and is perfect battery operated electronic devices, which satisfies the requirement for this project. The Transistor-Transistor Logic (TTL) was not used for this project because of its high power consumption. Also, Emitter-Coupled Logic (ECL) was not since ultimate speed is not required in this design.

The following reasons explain why the CMOS family was used for this project:

i. They do not respond to very fast noise pulses or circuit glitches because of its slower speed.

ii. They have a large (good) noise immunity (rejection) than other logic families.

iii. It is possible to pack more gates into the IC without running into heat dissipation problems because of lower power consumption.

iv. They are readily available in the market.

v. They impose fewer restraints on the power supply (+3v to +18v at very low currents).

2.4.0 THE POWER SUPPLY UNIT (PSU)

The power supply unit forms an important aspect of the project construction. It is a very important primary factor that determines whether the project works or not.

Generally, CMOS are usually driven by a battery supply or A.C supply because of their current drain, which is ranging from +3v to +18v.

For this project, a 240Vrms/12Vrms,step-down transformer was used to reduce the 240Va.c. from the public power supply authority (in this case N.E.P.A.) to 12Va.c.Since 9Vd.c.was chosen as the supply voltage for the

circuit, this 12Va.c. has to be rectified and regulated. This a.c. supplied is used to drive the circuit. Therefore, the difficulty of designing the power supply unit is extremely unavoidable and also the use of power supply regulated IC is required because of the voltage range.

Therefore, process of power delivery to the circuit can last for a long time as required, compared with when supply from a battery is used, whose power delivery can only last for a finite time. This is because as the current is drawn from the battery, the chemical components in the battery are consumed, the battery decreases towards zero, and we say that the battery is discharged at this point. However, the rate of discharge depends on how much current is drawn from the battery by the circuit. At higher currents, the battery lifetime is shorter. The transformer unit is given in figure 2.3

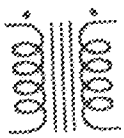

Fig. 2.3. Transformer Circuit Symbol.

For the transformer, the following relationships are valid:[3]

$$\frac{N_p}{N_s} = \frac{V_p}{V_s} = \frac{I_s}{I_p}$$

Where:

Np = number of turns of the coil on the primary side

Ns = number of turns of the coil on the secondary side

Vp = primary voltage

Vs = secondary voltage

Ip = primary current

Is = secondary current

Therefore, the required 12V by the CMOS used in this design to function effectively is gotten by the conversion of 220V, from N.E.P.A., to 12v by the step-down transformer located in the power section.

2.5.0 THE CLOCK (PULSE) GENERATOR

2.5.1 THE QUARTZ CRYSTAL

The clock pulse generator used in this project is the Quartz crystal. The quartz crystal has a mechanical resonant frequency at which it oscillates when excited.

A piece of quartz crystal can be cut to a specific size and shape to vibrate (resonate) at a precise frequency that is extremely stable with temperature and age. Frequencies from 10KHZ to 80MHZ are readily achievable. The operating frequency for the crystal used in this project is 32768HZ(or 32.768KHZ), 2^{14} counts per second.

Timers need to have accurate, stable clock pulses available. A quartz crystal, together with a simple circuit to generate digital pulses, fits the need of this project perfectly compared to the use of 555timer and Schmitt trigger as clock pulse generators.

2.5.2 THE CONTROL UNIT

The control unit is the pivot of the timer. It determines how the timer functions. Its major function is to preset the counters to the desired starting count or resetting of the counter as the case may be.

2.5.3 THE SWITCHES

All the switches used in this design work are on a panel (pad) from which the operation of the timer is carried out using appropriate buttons to perform a desired operation. The panel is a matrix of switches arranged in column and rows. Depressing a button (switch) short-circuits a row and a column. The panel is connected to each counter. Each switch has its unique function.

2.6 SEVEN SEGMENT DISPLAY DECODER/DRIVER

2.6.1 SEVEN SEGMENT DISPLAY UNIT

The display type used in this design is the Light Emitting Diode (LED) seven-segment display. The LED was used because of its brightness, low-cost, reliability, and compatibility with low voltage integrated circuitry. It can display the digits 0-9.

Lighting some subset of the seven segments as shown in figure 2.5 can form each decimal digit

The LED used in the design is a common-cathode type where the cathodes of all the segments are tied together and connected to ground. A BCD drives the display read out to seven-segment decoder/driver with active HIGH outputs that apply a HIGH voltage to the anodes of those segments to be activated. The seven-segment display is available in form of an IC.

The anodes are connected to the output of the CD4511B decoder. All the anodes of the LEDs are connected through the current-limiting resistors, to the appropriate outputs of the decoder/driver. By controlling current through each LED, some segments will light (1) and others will be dark (0) so that the desired character pattern will be generated.

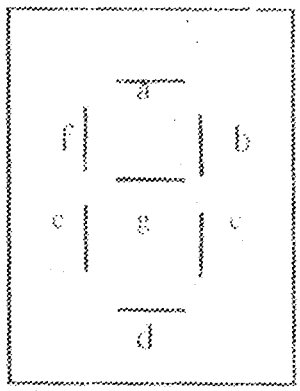

Figure 2.5 Seven-segments LED indicator arrangements [2].

2.6.2 BCD-TO-7-SEGMENT DECODER/DRIVER

A decoder is a circuit used to change a coded input, such as the BCD, to another code. The CD4511B used in this design takes a four-bit BCD input from the output of CD4029B counters and provide the outputs that passes current through the appropriate segments to display the decimal digital [2].

THE S-R LATCH

(i) The CD4027B

This is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J-K set, Reset, and clock input signals. Buffered

Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic level present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive going transition of the clock pulse. Set and reset

functions are independent of the clock and are initiated when a high level signal is present at either the set or reset input. The CD 40207 types are supplied in 16-lead hermatic dual – line ceramic packages (0 and F suffixes), 16-lead dual – in-line plastic packages (suffix) and in chip form (H-suffix).

It features include:

* Set – Reset Capability
* Static Flip-flop operation – retains indefinitely with clock level either "high" or "low".
* Medium speed operation – 16MHZ, clock toggle rate at 10v.
* Standardized symmetrical output characteristics.
* 100% tested for quiescent current at 20v.
* Maximum input current of 1μA at 18v over full package – temperature; 100nA at 18v and 25oC.
* Noise margin (over full package – temperature range)

1v at V_{DD} =5v

2v at V_{DD} =10v

2.5v at V_{DD} = 15v [3]

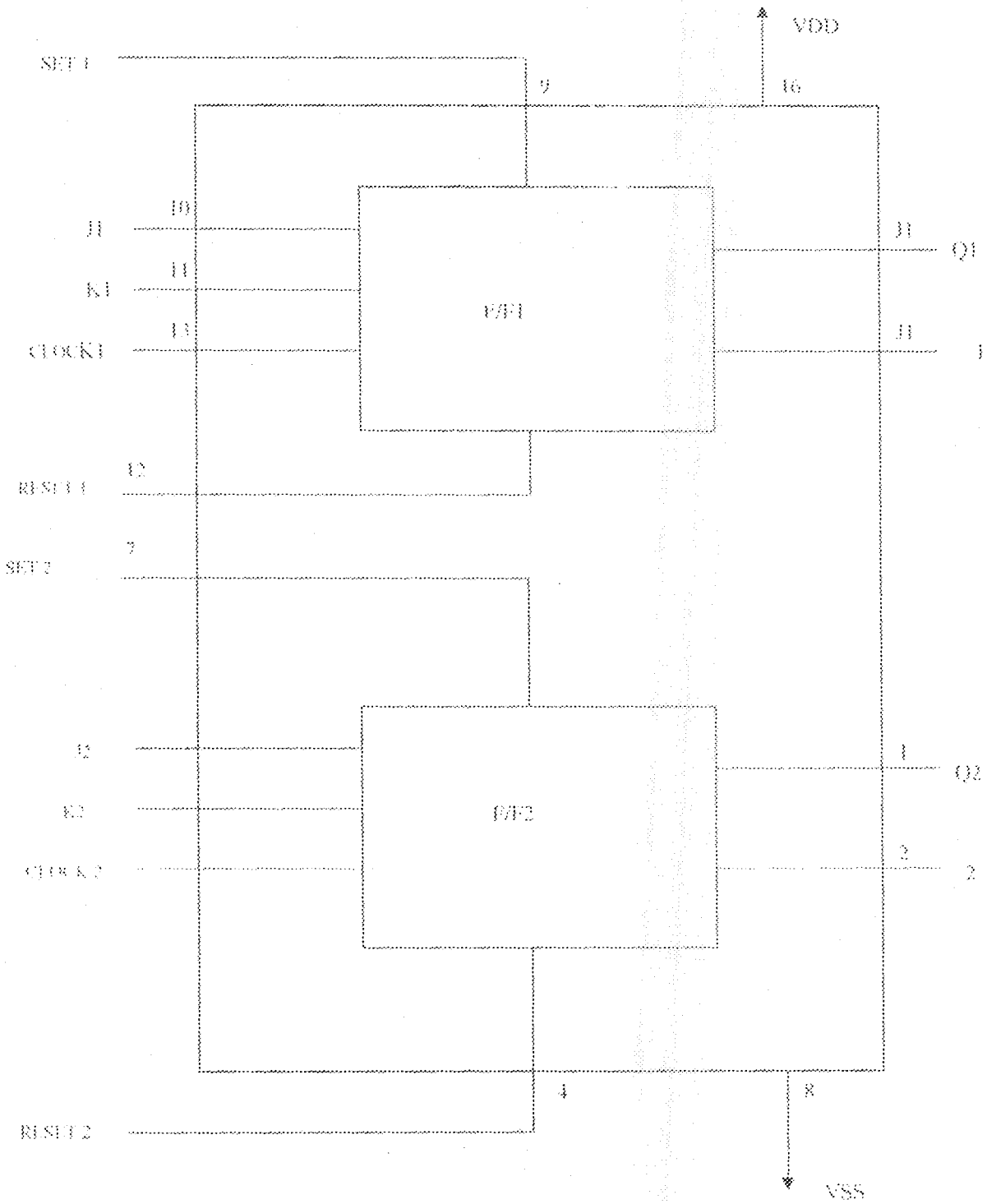

Fig. 2.6A Functional Diagram of CD4027B

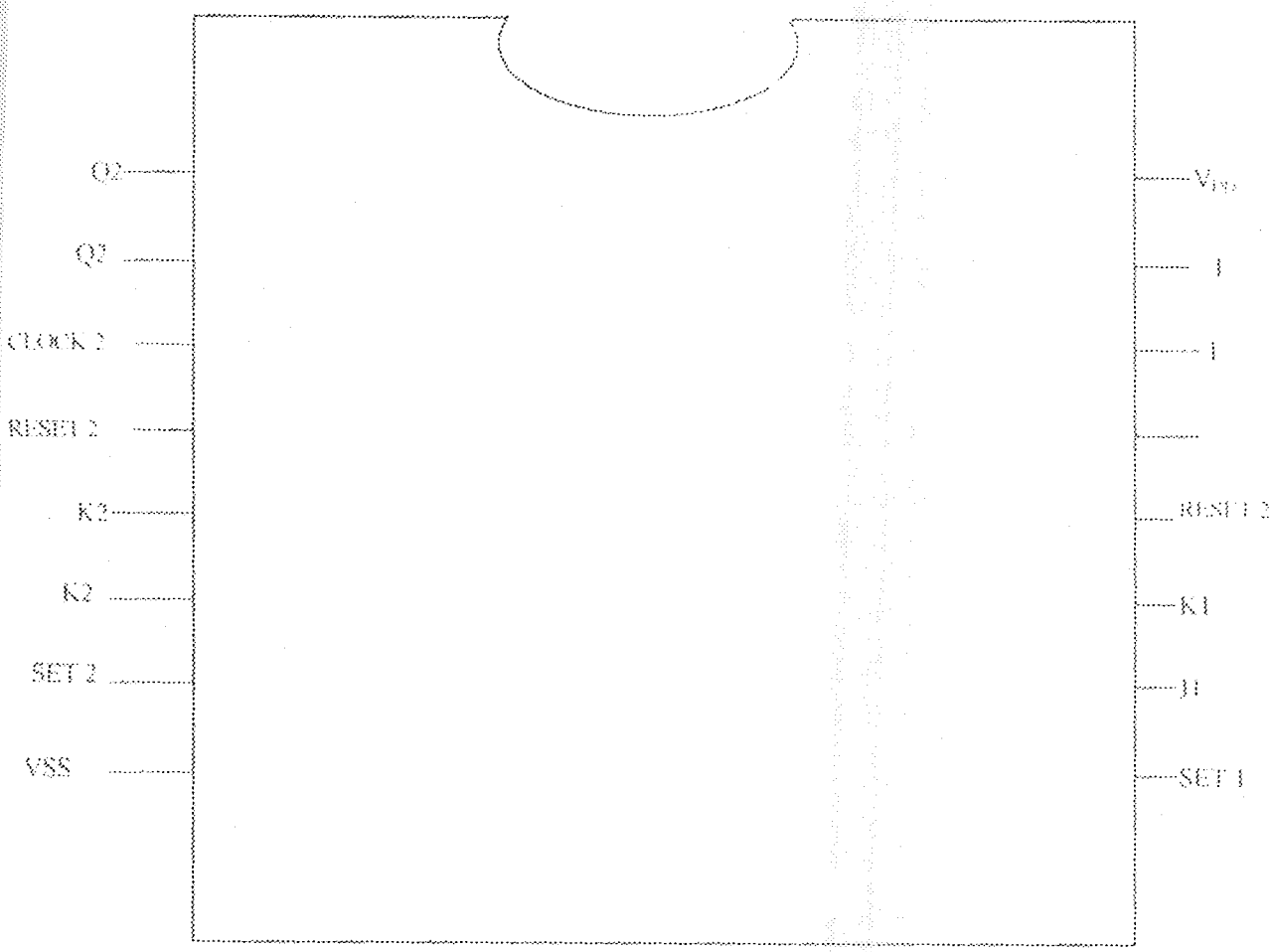

Fig. 2.6B Pinning assignment for CD4027B

The CD4027B integrated circuit has provisions for J-K, Set, Reset and clock input signals. Therefore, the clock and J-K inputs are grounded which permits the use of J-K master flip-flop as SET(s) – RESET(R) LATCH. Set and Reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input and the output signals are produced as buffered signals Q and O. The leading IC divides the frequency 14 times (e.g. 224=16,384). Therefore, the output is 2HZ (0.5 second) and further division through addition toggle flip-flop 4027B produces 1HZ (1 second) pulse required for the effective counter operation.

(ii) CD4511B

This is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active Low latch enable input (EL), an active Low ripple blanking input (BI), an active Low lamp test input (LT), and seven active HIGH n-p-n bipolar transistor segment output (Oa to Og).

Applications of CD4511B include:

* Driving LED displays
* Driving incandescent displays
* Driving fluorescent displays
* Driving LCD displays
* Driving gas discharge displays[1].

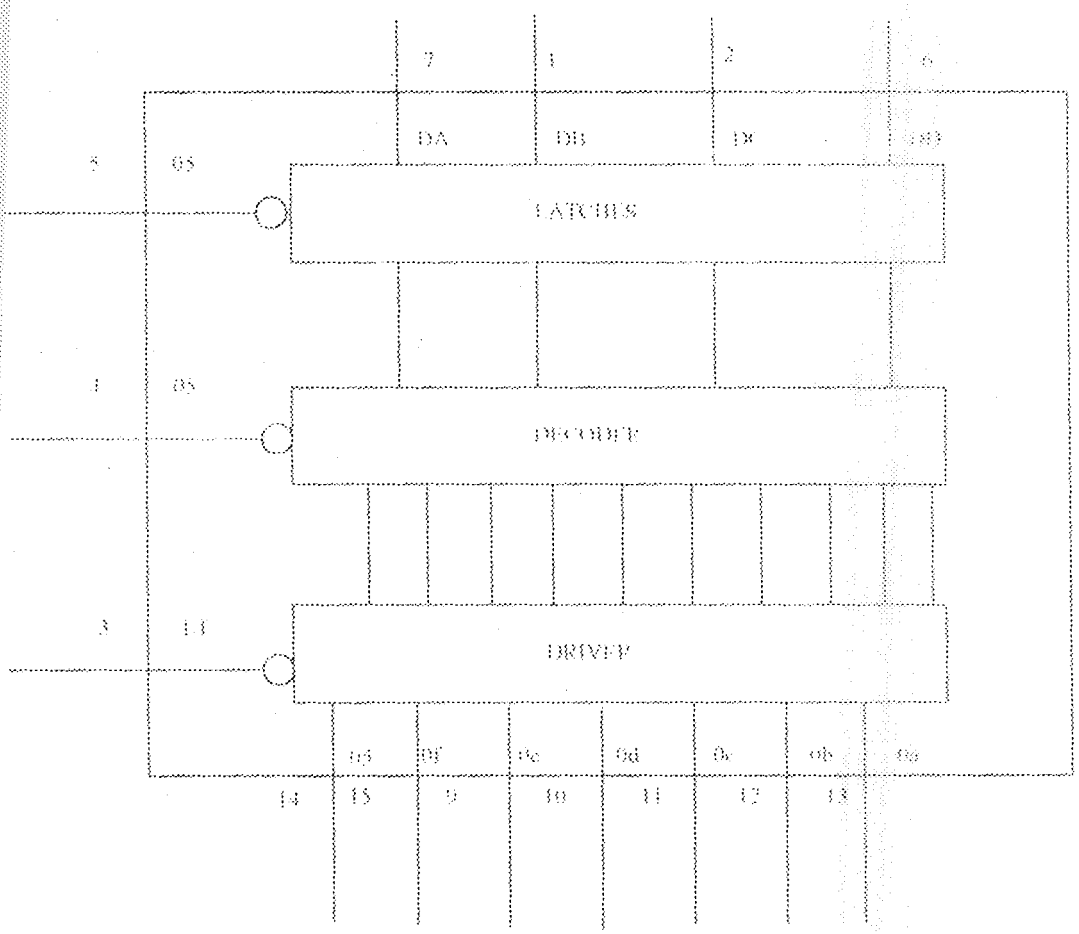

Fig. 2.6C Functional diagram of CD4511D

When $\overline{EL}$ is Low, the state of the segment outputs (Oa to Og) is determine by the data on D_A to D_D.

When $\overline{EL}$ goes High, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is Low, all the segment outputs are high independent of all other input conditions. With $\overline{LT}$ High, a Low on $\overline{BI}$ forces all segment output Low. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

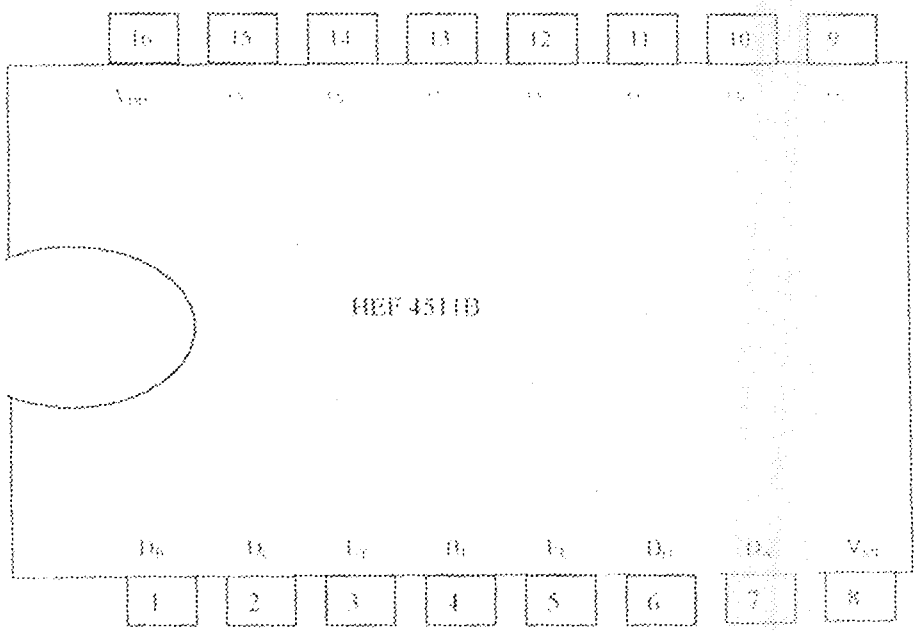

Fig.2.6D Pinning assignment diagram of CD4511B

PINNING

D_A to D_D = address (data) inputs

$\overline{EL}$ = Latch enable input (active low)

$\overline{BI}$ =Ripple blanking input (active low)

$\overline{LT}$ =Lamp test input (active low)

Oa to Og = Segment outputs

(iii) The CD4029B

This is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1", the counter counts in binary. Otherwise, it counts in decade. Similarly, the counter counts up when the up/down input is at logic "1" and vice versa.

A logical "1" preset enable signal allows information at the "jam" inputs to presets the counter to any state asynchronously with the clock. The counter is advanced one count at the positive – going edge of the clock if the carry in and preset enable inputs are at logical "0"

Advancement is inhibited when either or both of these two inputs is at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and Vss.

Its features include:

* Wide supply voltage range

*High noise immunity

*Low power TTL compatibility

*Parallel jam inputs

*Binary or BCD decade up/down counting [7].

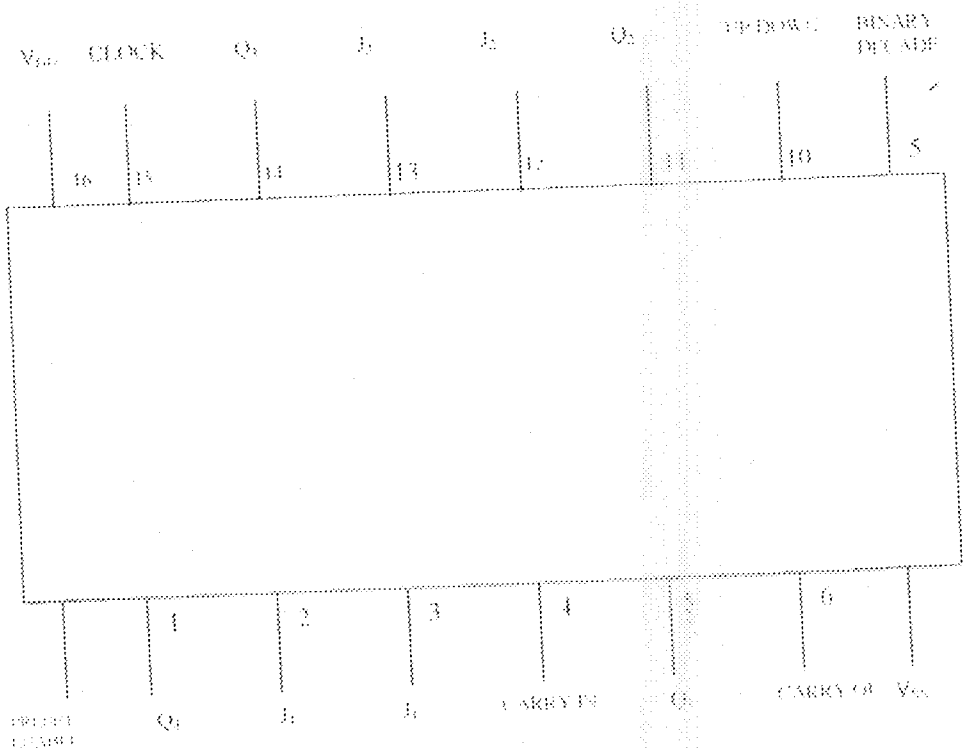

Fig. 2.6 E Pinning assignment for CD4029B

(iv) The CD4060B

They are 14-stage ripple carry binary counters. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the Zero state by a logical "1" at the reset input independent of clock

The features of CD4060B include:

* Wide supply voltage range
* High noise immunity
* Low power TTL compatibility
* Medium speed operation
* Schmitt trigger clock input [7].

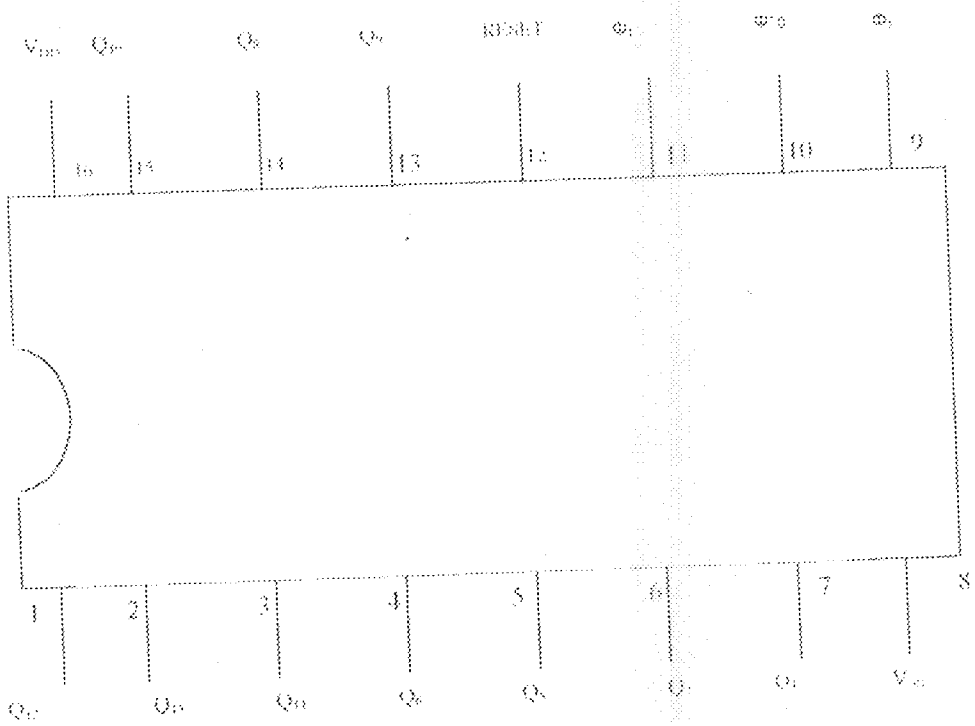

Fig.2.6 F Pinning diagram of C D4060B

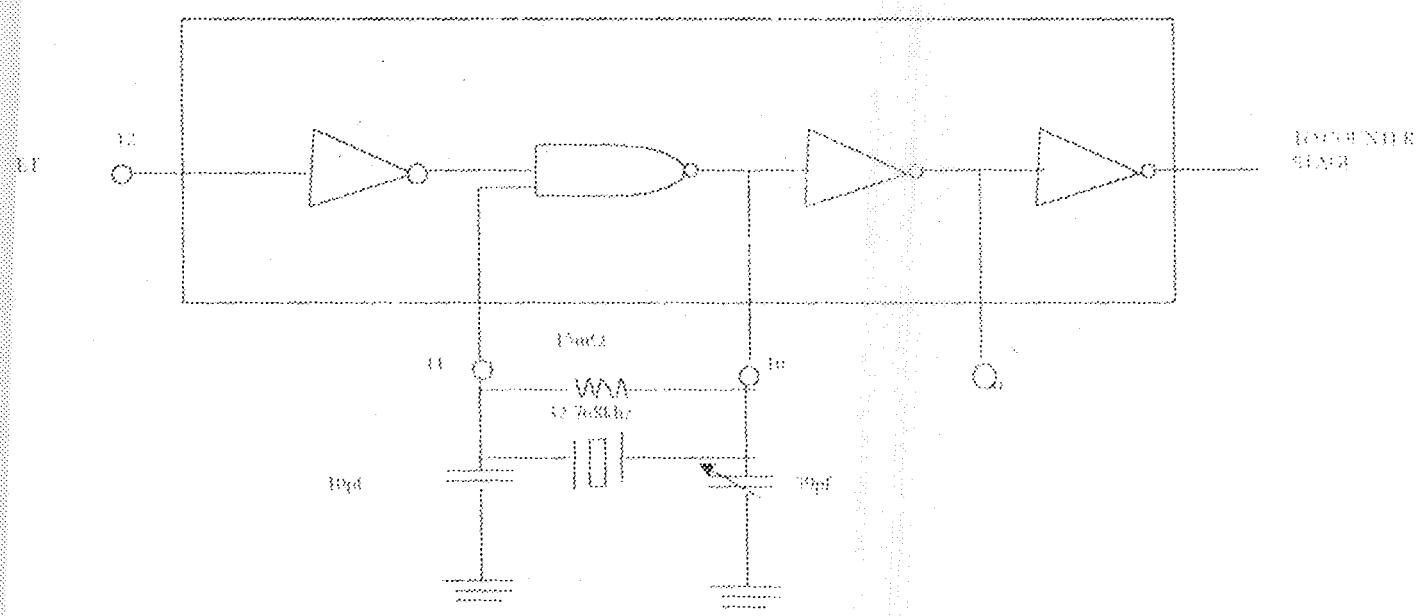

Fig.2.6.C Square oscillator based on CD4060B

CHAPTER THREE
CONSTRUCTION OF THE PROGRAMMABLE TIMER

3.1 INTRODUCTION

The design work having been done, a prototype model was built (on the bread board) before the circuit was transferred to the Vero board for permanent mounting. After the testing of the circuit layout on the Vero board and a satisfactory result was obtained, a protective casing was designed and constructed to house the circuit.

3.2 CONSTRUCTION DETAIL

The circuit construction is divided into two parts:

-the power supply unit;

-the control circuit and the driver.

The power supply unit was built with the transformer as the first component on the Vero board. The primary end of the transformer was connected to two legs of the bridge rectifiers. Across the two other legs of the rectifier, an electrolytic capacitor was connected with the right polarity. The connection was then made to the three terminal voltage regulators to yield the required 12V d.c required for the circuit operation.

Other components were mounted beginning with resistors and capacitors. The relay was then positioned using the five – pin guide and soldered into the board. Diodes D1, D2, D3 and D4 came next. The seven – segment display was soldered and finally, the switches were soldered.

During the construction process, care was taken to ensure that the right components were in the right place and with the correct polarity. Interconnections were made through etching of the Vero board and the use of insulated copper wires. All excess wires were neatly clipped, making sure that all of the soldered connections were properly made. The components were laid

out on the Vero board with enough space to give room for ventilation, troubleshooting, and replacement of faulty components.

After the testing, a protective casing was designed and constructed to house the circuit. The read out display and the control switches were mounted in the front panel for easier reading and identification respectively. They were held in place with the help of a couple of drops of super glue. The scanned pictures of components layout on the copper clad matrix board (Vero board) and the casing were shown in fig.3.1 and fig.3.2 respectively.

The choice of materials used for the construction of the casing is based on the cost, the strength, reliability, and physical outlook. It is a wooden casing, which is perforated for ventilation reason during the operation of the system; it is prevented from any risk of short circuitry of the soldered components because the wood is a good insulator.

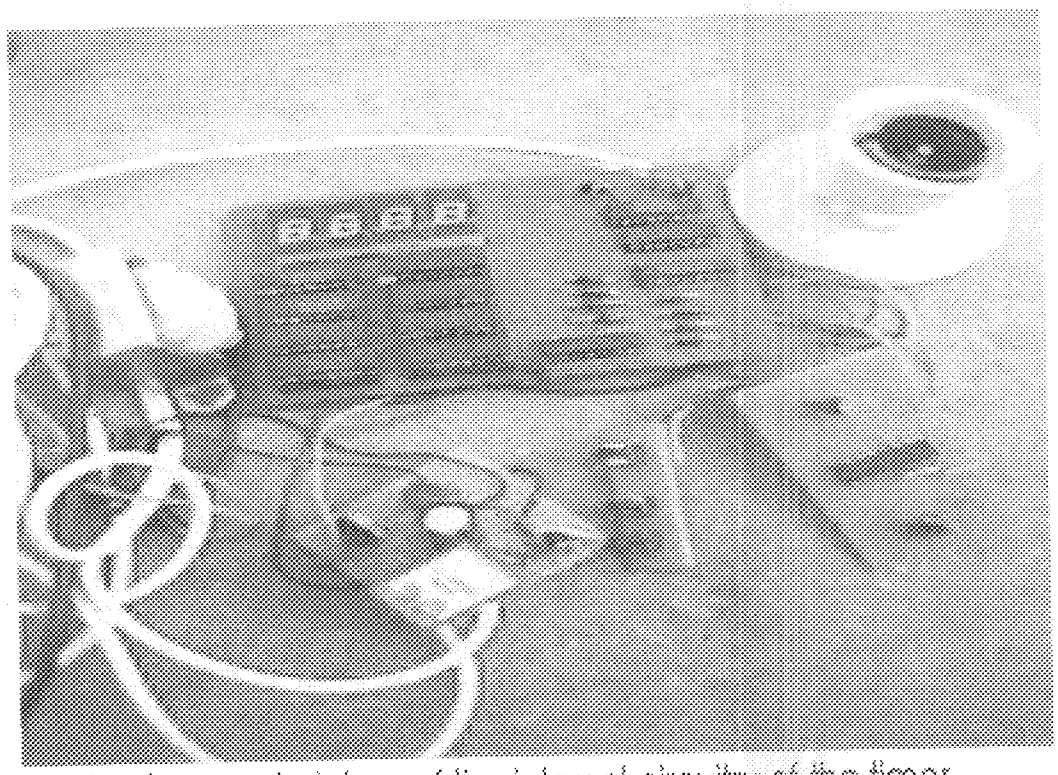

Fig 3.1 Scanned picture of the internal circuitry of the timer.

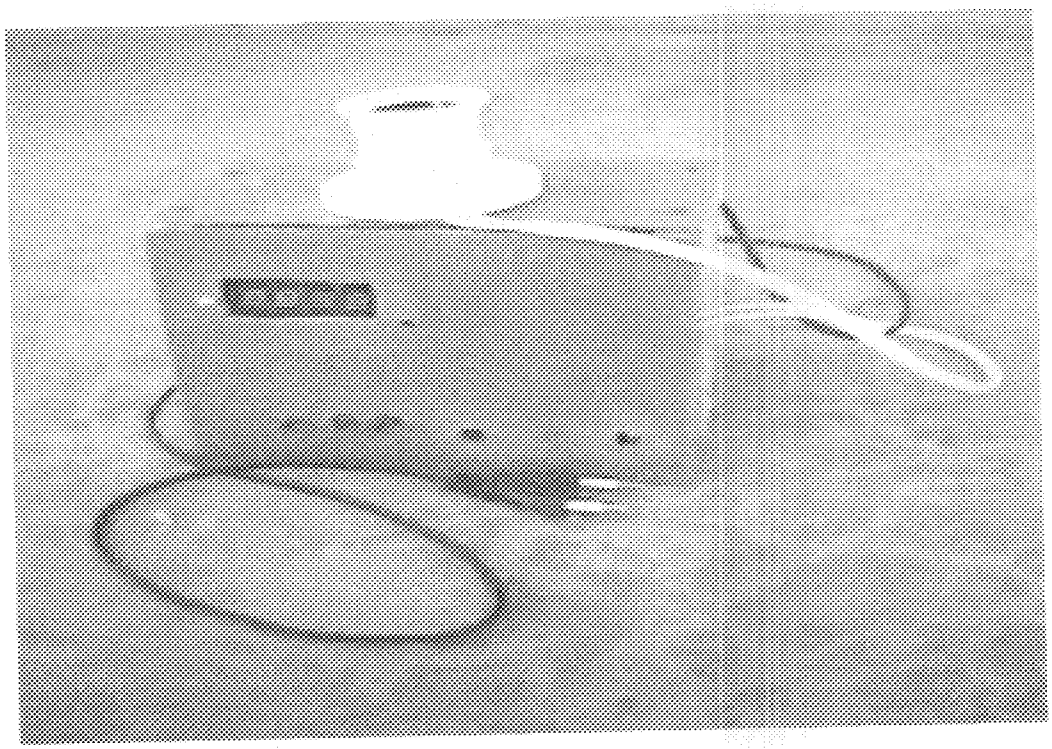

Fig 3.2 Scanned picture of the coupled timer

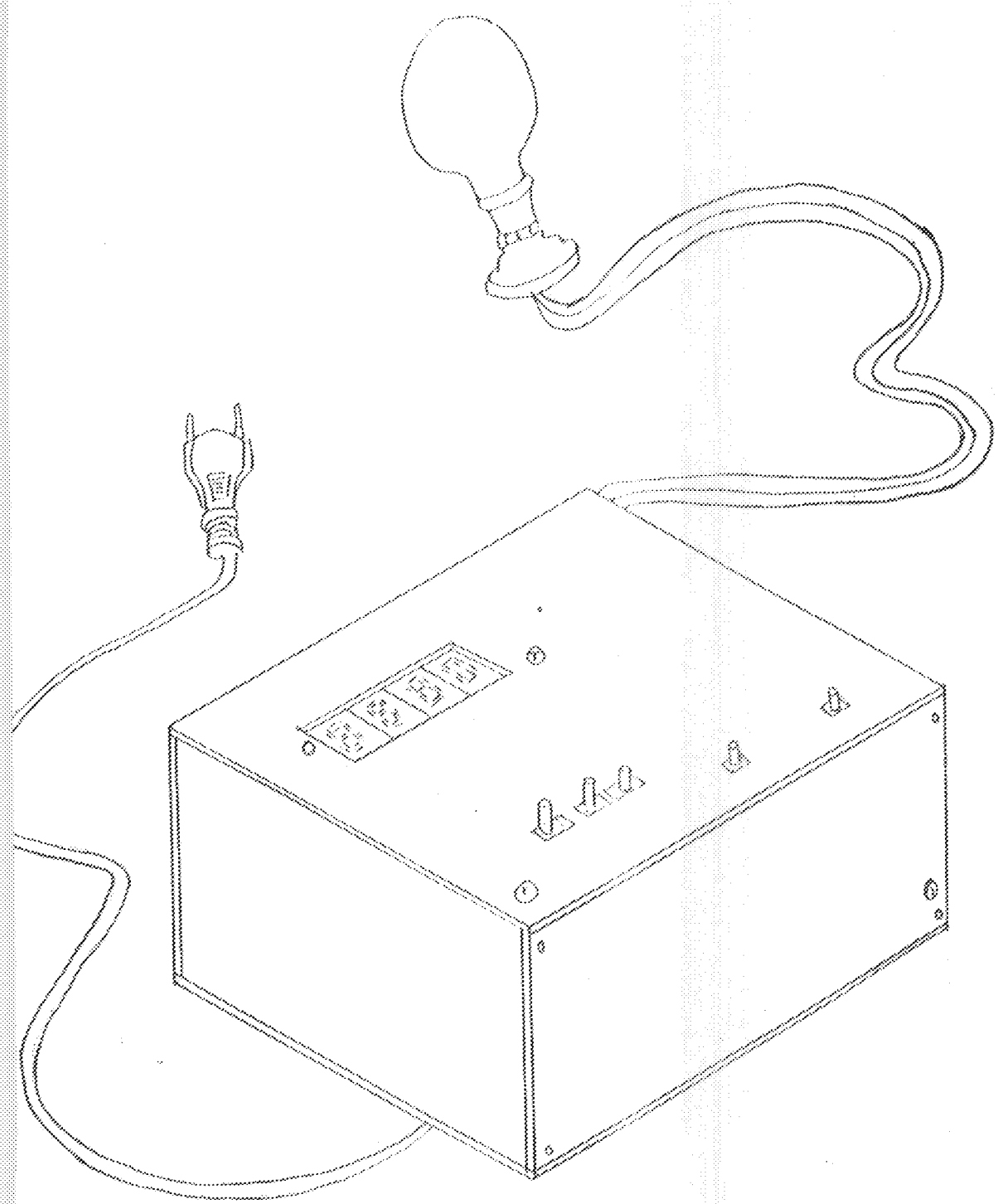

fig 33 Isometric Sketch of the Casing

3.3 THE COMPONENTS LISTING:

Most of the components used were in the form of integrated circuits (ICs). Detail lists of the components used are given below. All the ICs used are of the complementary metal-oxide semiconductor (CMOS) family

S/N	COMPONENTS TYPE	QUANTITY USED
1	CD4511B Decoders	4
2	CD4029B Counters	4
3	CD4027B Dual J-K Master flip-flop	2
4	CD4060B Divider/Oscillator	1
5	CD7805B	1
6	CD4081B Quad-2-input AND gate	1
7	CD4071B	1
8	CD4069B Hex inverter (NOT gate)	1
9	CV Relay	1
10	Resistors: 33k, 10k	5
11	Diode IN4001	4
12	Quartz crystal	1
13	Capacitors Ceramic 75pf, 30pf	1
14	Soldering lead	Few yards
15	Seven-Segment LED indicator	4
16	Vero board	1
17	Connection wires	Numerous
18	Bush buttons	5

3.4 TESTING

On completion of the construction, a careful test of the completed circuit was conducted against another timer device (i.e digital wrist watch). A 60W bulb was used as an external device (indicator), which was turned ON with the aid of the start button.

The set switch was used to adjust the counters to the require timing. And the start switch was pressed and the counters begin to count down to zero. The digital wristwatch was simultaneously used for the timing.

3.5 RESULT

When the counters reached 0000, the relay triggered/switched off the bulb and this took place at exact time the digital wristwatch indicated the presumed count-level.

Therefore, this digital wristwatch confirmed the accuracy of this timer. This is because the type of the crystal oscillator use by the digital wristwatch is what was used for the design. Also, digital wrist watches use CMOS technology as used in the construction of this timer.

On completion of the construction, it was expected that the clock generator when excited should generates clock pulses using quartz crystal, whose operating frequency is 32.768kΩ. The down counters produced counts from 9959 to 0000 through the decoder/driver, which was displayed on the seven-segment display unit. The relay switched off the bulb at the end of a set input count down to 0000 of the timer.

Since the aims of this design were achieved, therefore, the design, research, and construction are successful.

CHAPTER FOUR

RECOMMENDATIONS AND CONCLUSION

4.1 RECOMMENDATIONS

Though the aims of this project work have been successfully achieved to some extent, however, there were some technical difficulties encountered during the construction. These problems include:

(i) Some of the components used were not readily available e.g problem of getting common cathode display on time delayed the construction a little bit.

(ii) Some of the ICs used did not function well as expected which led to their removal and they were replaced with some better ones e.g one of the 40293 was bad and as a result it led to error but was later changed with a better one.

(iii) There was short circuit during the construction.

As already mentioned, these problems encountered were eventually overcome and this made the construction to be a success.

Therefore, it is my view that the practical curriculum of the department be reviewed in such a way that more current and relevant areas of practical electronics be improve upon.

4.2 CONCLUSION

The design and construction of the programmable timer was quite eventful. By the fact that the project works to desired specification and projection, I believe and hope that the circuit would be appreciated and fully utilized by the target domestic and industrial concern where it is applicable with slight modifications to suit their individual desire.

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