DESIGN AND CONSTRUCTION OF AN AUTOMATIC CHANGE-OVERSWITCH USING SEQUENTIAL LOGIC AND CONTROL SYSTEM.

BY.

AKINTOLA, ANTHONY OLUFEMI.

93/3521.

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

BEING A FINAL YEAR PROJECT SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF

BACHELOR OF ENGINEERING

[B. ENG.].

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, FEDERAL UNIVESITY OF TECHNOLOGY, MINNA

MARCH, 2000.

1998/99 Session

DECLARATION

I sincerely declare that this project work was completely carried out by me under the Supervision of Engr (Dr) Y. A ADEDIRAN (H O D) of Electrical and Computer Engineering Department, Federal University of Technology, Minna, Niger State.

24/03/2022.

DATE

AKINTOLA A. O.

CERTIFICATION

I hereby certify that this project titled "THE DESIGN AND CONSTRUCTION OF AN AUTOMATIC-CHANGE OVER SWITCH USING SEQUENTIAL LOGIC AND CONTROL SYSTEM". Was carried out by AKINTOLA ANTHONY OLUFEMI under the supervision of the Department of Electrical and Computer Engineering, Federal University of Technology, Minna, Niger State, in partial fulfillment of the requirements for the award of Bachelor of Engineering (B.Eng.) degree in Electrical and Computer Engineering.

Engr. (Dr) Y. A. ADEDIRAN
SUPERVISOR

.....21/3/2023
SIGN & DATE

Engr. (Dr) Y. A. ADEDIRAN
HEAD OF DEPARTMENT

.....31/3/2023
SIGN & DATE

DR. J.O ONI
EXTERNAL EXAMINER

..... 6/4
SIGN & DATE

DEDICATION

To My Creator, Lord and personal Saviour, Jesus Christ.

To My indispensable parents Mr Francis A. Akintola and Mrs Victoria. A. Akintola.

ACKNOWLEDGEMENT

To God be the glory, great things He has done, He gave the breath that kept me alive, He gave the wisdom, knowledge and understanding that proved me worthy of University education. To him be honour, power and majesty forever and ever. Amen.

I am indebted to my parents Mr Francis A Akintola and Mrs Victoria A. Akintola for their tireless support, encouragement, prayers and provision throughout my academic pursuit. I want you to know that I 'm the fertile seed that you have planted and out of me the God of Heaven in whom I live shall cause you to reap in thirty, sixty- and hundred-fold.

I want to appreciated my senior ones Dr Tunde Akintola and Auntie Nike Akintola for their tremendious financial support, advice and prayers. They have been a source of encouragement to me. Alsc to my junior ones, Miss Bidemi Akintola, Mr Segun Akintola, Miss Bola Akintola and Mr. Folusho Akintola for their constant prayers and love. I want to say a very big thank you to you all.

I am most indebted foremost to my Head of Department and as well my supervisor, Engr (Dr) Y.A. Adediran for his tremendious support and overwhelming encouragement both in guiding and directing me in the course of my project accomplishment.

I want to appreciate brother Toyin Adedokun, a brother I can look up to in difficult times and who has never denied me help when it was in his power to act. I want to say that the God of Heaven shall not forget your Labour of love. Amen.

I shouldn't forget my course-mates, study group members and my friends particularly Akinola Aina, Bamidele Dada, Christopher Umolu, Biodun Oladunjoye, Steve Aboyeji, Mike Olasehinde, Ezekiel, Shola Adesanya, Steve Adunbarin, Bro kunle Ajakaiye and Bro Tunde Okediji for their encouragements.

I'm completely indebted to Miss Ajibola Oluwatimilehin Olanipekun for all her love, prayers, endurance and waiting upon the Lord through out my

academic pursuit, for an expected end being revealed by the Almighty God for the life He has prepared for us to share together.

I love you dearly.

ABSTRACT

The demand for uninterrupted power supply in every organisation is always very high. The incidence of frequent mains failure in Nigeria, which can be inconvenient and costly, led to the idea of automatic change over switch.

The function of this system is to sense the supply mains failure, and initiate the generator solenoid to start the generator and load it whenever there is failure from the mains.

It also senses the restoration of the mains after failure and switching it back to the mains and stopping the generator without the intervention of any operator or skill labour.

In the realisation of the circuit that will perform this function, two logic gates ICs were designed by the use of AND, NOT and NAND logic gates to carry out the logic control of the system. Light emitting diodes (LEDs) of various colours are incorporated to indicate the operation of the various stages.

TABLE OF CONTENTS

PAGE

DECLARATION i

CERTIFICATION ii

DEDICATION iii

ACKNOWLEDGEMENT iv

ABSTRACT vi

TABLE OF CONTENTS vii

CHAPTER ONE

1.0 INTRODUCTION 1

1.1 BRIEF HISTORY OF CHANGE-OVER SWITCH 1

1.2 AIMS AND OBJECTIVES 1

1.3 METHODOLOGY 2

1.3.1 TOP-DOWN HIERARCHY 2

1.4 LITERATURE REVIEW 3

1.4.1 LOGIC GATES 3

1.4.2 INTERGRATED CIRCUITS (ICs) 4

1.4.3 LOGIC FAMILIES 5

1.4.3.1 COMPLEMENTARY METAL OXIDE SEMI CONDUCTOR (CMOS) LOGIC 5

1.4.3.2 TRANSISTOR TRANSISTOR LOGIC (TTL) 6

1.5 PROJECT OUTLINE 7

1.5.1 THE BLOCK DIAGRAM 7

CHAPTER TWO

2.0 SYSTEM DESIGN 8

2.1 PROBLEMS ASSOCIATED WITH THE SYTEM DESIGN 8

2.2 DERIVATION OF THE TRUTH TABLE 8

2.2.1 SIMPLICITY OF THE TRUTH TABLE 9

2.2.2 RELATING THE TRUTH TABLE TO BOOLEAN EXPRESSIONS. 10

2.3 THE OPERATIONAL LOGIC DIAGRAM OF THE SYSTEM DESIGN...12

2.4 DESIGN OF THE LOGIC INTEGRATED CIRCUITS. 12

2.4.1 SELECTION OF THE INTERGRATED CIRCUITS. 13

2.5 THE MAIN CIRCUIT DIAGRAM OF THE SYSTEM DESIGN. 13

2.6 THE DESIGN OF POWER SUPPLY UNIT. 13

CHAPTER THREE

3.0 CONSTRUCTION, TESTING AND RESULTS. 16

3.1 CONSTRUCTION. 16

3.1.1 VERO BOARD. 16

3.1.2 SOLDERING. 16

3.1.3 CASING. 17

3.2 TESTING. 17

3.3 RESULTS. 18

3.3.1 START GENERATOR. 18

3.3.2 LOAD GENERATOR. 18

3.3.3 LOAD NEPA. 19

3.3.4 STOP GENERATOR. 19

CHAPTER FOUR

4.0 CONCLUSION. 20

4.1 RECOMMENDATIONS. 20

4.2 PROBLEMS ENCOUNTERED. 20

REFERENCE. 21

APPENDIX. 23

CHAPTER ONE

INTRODUCTION

1.1 BRIEF HISTORY OF CHANGE –OVER SWITCH

Over the years, the change-over switch has been widely used for both domestic and industrial purpose. Before the introduction of the electro-mechanical device known as change-over switch, there had been other local means of changing the lines from the mains (NEPA) to the generator set whenever there was power failure. This was of course very cheap and simple. As the years went by, the problems associated with this means of changing the lines (the use of wires and sockets to change the line) gave rise to the need for designing of a switch which would be capable of automatically switching the circuit from the mains (NEPA) lines to the generator sets when there is a power failure. The electro mechanical device used for this purpose of moving a circuits from one set of connections to another is called CHANGE-OVER SWITCH.

1.2 AIMS AND OBJECTIVES

The aims and objectives of this project work is to design and construct an electronic device using logic gates sequential control system that is capable of carrying out the following functions.

(i) To sense the failure from the mains

(ii) To initiate the generator solenoid to start the generator

(iii) To load the generator.

(iv) To sense the restoration of the mains after the failure.

(v) To direct the circuit from the generator to the mains (NEPA)again.

(VI) To stop the generator after the mains has been loaded

ADVANTANGES OF AUTOMATIC CHANGE-OVER SWITCH

(i) Create efficiency and reliability

(ii) Time saving operation

(iii) Save damages to both lives and properties

(iv) No human intervention is required

(v) Less costly

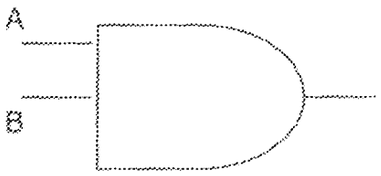
(vi) Portable

1.3.0 METHODOLOGY

This project is a model and is digital in nature.

There are some different logic gates that are being used in the design of the project. Some of these logic gates and their truth tables are given in figure 1.1

AND GATE

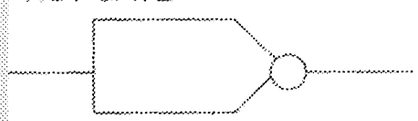


(a)

TRUTH TABLE

INPUT		OUT PUT
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

NOT GATE

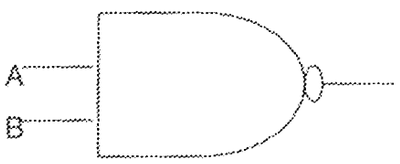


(b)

Truth Table

INPUT	OUTPUT
0	1
1	0

NAND GATE



(c)

Truth Table

INPUT		OUTPUT
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

1.3.1 TOP-DOWN HIERARCHY

The methodology employed for the design of this work is the Top-down hierarchical logic design. This methodology consist of logic levels as illustrated.

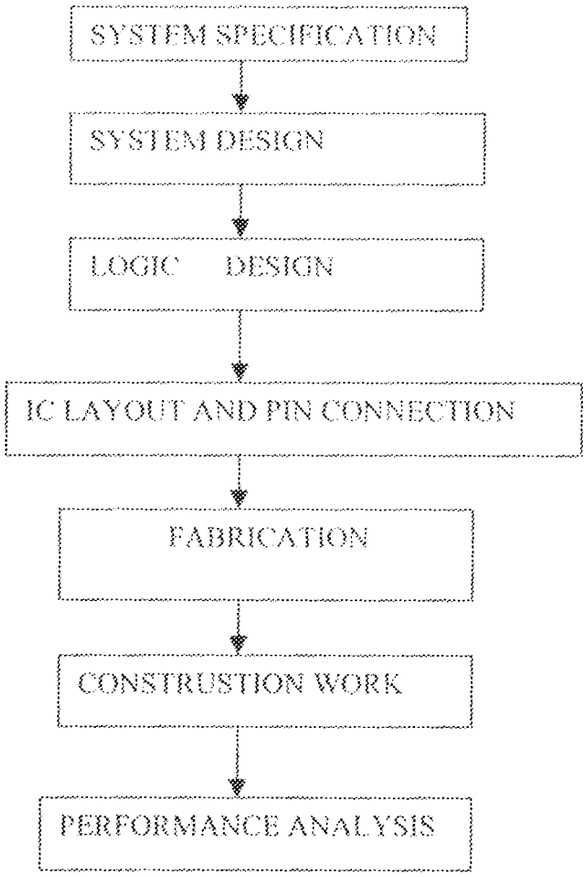


FIG 1.2

Each level is explained in details in the subsequent chapters.

1.4 LITERATURE REVIEW

In order to keep pace with the trend in technological advancements, organisations and industries are tirelessly making efforts to automate their systems to enhance greater efficiency in the performance of their work force, leading to higher productivity.

1.4.1 LOGIC GATES

A logic gate is an electronic circuit which makes logic decisions. It has one output and one or more inputs. The output signal appears only for certain combinations of input signals. Logic gates are the basic building blocks from which most of the digital systems are built up. These logic gates include AND gate, OR gate, NOT gate, NAND gate and the rest.

These circuits called gates are blocks of hard ware that produce a logic-1 or logic-0 output signal if input logic requirements are satisfied.

Note that four different names have been used for the same type of circuits.

(a) Digital circuits

(b) Switching circuits

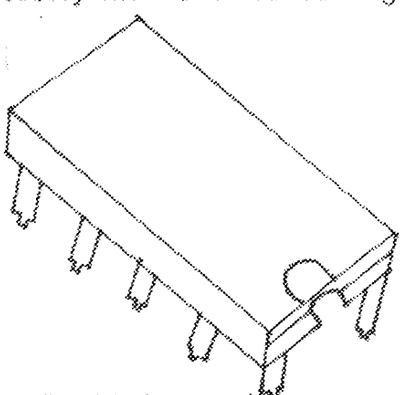
(c) Logic circuits and

(d) Gates

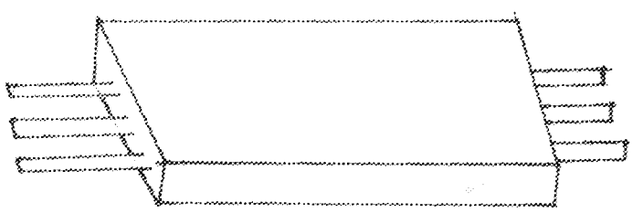
1.4.2 INTERGRATED CIRCUIT (ICS)

Digital circuits are invariably constructed with integrated circuits. An integrated circuit. (abbreviated IC) is a small silicon semi conductor crystal, called a chip, containing electrical components such as transistors, diodes, resistors, and capacitors. The various components are inter-connected inside the chip to form an electronic circuit. The chip is mounted in a metal or plastic package, and connection are welded to external pins to form the IC. Integrated of detachable components in that individual components in the IC cannot be separated or disconnected and the circuit inside the package is accessible only through the external pins.

Integrated circuits come in two types of packages, the flat package and dual-in-line (DIP) package. The dual-in-line package is the most widely used type because of the low price and easy installation on circuit board. The envelope of the IC package is made of plastic or ceramic. Most packages have standard sizes, and the number of pins ranges from 8 to 64. Each IC has a numeric designation printed on the surface of the package for identification. Each vendor publishes a data book or catalogue that provides the necessary information concerning the various products.



(a) Dual-in-line packages



(b) Flat Packages

Fig 1.4 (a and b) integrated circuit packages.

Several logic gates in a single package make it a small-scale integration (SSI) device. To qualify as medium-scale integration (NSI) device, the IC must perform a complete logic function and have a complexity of 10 to 100 gates. A large-scale integration (LSI) device performs a logic function with more than 100 gates. There are also very-large –scale integration (VLSI) devices that contain thousands of gates in a single chip.

1.4.3 LOGIC FAMILIES

Integrated circuit logic families can be divided into broad groups: The bipolar and the Unipolar (which is referred to as the metal oxide semi-conductor (MOS families). Both rely on the switching of transistor between two descrete states in order to represent the logical behaviour of a function. The bipolar families are based on the bipolar transistor whereas the MOS system uses the unipolar field effect transistors as their components.

The IC digital bipolar logic families include the following:

RTL Resistor- Transistor Logic

DTL Diode –Transistor Logic

TTL Transistor –Transistor Logic

ECL Emitter - Coupled Logic

I^2L Integrated Injection Logic.

The IC digital unipolar or MOS logic families include the following:

P - MOS Logic

N - MOS Logic

C - MOS Logic

1.4.3.1 CMOS LOGIC

Complementary metal oxide-conductor logic uses both P and N channels in the same circuits. It is faster than PMOS and NMOS and requires considerably less power than the low power TTL series. CMOS is however still inferior to standard TTL in terms of operating speed. MOS circuits can operate off a wide range of supply voltages. If CMOS

s being used along side with TTL, a 5V supply would be used. However, when used alone, it will operate satisfactory over the range of 3v to 20v.

ADVANTAGES OF CMOS

(i) It is voltage-controlled rather than current controlled

(ii) It has a wider range of voltage for operation. (3v-18v)

DISADVANTAGES OF CMOS

The disadvantages of CMOS ICs are that they do not operates as fast as TTL. And, because they are designed to operate on very minute currents, they are not designed to pass even moderate currents by TTL standards. Thus even static electricity can damage them. For this reason, they must not be handled unless special earthing precautions are taken.

1.4.3.2 TRANSISTOR TRANSISTOR LOGIC (TTL)

The 7400 series of transistor transistor logic (TTL) was introduce by the Texas Instruments in 1964. The principal features of a TTL gate is a multiple emitter input transistor that is functionally equivalent to the input diodes in a DTL circuit.

The TTL logic structure has been continuously developed to meet more stringent speed and power consumption standards some of the available series include the following:

(a) **HIGH SPEED TTL (74 HOO SERIES)** Where the circuitcry is basically the same as the standard TTL but the resistors within the circuits have been reduced in values resulting in faster switching at the expense of increased power consumption.

(b) **LOW POWER TTL (74LOO SERIES) Where** the resistor values have been increased given reduced power consumption at the expense of Larger propagation time.

c) **SCHOTTKY TTL (74SOO SERIES)** Where there is a schottky barrier diodes between the base and collector of every transistor in the gates. It can change state much faster and is the highest speed TTL available.

(d) **LOW POWER SCHOTTKY (74LS00 SERIES)** Where the use of schottky diodes and high resistor values lead to low power consumption, but the reduction in speed is less than in the low power range due to the diode clamps.

1.5 PROJECT OUTLINE

The purpose of this project is to sense the mains failure, and initiate the generator solenoid to start the generator and load it whenever there is failure from the mains. It also senses the restoration of the mains after failure and switching back to the mains and stopping the generator without the intervention of any operator or skills.

In the design, two logic gate ICs were obtained by the use of AND, NOT, and NAND logic gates to carry out the logic control of the system.

The block diagram of the system is shown in the Fig 1.5.

1.5.1 THE BLOCK DIAGRAM OF THE SYSTEM

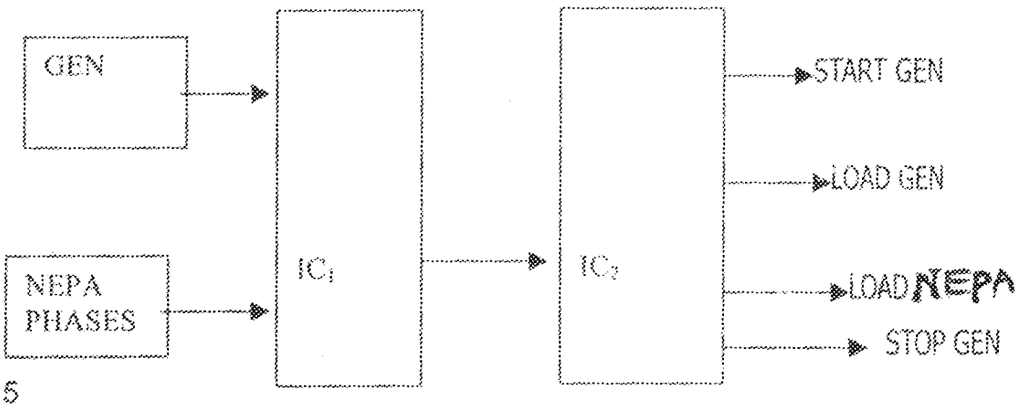


Fig 1.5

CHAPTER TWO

2.0 SYSTEM DESIGN

2.1 PROBLEMS ASSOCIATED WITH THE SYSTEM DESIGN

An immense effort has been put in place over the past years to overcome the disadvantages or short-comings associated with the electro-mechanical type of the change-over switch. And these efforts have however been able to reduce the hazards to the minimum. The problems associated with this types caused damages on properties, slowed production and claimed lives.

Some of the organisations that need steady supply of electricity includes: Hospital, (during major surgical work), medical laboratories and industrial set-up which uses cranes, lifters. Other firms include Radio houses and television houses where they are not expected to be off the air any minute, especially during special broad casting like presidential address.

The design of a combinational logic circuit begins from the verbal statement or outline of the problem and next is a logic circuit diagram or a set of Boolean functions from which the logical diagram can be easily obtained. Some of the practical steps include the following:

(a) The problem is stated or outlined

(b) The number of available input variables and the required output variables are determined

(c) The input and output variables are assigned letter symbols

(d) The truth table that define the required relationships between input and output is defined.

(e) The logic diagram is drawn

2.2 DERIVATION OF THE TRUTH TABLE

The truth table for the combination logic circuit of this system is derived from the already stated problems. It consists of input columns and the output columns. In the

input columns, the three NEPA phases and generator lines are designated by ϕ_1, ϕ_2, ϕ_3 and ϕ_G for phase I, phase II, phase III and the generator.

The 1s and Os in the input column are obtained from 2^4 binary combinations available for the four input variables. The binary values for the output are determined for examination of the stated problems. The output is therefore either START GEN, LOAD GEN, LOAD NEPA OR STOP GEN.

The truth table is however shown in the table given below.

Table 2.1 **TRUTH TABLE OF THE SYSTEM**

INPUT				OUTPUT
ϕ_1,	ϕ_2,	ϕ_3	ϕ_G	
0	0	0	0	START GEN.
0	0	0	1	LOAD GEN.
0	0	1	0	START GEN.
0	0	1	1	LOAD GEN.
0	1	0	0	START GEN.
0	1	0	1	LOAD GEN..
0	1	1	0	START GEN.
0	1	1	1	LOAD GEN.
1	0	0	0	START GEN.
1	0	0	1	LOAD GEN.
1	0	1	0	START GEN.
1	0	1	1	LOAD GEN.
1	1	0	0	START GEN.
1	1	0	1	LOAD GEN.
1	1	1	0	LOAD NEPA
1	1	1	1	STOP GEN.

2.2.1 SIMPLICITY OF THE TRUTH TABLE

From the above truth table, the karnaugh Map is obtained from the various outputs. The Boolean algebraic expression was also written and finally the circuit was minimized using the postulates and theorems of Boolean algebra.

The summary of the output of the circuit from the truth table is

(i) Start Gen

(ii) Load Gen.

(iii) Load NEPA

(iv) Stop Gen.

From the truth table above, the three phases of the mains are assumed to be one input.

Table 2.2 **SUMMARY OF THE TRUTH TABLE.**

NEPA	GENERATOR	OPERATION
0	0	START GENERATOR
0	1	LOAD GENERATOR
1	0	LOAD NEPA
1	1	STOP GENEPATOR

The above table gives the summary of the operations in the truth table.

2.2.2 RELATING THE TRUTH TABLE TO BOOLEAN EXPRESSIONS

From the truth table shown in Table 2.1, the karnaugh Map for the start generator output is shown in the Fig 2.1 below.

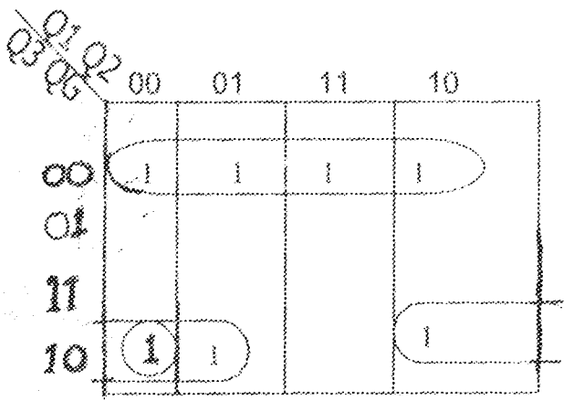


Fig 2.1 Karnaugh Map for the start generator output. The Boolean algebraic expression for the start generator output of the above K-map is obtained as:

$\bar{\phi}_1, \bar{\phi}_2, \bar{\phi}_3\, \bar{\phi}_0 + \bar{\phi}_1, \phi_2, \bar{\phi}_3\, \bar{\phi}_0 + \phi_1, \phi_2, \bar{\phi}_3\, \bar{\phi}_0 + \phi_1, \bar{\phi}_2, \bar{\phi}_3\, \bar{\phi}_0 + \bar{\phi}_1, \bar{\phi}_2, \phi_3\, \bar{\phi}_0 + \bar{\phi}_1, \phi_2, \phi_3\, \bar{\phi}_0 + \phi_1, \bar{\phi}_2, \phi_3\, \bar{\phi}_0.$

Using postulate of Boolean algebra which stated that $(\phi + \overline{\phi}) = 1$.

The above expression can be re-write as follows

$\overline{\phi_1}, \overline{\phi_3}\,\overline{\phi_G}\,(\overline{\phi_2}, + \phi_2) + \phi_1, \overline{\phi_3}\,\overline{\phi_G}\,(\phi_2, + \overline{\phi_2}\,) + \overline{\phi_1}, \phi_2, \overline{\phi_G} + (\overline{\phi_2}, + \phi_2\,) + \phi_1, \overline{\phi_2}, \phi_3\,\overline{\phi_G}$

But $(\overline{\phi_2}, + \phi_2) = 1$

Therefore, $\overline{\phi_1}, \overline{\phi_2}, \overline{\phi_G}\,.1 + \phi_1, \overline{\phi_3}, \overline{\phi_G}\,.1 + \overline{\phi_1}, \phi_3, \overline{\phi_G}\,.1 + \phi_1, \overline{\phi_2}, \phi_3\,\overline{\phi_G}$ = Start Gen.

After further steps of minimization, we now have $\overline{\phi_3}, \overline{\phi_G}\,(\overline{\phi_1}, + \phi_1) + \overline{\phi_1}, \phi_3, \overline{\phi_G} + \phi_1, \overline{\phi_2}, \phi_3\,\overline{\phi_G}$

$\overline{\phi_3}\,\overline{\phi_G} + \overline{\phi_1}, \phi_3\,\overline{\phi_G} + \phi_1, \overline{\phi_2}, \phi_3\,\overline{\phi_G}$ = START GENERATOR

When the logic condition above is satisfied from the logic circuit, the circuit will start the generator automatically. It can be seen that the generator is low for all through the input gates.

From the truth table shown, the Karnaugh Map for the load generator output is shown in fig 2.2

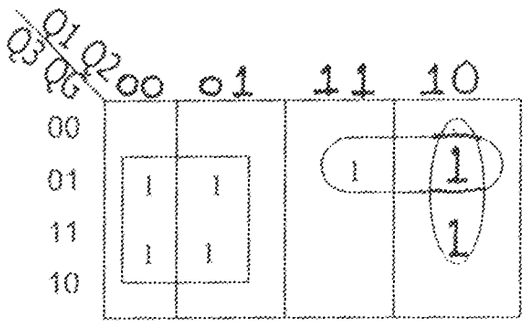


Fig 2.2 K –Map for the load generator output.

The Boolean algebraic expression for the Load generator output of the K-Map above is obtained as shown below.

$\overline{\phi_1}, \overline{\phi_2}, \overline{\phi_3}\,\phi_G + \overline{\phi_1}, \phi_2, \overline{\phi_3}\,\phi_G + \phi_1, \phi_2, \overline{\phi_3}\,\phi_G + \phi_1, \overline{\phi_2}, \overline{\phi_3}\,\phi_G + \overline{\phi_1}, \overline{\phi_2}, \phi_3\,\phi_G + \overline{\phi_1}, \phi_2, \phi_3\,\phi_G$

$+ \phi_1, \overline{\phi_2}, \phi_3\,\phi_G$

minimizing the above equation, we now have $\overline{\phi_1}, \overline{\phi_3}\,\phi_G\,(\overline{\phi_2}, + \phi_2,) + \phi_1, \overline{\phi_3}\,\phi_G\,(\phi_2, + \overline{\phi_2},) + \overline{\phi_1}\,\phi_3\,\phi_G + (\overline{\phi_2}, + \phi_2,) + \phi_1, \overline{\phi_2}, \phi_3\,\phi_G$

therefore, $\overline{\phi_1}\;\overline{\phi_3}\,\phi_G + \phi_1\,\overline{\phi_3}\,\phi_G + \overline{\phi_1}\;\phi_3\,\phi_G + \phi_1, \overline{\phi_2}, \phi_3\,\phi_G + \overline{\phi_1}, \overline{\phi_3}\,\phi_G + \phi_1\,\overline{\phi_3}\,\phi_G + \overline{\phi_1}\,\phi_3\,\phi_G + \phi_1\,\overline{\phi_2}, \phi_3\,\phi_G$

$\phi_1\,\phi_G\,(\overline{\phi_3}, + \phi_3) + \phi_1, \overline{\phi_3}\,\phi_G + \phi_1, \overline{\phi_2}, \phi_3\,\phi_G$ but $(\overline{\phi_3} + \phi_3) = 1$

$\overline{\phi}_1, \phi_G + \phi_1, \overline{\phi}_3\, \phi_G + \phi_1, \overline{\phi}_2, \phi_3\, \phi_G$ = Load generator.

When the Boolean expression above is satisfied from the logic circuit, the circuit will load the generator automatically. It can be seen that the generator is high for all through the input gates.

The Boolean algebraic expression for LOAD NEPA and STOP GENERATOR are as shown below as derived from truth table.

LOAD NEPA: $\phi_1, \phi_2, \phi_3\, \overline{\phi}_G$

When this Boolean expression occurred, it means that the generator off and the three phases of the mains are on.

STOP GENERATOR. $\phi_1, \phi_2, \phi_3\, \phi_G$

This instruction is recongnised and executed when the three phases of the mains are ON and the generator is also ON.

2.3 The Operational logic diagram of the system design

In the realization of the circuit thát will perform this function, two logic gate ICs were designed by the use of AND, NOT and NAND logic gates to carry out the logic control of this system.

The operational logic diagram of the system is however drawn based on the derivation of the truth table.

The Fig 2.3 therefore show the operational logic diagram of the system.

2.4 Design of the Logic IC

In realization of the system, all the functional blocks of this circuit are integrated logic circuit or gate expect the power supply unit. The intergrated circuits used for this design came into reality after going through the normal procedure for designing a combinational logic circuits.

2.4.1 Selection of the ICs

From the design; 3 – input positive NAND gate and AND gate are used.

From the logic gate obtained, the selection of ICs can then be made. Three – input NAND gate exists commercially as QUAD 3 – input NAND gate e.g SN 7410(JN) for CMOS version and as SN 74LS10 (JN) for TTL version.

Similarly, there are 2 – input positive AND gate named SN7408 (JN) for CMOS version and as SN 74LS08 (JN) for TTL version.

The internal pin arrangement for these integrated circuits (ICs) are shown in Appendix.

2.5 The Main Circuit Diagram of the System Design

After the design of the logic ICs and the selection of the ICs are made, the comprehensive circuit diagram is however drawn.

The circuit diagram is shown in Fig 2.4 which shows the power supply unit of the system, the electrical connections of the circuit and the LEDs indicating the operations at the output.

2.6 The Design of Power Supply UNIT

The three NEPA phases are stepped down through step-down transformers to obtains 6v dc to enable it drive the logic ICs comfortably and the generator set line is also stepped – down to 6v dc. An external 6v dc source is connected to the system to power the ICs.

Hence, four 6v – transformers are selected, so that each of the three NEPA phases has its own step-down transformer and also the generator.

The output voltage of each transformer is filtered using two IN4001 – diodes, a 10Uf 25v capacitor and two 1k ohms – resistors.

In the power supply units, a total of eight diodes, four capacitors and eight resistors were used for the design to filter the output voltage of the transformers which also act as the input to the circuit.

CHAPTER THREE

CONSTRUCTION, TESTING AND RESULTS

3.1 CONSTRUCTION

In this project work, before the components were finally soldered on PCB, or Vero board, the circuit was wired on a bread – board. This stage of the project work is the proto type. The circuit was tested on this board and it was certified to be working before the transfer of components to the Vero board.

The unusual name "bread – board" seems to have arisen from the early practice of building radios an handsome slabs of varnished wood, with tubes, coils, e.t.c and the interconnection wires all fastened to the topside of the board. The practice of testing circuit by trial versions on some sort of jig is still called bread-boarding.

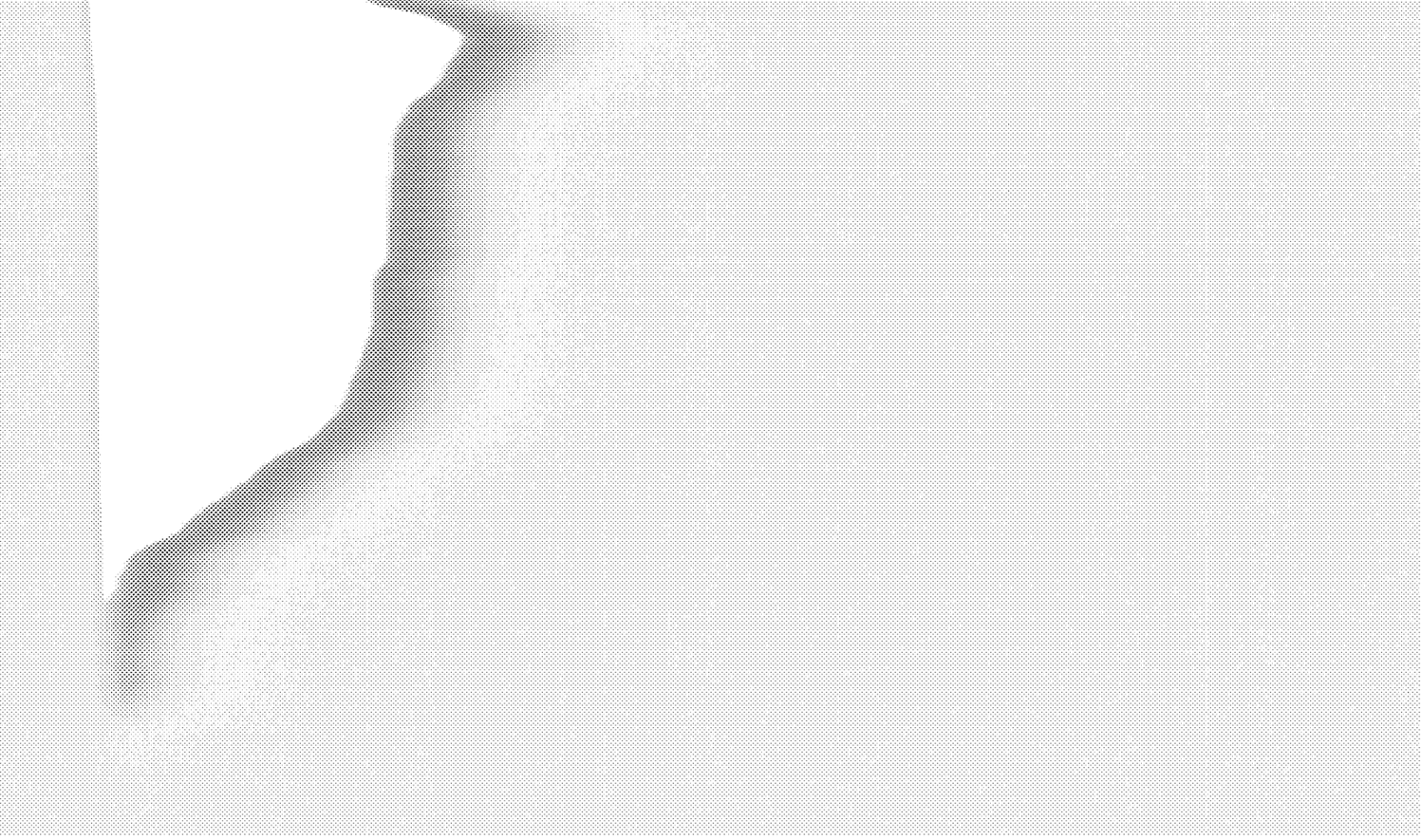
Bread – board can be described as a hardy plastic blocks with rows of holes spaced to accommodate ICs or other components and (usually some extra rows for distributing power supply Voltages). These are intended for testing circuits not for constructing permanent versions.

3.1.1 VERO BOARD

The board which was used for the final wiring of this project work is Vero board which can also be call circuit board. It is the most common kind of board used for the construction of this kind of project work. It is made up of a thermo-setting material with one surface coated with copper material to enhance conducting and easy soldering of the components. It has holes in rows spaced to accommodate ICs or other component as large as possible.

3.1.2 SOLDERING

After positioning of the components on the vero board as provided on the schematic diagram as shown in Fig 2.4. The joining of the legs of the components was made using the soldering Iron of rating 60w/220v and soldering lead. Most of the



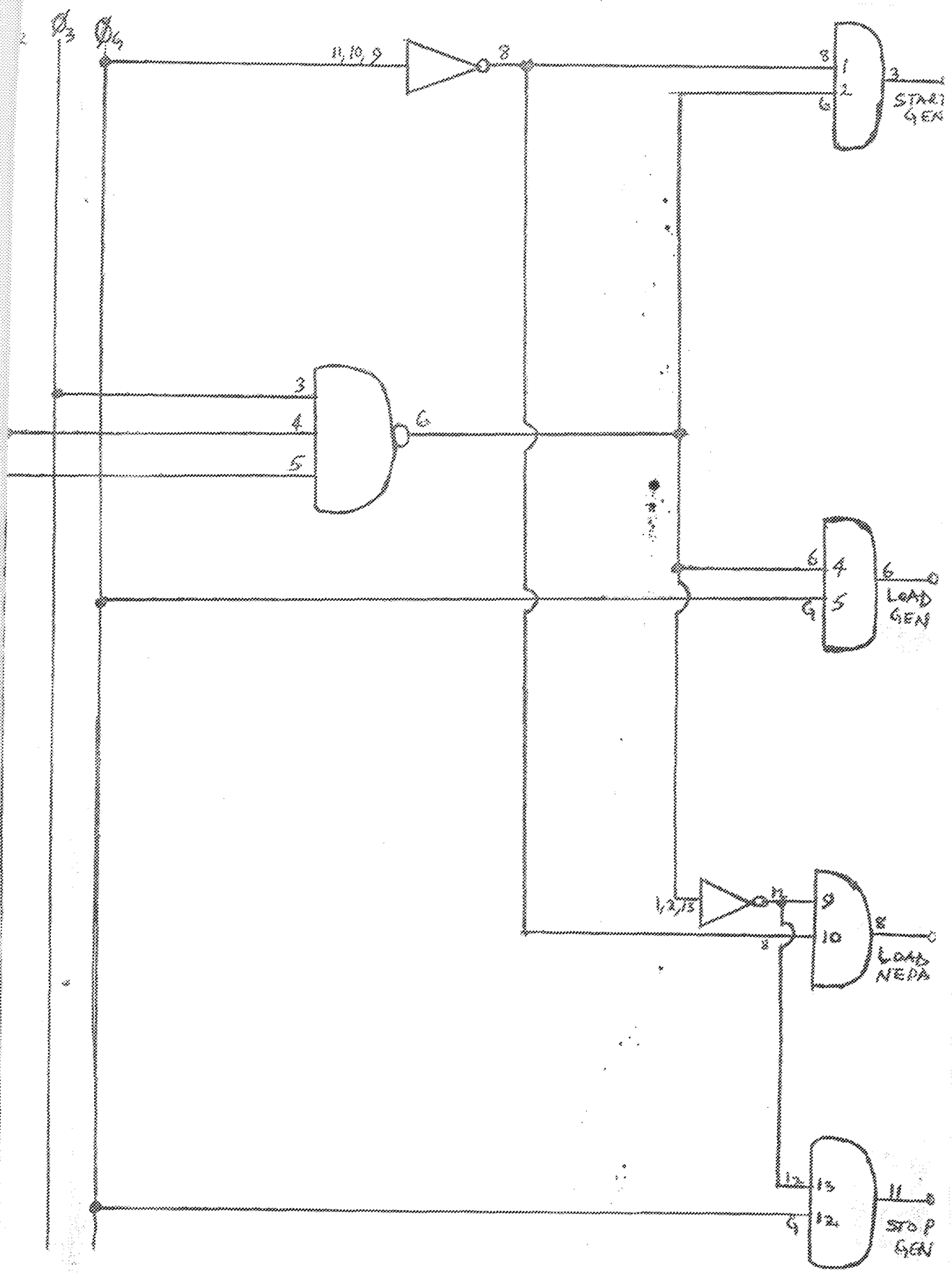
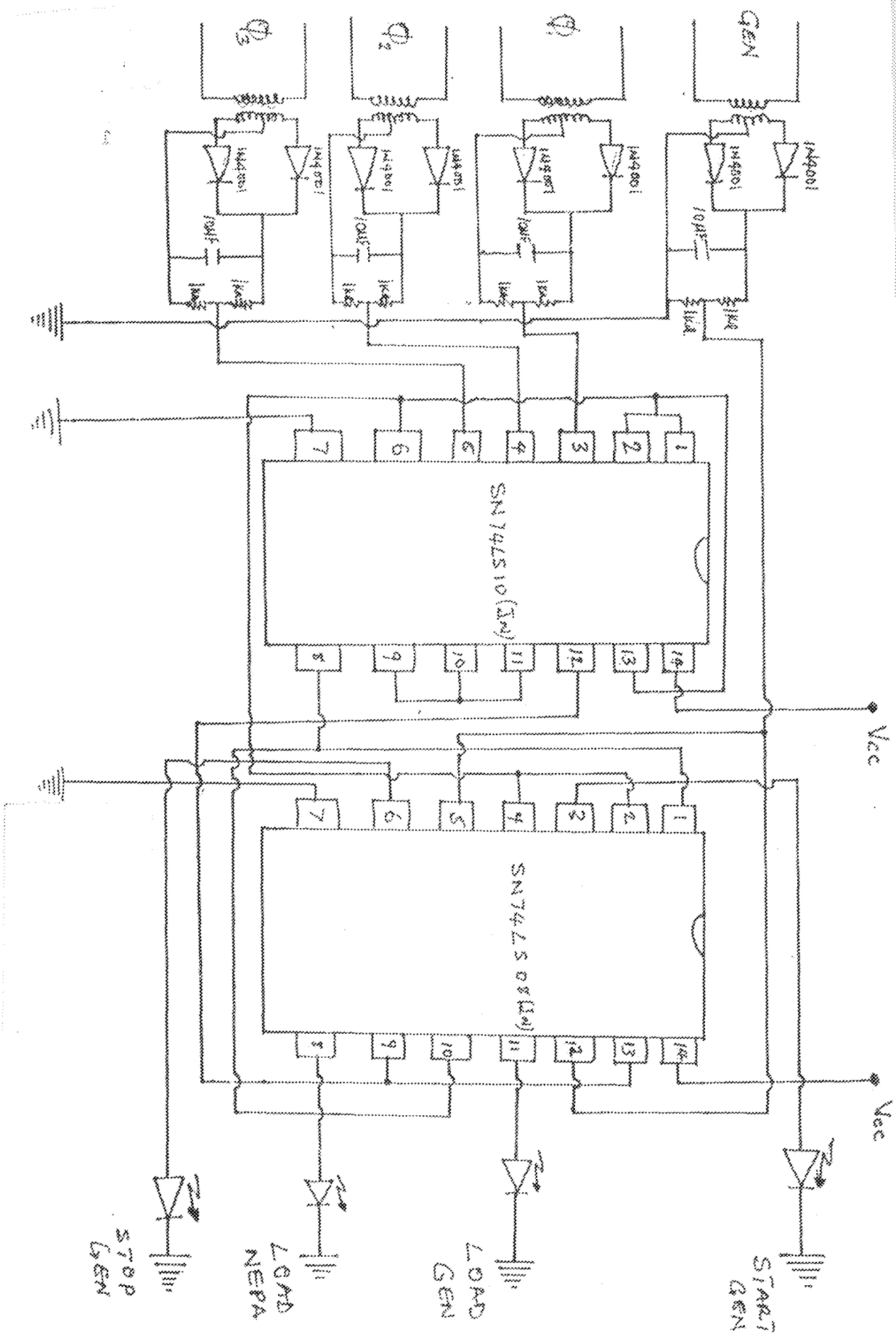


FIG 2.3

work. Some of such circuits include the following: Mains failure sensor circuit, Delay circuit and all these circuits were not incorporated in this work for time and economic reasons (i.e. high cost).

- This project work is therefore open to any student who

FIG 2.4. COMPLETE CIRCUIT DIAGRAM



components are very sensitive to heat and so extra care was taken in soldering to avoid burning of the components. To be on the safer side, it is advisable to use a soldering iron of the rating 25w – 40 w/220v.

3.1.3 CASING

The casing for this project work was effected using a wooden material built into a box shape with the dimension of 29.5cm by 21.5 cm externally and 27cm by 19cm internally. Openings were provided on the casing as shown in the figure below for the purpose of ventilation, power indicator lamp and the rest of the output LEDs.

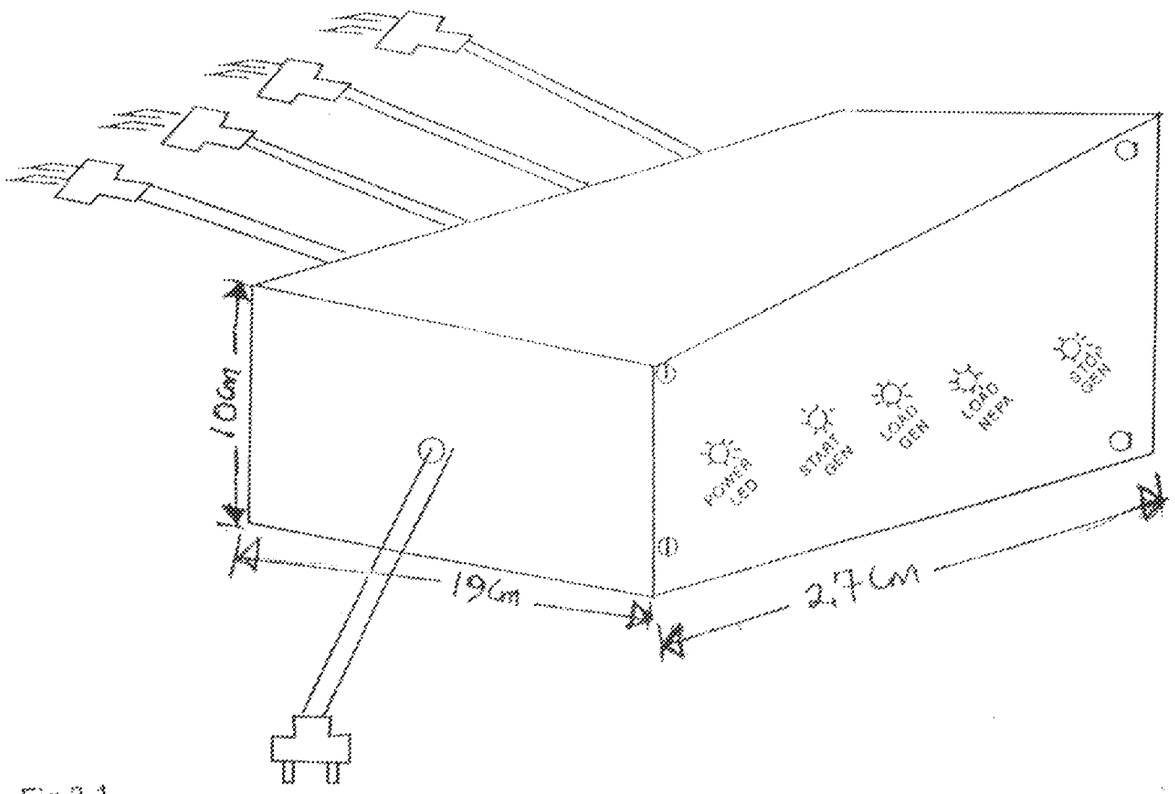


Fig 3.1

3.2 TESTING

The principle of operation of this change-over switch can best be understood using the basic principle of AND and NAND gate truth tabie. The reason being that the circuit is purely a logic circuit by design.

For a 3 – input NAND gaie, the output will only be low (0) when all the inputs are high (1). For a 2 – input AND ga.e the output will only be high (1) when all the inputs are high (1). If for any reason, any of the inpuls low (0) the output will be low (0).

Having gotten the basic principle of the AND and NAND gate operation, we can now go ahead to explain the working principle of this logic circuit which is designed using these gates. The operation sequence of this circuit includes the following:

(1) Mains monitoring unit, detecting partial or complete failure of the mains phases and initiating the generator solenoid to start (START GENERATOR)

(2) Loading of the generator after a predetermined period of time for the generator to reach the required revolution (LOAD GENERATOR).

(3) When the mains is restored, the load is immediately transferred to the mains (LOAD NEPA).

(4) When the mains is restored, after a predetermined period of time, the generator solenoid is de-energised and will shut – down the generator i.e (STOP GENERATOR)

3.3 RESULTS

3.3.1 START GENRATOR

When the 3 – input (i.e 3 – phases of the mains) of the NAND gate of IC_1, are present, the output of the gate at pin 6 will be low (0) thereby the generator will not be started or initiated but the NEPA will still be loaded.

As soon as one of the NEPA (mains) phases fails or all the phases fail, then the output of the NAND gate at pin 6 of the IC_1, will come high (1), and since the low (0) output of the generator, is inverted, it will become high (1). Consequently, the two inputs of the AND gate of the IC_2 will be high and it will now energise the solenoid of the generator to start the generator.

3.3.2 LOAD GENERATOR

As the generator is started, it will be allowed to run for about 10 –25 microseconds to enable the generator attain maximum revolution before loading the generator as predetermined by the time delay circuit attached to the output of the START GEN – with the output of the generator high (1) and the output of the NAND gate in IC_1, i.e pin 6 is

high (1) because either one of the inputs or all the phases low (0), the output becomes high (1). This makes the two inputs to the AND gate of IC_2 i.e pin 4 and pin5 become high (1) and invariable, the output of that gate at pin 6 of the IC_2 will be high (1) and it will load the generator. Note, these operations are carried out within a couple of microseconds depending on the predetermined time set.

3.3.3 LOAD NEPA

Immediately the 3 – phases of the mains (i.e the 3 – inputs of the NAND gate in IC_1) are restored, the output of the gate at pin 6 of the IC_1 will go low (0). Remember that the condition for an AND gate to be high (1), is for the two inputs to be high (1), so load generator will go off because one of the input is low (0). The output of the NAND gate of IC_1, will be low (0) as a result of the restoration of the 3 – phases of the mains. The low (0) output of this pin 6 is now inverted using an inverter, this makes the signal high (1). The low (0) output of the generator which feeds pin 10 of the AND gate is equally inverted by an inverter which now makes the input signals at pin9 and pin 10 are high (1), then the output of the AND gate which is pin II of the IC_2 will be high (1) and then LOAD NEPA.

3.3.4 STOP GENERATOR

The operation of the stop generator comes immediately after the NEPA is been loaded. The two inputs to the AND gate of the IC_2 are: The output of the generator which is high (1) is fed into the pin 12 of the AND gate of the IC_2 and the second is the inverted output of the pin 6 of IC_1 is equally high (1) is fed into the pin 13 of the IC_2. The output of this AND gate is the pin II of the IC_2 which now comes high (1) and de- energises the second solenoid of the generator to cause it shut – down.

CHAPTER FOUR

4.0 CONCLUSION

The output of the system is indicated by Light Emitting Diodes (LEDs) of various colours to show the operation that currently taken place.

The system will start the generator whenever at least one phase from the NEPA mains is off and the generator is also at off state.

It will load the generator after certain seconds the generator has been started and also when at least one phase from the mains is still off.

The system will stop the generator after there is restoration of the mains from NEPA.

Lastly, Load NEPA will be indicated at the output of the system after the generator is completely off and the mains are ON.

The little that was done on this project "Automatic change –qver switch" has actually broadened my practical knowledge of power electronics. It has equally increased my knowledge of trouble shooting using electronic equipments. It gave me an opportunity to carry out research on the automatic control system, which leads to the automation of the industries today.

4.1 RECOMMENDATIONS

The end of the road has not been reached as far as electronics is concerned and as far as modification of this project is concerned.

There are some other circuits that can be incorporated or attached to the outputs of this particular circuit to obtain perfection of the operation of this project work. Some of such circuits include the following: Mains failure sensor circuit, Delay circuit and all these circuits were not incorporated in this work for time and economic reasons (i.e. high cost).

This project work is therefore open to any student who may want to embark on this interesting work, it may interest you to know that the construction of all the circuit

incorporated together is beyond the scope of our level of study. I wish to suggest at this point this could be given as group project.

4.2 PROBLEMS ENCOUNTERED

In the course of my construction especially the first stage of the circuit which is power rectification of the in coming NEPA phases into the IC_1, the phase II developed a problem of not giving the correct voltage at the expected points. This was later discovered to be a break on the vero board and not with any of the components. This problem was rectified by changing the position of the phase II to another part of the board.

Another was the non – availability of some components within my reach which compelled me to travel outside my area for the components and invariably increased the cost of this project.

Finally, time was not enough for the research and the practical tests in the laboratories.

REFERENCES

(1) STRANGIO, C. E "Digital Electronics, Fundamental concepts and applications" Second Edition, prentice Hall of India Private Ltd. 1987

(2) MANO, M. M. "Digital Design" Eaglewood cliffs, New Jersey. (1984)

(3) STONHAM, T. J "Digital Logic Techniques principle and practice". Van Nostrand Renhold Co. Limited U. K. 1987.

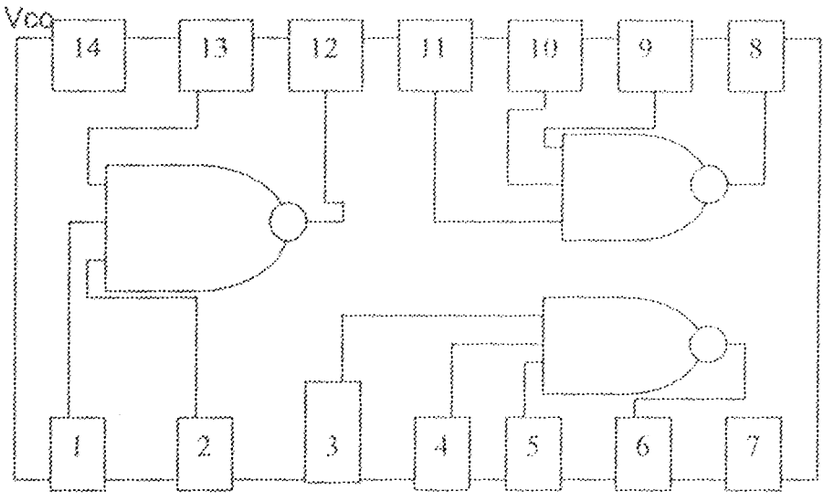
) LAUGHTON, M. A etal. "Electrical Engineering Reference Book". Fourth Edition, Butler–Worth & Co. Publishers Limited. 1985.

HAROWITE, A. O. "The Art of Electronics" Second Edition, Cambridge University press (Great Britain). 1995.

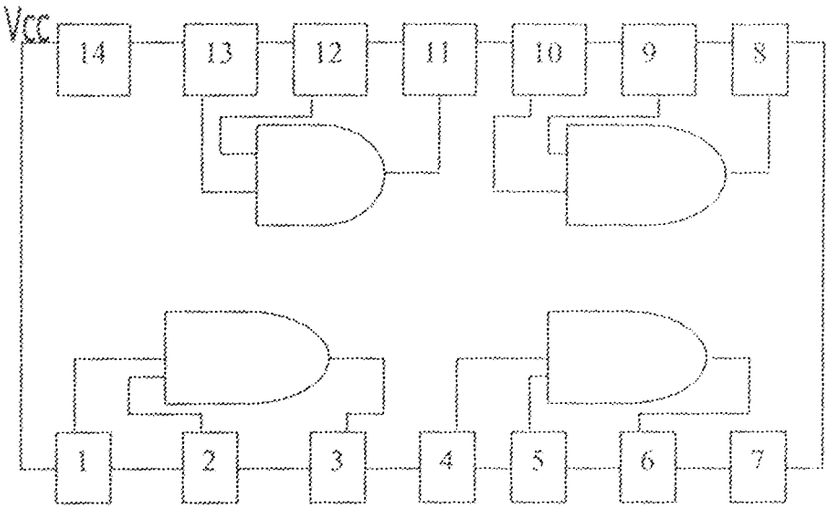
ASA, B. "The Longman Encyclopedia" Longman Group Limited United Kingdom, 1989.

TURNER, L. W. "Electronics Engineers Reference Book" Butter Worth Publishers. Inc. Boston, 1981.

APPENDIX



SN 74LS10 (J, N)



SN 74LS08 (J, N)