DESIGN AND CONSTRUCTION OF SECURITY SYSTEM MONITORING NEPA METER

BY

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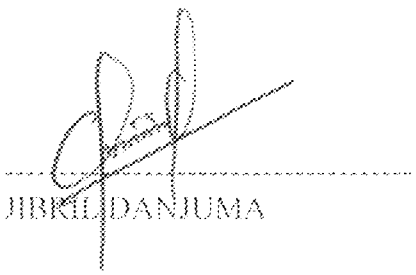
SEPTEMBER, 2003.

DECLARATION

I hereby declare that this project is my original work and is the best of my knowledge, it was never been presented in any form of several of diploma or degree.



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13/10/23

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DECLARATION

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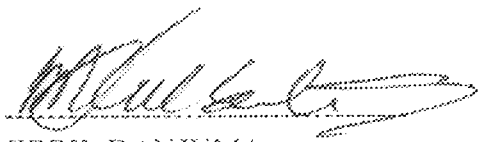

JIBRIL DANJUMA

DATE

CERTIFICATION

This is to certify that this project titled: Design and Construction of Security System Monitoring NEPA Meter was carried by JIBRIL DANJUMA 97/6048EE under the supervision of Engr. Musa Abdullahi and submitted to Electrical and Computer Engineering Department, Federal University of Technology, Minna in partial fulfillment of the requirements for the award of Bachelor of Engineering (B. Eng.) Degree in Electrical and Computer Engineering.

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(HEAD OF DEPARTMENT) DATE

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(EXTERNAL EXAMINER) DATE

DEDICATION

This work is dedicated to my parents, Uncle – Engineer M. M. Princewill, Mr. and Mrs. E. A. Nneli; for their unrelenting Support and encouragement throughout my formative years. I remain forever grateful for their love and support.

ACKNOWLEDGEMENT

This was perhaps the most difficult page to write due to the fact that a number of friends, colleagues and lecturers have been crucial in one way or the other to the successful conclusion of my five years plus career in Federal University of Technology, Minna.

Nevertheless, my heartfelt appreciation goes to my project supervisor Engr. Musa Abdulhahi whose pearls of wisdom and encouragement has been invaluable. I would like to acknowledge my friends and room-mates throughout the years. Firstly, I would like to acknowledge the occupants of Sheraton Block (202), John Saliu, Abel Abenemi, Peter Ikiriko, Uche Okechukwu, Osarobo Otasowie and Seun A. I also salute my friends the family of Ekweme and the family of Ikechukwu.

Also a bulwark of support and companionship in good times and bad are beloved sister Ifeyinwa Nneli (ASUTECH), Ezekiel Ogba (FUT. Owerri), brother Cheyi in Owerri and Pastor (Dr) Abifarin of Mechanical Department, Federal University of Technology, Minna.

To all these people and those I have not mention all I say is thank you! And most of all to God Almighty under whose guidance and protection I have been all through the years.

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ABSTRACT

This project dwell on the comprehensive design and conclusion of a multiplexed security system monitoring NEPA meters for a medium sized residential building as well as industrial and commercial area to monitor mainly NEPA meters located at open places, also can be modified to monitor open/closed status of many access doors. Each meter controls the state of each of switch on LED's that are mounted on a monitoring panel at the security guard's station. Also the basic ideal can be expanded to any number of meters by modifying the system.

A comprehensive and profound insight into the working of the circuit will be appreciated as we go along. The whole system in the basic form consists of (1) Sensors (2) LED's (3) Analogue multiple (4) BCD Counter (5) 555 Timer and Tone siren/alarm (6) Power supply unit.

CHAPTER ONE

1.1 INTRODUCTION

This project dwells on the comprehensive design and construction of a multiplexed security system monitoring NEPA Meters for a medium sized residential building. Although no alarm system is foolproof, they do serve as a warning for most house burglaries. Building may be equipped with detection systems that will transmit an alarm. Some detectors are designed to respond to light and others to darkness. In many junctions, detection systems are required in public buildings, apartment houses and sometimes even in private homes. There are two or more main types of burglary alarm system.

One uses a photoelectric cell. In some of these detectors when a beam of light is obscured or when light falls on a diode it detects it. This is the most effect types of security alarm system and is incorporated with Invisible infra-red beams placed at strategic points around the building. Although this type of system is more difficult to install.

The second is the voltage or current sensing type of alarm system. It is less susceptible to false triggering due to climate changes, extreme variations in temperature and outside electrical interference.

In either case the change set off an alarm. The alarm may sound locally, or it may be designed to alert a central station with notification to the security department. Both types can be run by batteries or by building current.

It is for this very fact that it was decided to incorporate infra-red sensors at very sensitive points. But since NEPA meters are mounted on an open places which will be very difficult for an infra-red sensor to differentiate an intruder from patrolling members/people (or

NEPA official) and also due to cost implications, touch switches and mechanical sensors were used in the design.

In the design of the system, a logical and well reasoned approach using standard MSI and LSI components were used. These components were obtained at bargain prices. For as much as possible, the criteria of reliability first, cost second were adopted. I have also tried as much as possible to realize the overall design keeping the following design objectives in mind.

(i) Does the system work?

(ii) Is it reliable?

(iii) In the concept simple?

(iv) Is it economical?

All these goals must be optimized while keeping cost in mind in order to realize a good design. The only time that these goals were in conflict was in choosing the quality of the components used.

This is because it is certainly false economy to buy a cheaper component if reliability is sacrificed. The design of the whole system was realized using a simple, modular block diagram shown in fig. 1.1.

The integral system in its most basic form consists of:

(i) The sensors (infra-red, mechanical touch-switch etc)

(ii) D-latches and LED's

(iii) Analogue multiplier

(iv) Synchronous up/down counter

(v) Control logic

(vi) BCD-to-7 segment display

(vii) Power amplifier

(viii) Tone generator.

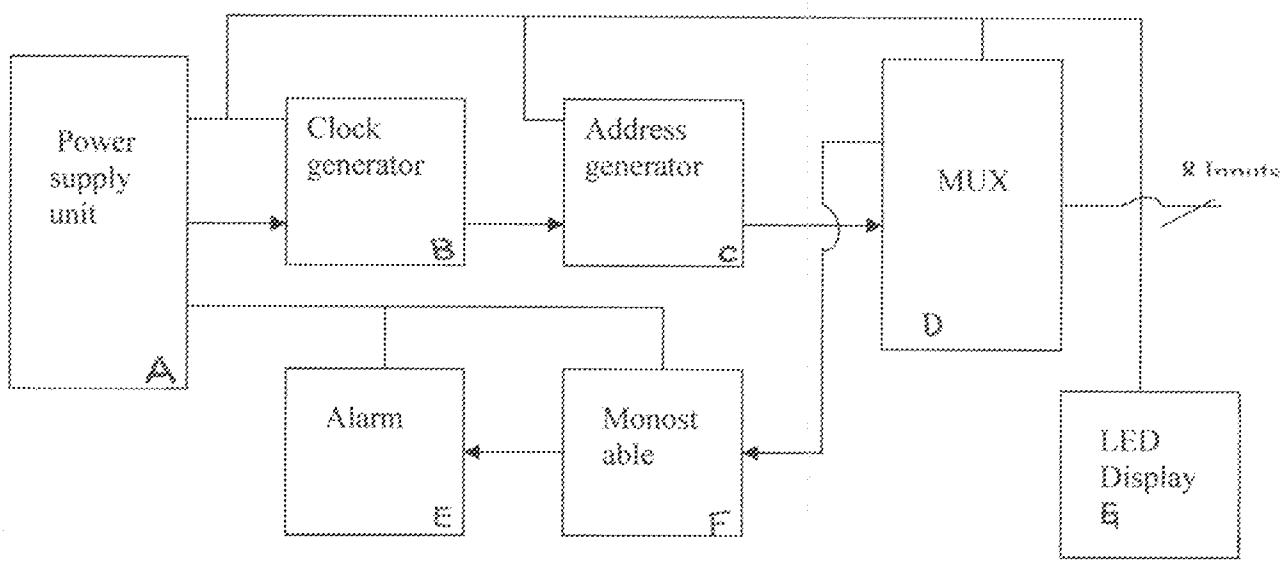


Fig. 1.1: **Block diagram of the project**

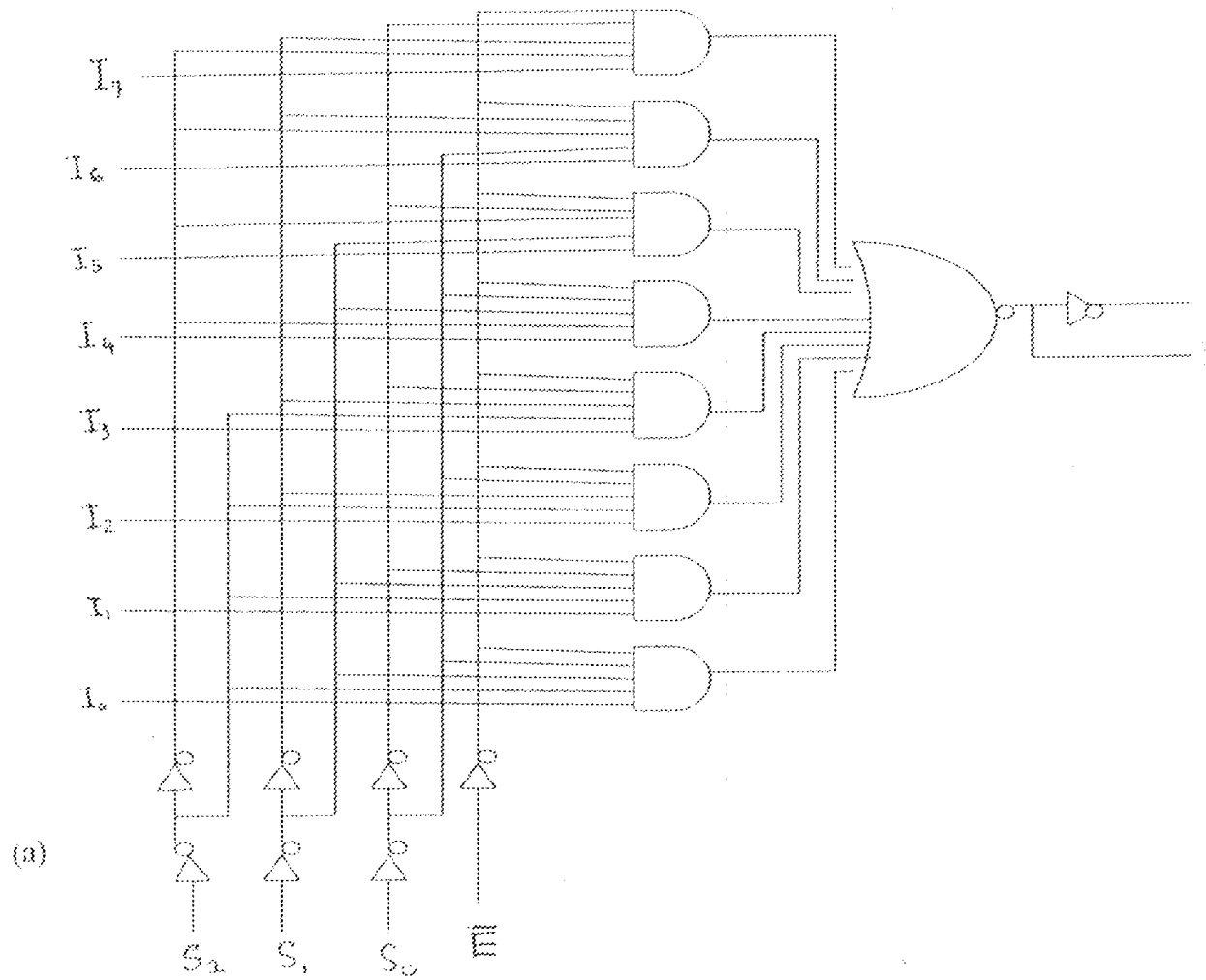
CHAPTER TWO

2.1 MULTIPLEXERS/DEMULTIPLEXERS

A multiplexer or data selector is a logic circuit that except several data inputs allows only one of them at a time to get through to the output. The routing of the desired data input to the output is controlled by SELECT inputs (sometimes referred to as ADDRESS input).The term multiplexing means transmitting other signals on a Single wire by interleaving samples of each while the term demultiplexing means separating the output signal from a multiplexer into signals again.

The question that immediately occurs to the reader is "why go to the trouble of chopping up the signals, sending them down a wire and reconstructing them on the other side of the line?" The answer to this is that multiplexing-demultiplexing reduces the numbers of wires required to send data signals from one point to another.

The multiplexer acts like a digitally controlled juxtaposition switch where the digital code applied to the SELECT inputs controls which data input will be switched to the output. An eight-input multiplexer; for example "selects" one of eight Inputs to appear at the output. A three bit binary code determines which input will appear at the output. Usually, multiplexers also come packaged as quad two-input (42-input multiplexers in one packaged), dual four-input and 16-input (in a large, 24 pin package). The figure below shows the schematic Logic diagram of a multiplexer and its truth table.



(a)

(b)

$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
1	x	x	x	1	0
0	0	0	0	$\overline{I_0}$	I_0
0	0	0	1	$\overline{I_1}$	I_1
0	0	1	0	$\overline{I_2}$	I_2
0	0	1	1	$\overline{I_3}$	I_3
0	1	0	0	$\overline{I_4}$	I_4
0	1	0	1	$\overline{I_5}$	I_5
0	1	1	0	$\overline{I_6}$	I_6
0	1	1	1	$\overline{I_7}$	I_7

Fig. 2.1 (a) Logic diagram; (b) truth table.

For the purpose of this project the CD4051 cmos analogue multiplexer/demultiplexer which is a single 8-channel multiplexer having binary control input A, B and C and an inhibit input.

Generally, this class of analogue multiplexers/demultiplexers is digitally controlled analogue switches which have a low off leakage current.

Control of analogue signals up to 15 volts peak to peak can be achieved by digital signal amplitude of 3 to 15 volts.

For example, if VDD= +5volts, VSS= 0 volts and VEE = -5 volts, analogue signals from –5v to +5v can be controlled by digital inputs of 0 to 5v.

The multiplier circuits dissipate extremely low quiescent power over the logic state of the control signals.

When a logic 1 is present at the inhibit input terminal, all the channels are off. Apart from analogue and digital multiplexing /demultiplexing, other applications of this device are analogue to digital and digital to analogue conversion and signal gating.

It is pertinent to note that the 4051 A multiplexes / Demultiplexer come in a 16 lead or 16 pin dual in line plastic package.

The pin configuration of the integrated circuit is shown in fig. 2.2.

Evidently, from the truth table and the logic diagram one can now ascertain that the 3-bit code [which is often called the address of the input] determines which 8 signals that will be sent onto the output.

Fig. 2.2: Pin Configuration of CD4051A

INPUT STATES				
Inhibit	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

2.2 LED DISPLAYS

A display means an optoelectric device that can show a number ["number display"], or any letter or number 0-9 and a-f ["hexadecimal display"], or any letter or

number ("alphanumeric display"). The dominant display technologies today are LED's and LCD's [Liquid crystal displays].

LCD's are the newer technology with significant advantages for [a] battery operated equipment owing to it's low power dissipation, [b]equipment for use in outdoors or high ambient light levels [c] displays with many digits or characters.

LED's by comparison are some what simpler to use, particularly if you need only a few digits or characters. They also come in three colours and they look good in subdued light, where their good contrast makes them easier to read than LCD displays.

Many numerical displays use a 7- segment configuration to produce the decimal character 0-9 and some times the hex characters A-F. Each segment is made up of a material that emits light when current is passed through it. Most commonly used materials include light emitting diodes [LEDs] and incandescent filaments.

The diagram below shows how an LED can be connected, so that when there is a low, the LED will light. It is important to note that the 220 ohms resistor is necessary to limit the current through the LED to about 15mA (or 0.023A). The common cathode devices and the common anode devices are connected as shown below. To light LED in this type of display, you will apply a logic low signal to its cathode. For the common cathode device, the LED is lit up when a logic high signal is applied to the positive end or anode of the device.

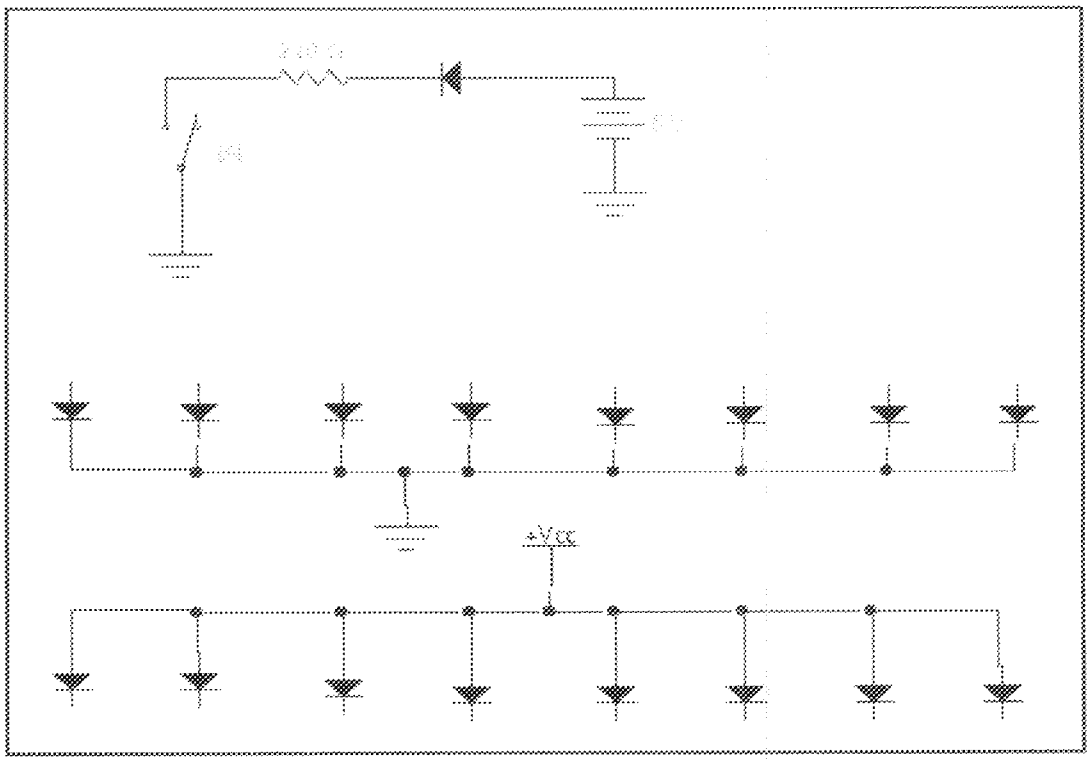


Fig. 2.3. **(a) Common cathode device; (b) common anode device.**

2.3 COUNTERS

In digital logic design, it is well known fact that a counter can be implemented by connecting flip-flops together. Many systems including industrial process systems, data handling systems, and digital computers use counters. Some of the well known applications of counters are

1. Direct counting 2. Divide by N 3. Measurement of frequency 4. Measurement of time. 5. Measurement of distance 6. Measurement of speed 7. Wave form generation and 8. Conversion between digital and analogue information.

A wide variety of counters are available in the market as single chips and some of the crucial factors to look for are:

SIZE: you can obtain BCD (divide by 10) and binary (or hexadecimal divide by 16) counters in the popular 4-bit class. There are larger counters up to 24 bits (not all available as outputs) and there modulo - n counter that divide by an integer n, specified as an input. Counters can always be cascaded to obtain more stages.

a. CLOCKING: It is very important to determine whether the counter is a "ripple" counter or a "synchronous" counter. The synchronous clocks all flip-flops simultaneously, whereas in a ripple counter each stage is clocked by the output of the previous stage. Ripple counters generate transient states since the earlier stages toggle slightly before the later ones. For instance, a ripple counter going from a count of 7(0111) to 8(1000) goes through the stages of 6, 4, and 0 along the way. This doesn't cause in well designed circuits but it would in a circuit that used gates to look for a particular state.
Ripple counters are slower than synchronous counters because of the accumulated propagation delays. Ripple counters clock on negative going edges for easy expandability (by connection the Q output of one counter to the clock input of the next). Synchronous counters clock on the positive edge.

b. UP/DOWN; some counters can count in either direction under control of some inputs. The two possibilities are (a) an Inputs that set the direction of count and (b) a pair of clocking inputs one for up one for down. Some good examples are the SN 74191and SN 74192.

c. LOAD AND CLEAR; most counters have data inputs so that they can be preset to a given count. This is handy when you want to make a modulo-n counter for example. The load function can either be synchronous or asynchronous. Synchronous load means that

the data on the input lines are transferred to the counter coincident with the next clock edge, if the LOAD is asserted independent of the clock.

The term "parallel load" is sometimes used, since all bits are loaded at the same time.

The clear (or RESET) function is a form of Pre-setting. The majority of counters have a Jam-type clear junction though some have Synchronous clear.

e. OTHER SPECIAL FEATURES: Some counters feature latches on the output lines, these are always of the transparent types so the counter can be used if no latch were present (any counter with parallel load inputs can function as a latch, but can't count at the same time as data are held, as you can with a counter /latch. the combination counter plus latch is sometimes very convenient. For example if you want to display or output the previous count before beginning a new cycle of counting.

In frequency counting, this would allow a stable display, with updating after each counting cycle rather than a display that repeatedly gets reset to zero and then count up.

THE BCD COUNTERS 7490 CHIP.

The chip chosen in this project is the 7490 decade counter. The decade counter has 10 distinct states which counts in sequence from 0000 (zero_ through 1001 (decimal 9). To reiterate, any MOD-10 counter, and any decade counter that counts in binary 0000 to 1001 is a BCD counter.

For the purpose of this project MOD-10 counter was configured to count from 000 to 111.

CMOS DESIGN CONSIDERATION

In the design of this circuit two base logic families namely CMOS AND TTL were used. Design and handling recommendations for CMOS, which are included in several data books should be consulted by the designer using this technological, under-listed here are some selected recommendations which illustrate the importance of information.

(1) All unused C-Mos inputs should be tied either to V_{DD} or V_{SS} whichever is appropriate for proper operation of the gate. This rule applies to even inputs of unused gates, not only to protect the inputs from static charge build-up, but to avoid unnecessary supply current drain. Floating gate inputs wall cause all the FET's to be conducting, wasting power and heating the chip unnecessarily.

(2) Cmos input should never be driven when the supply voltage V_{DD} is off, since the damage to the input protecting devices could result. Inputs wired to edge connector should be resistors to V_{DD} or V_{SS} to guard against this possibility.

(3) Slowly changing inputs should be conditioned using Schmitt trigger buffers to avoid oscillations that can arise when a gate passes slowly through the transition region.

(4) WIRED – END configurations cannot be used with Cmos gates, since wiring an output high to an output low would place two FET's in the condition directly across the chip supply.

(5) Capacitive leads greater than 5000PF across Cmos gate outputs act as short circuits and can over heat the output FeT's at higher frequencies.

(6) Designs should be used that avoid the possibility of having low impedance (such as generator outputs) connected to Cmos inputs prior to power up of the Cmos chip. The resulting current surge when V_{DD} is turned on can damage the input.

TTL DESIGN CONSIDERATION

Some of the significant tips to note while using TTL (Transistor-Transistor Logic) chip are:

(1) Power supply, grounding and decoupling

The power supply should be 5u with less than 5% ripple factor and better than 5% regulation.

(2) Unused gates and inputs

If a gate on a package is not used, its inputs should be tied either high or low, whichever results is the least supply current. For example the 7400 draws three times the current with the output low than with the output high, so the inputs of an unused 7400 gate should be grounded. For a 7400 NAND gate, such an input must either be tied high or parallel with a used input. It must be recognized that parallel inputs count as two when determine the fan-out. Inputs that are tied high can be connected either to V_{CC} through a 1K or higher resistance (for protection from supply voltage surges) or to the output of an unused gate whose input will establish a permanent output high. Several inputs share a common protective resistance. Low power Schottky TTL requires no resistance. Since 745XX inputs tolerate up to 15V without breakdown. If inputs of low-power Schottky are connected in parallel and driven as a single input, the switching speed is decreased, in contrast to the situation with other TTL families.

(3) Use of line lengths of up to 10 inches requires no particular precautions, except that no same critical situation lines cannot run code for an appreciable distance without causing cross talk due to capacitive coupling between them for transmission line connections, a gate should drive only one line, and a line should be terminated in only one gate input.

If overshoots gate are a problem, a 25-50ohm resistor should be used in series with the driving gate input and the receiving gate input pulled up to 5V through a 1K resistor. Driving and receiving gates should have their own decoupling capacitors between the V_{CC} and ground pins.

Parallel lines should have a grounded line separating them to avoid cross talk.

(4) Mixing TTL subfamilies

Even synchronous sequential system often has asynchronous features such as reset, preset, load and so on. Mixing high speed 74s TTL with lower speed TTL (74Ls) for example can cause timing problems resulting in anomalous behaviour.

2.4 TIMING CIRCUIT

An external CR network forms the base of most timing arrangements in their IC'S. This simplest circuit is shown in fig. 2 and consists of a changeover switch and a sense resistor connected to the capacitor.

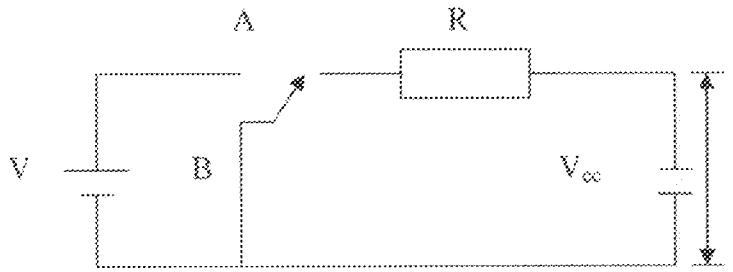


Fig 2.4: **Basic timing circuit**.

If we assume the capacitor is fully discharged with the switch at 'B' and the switch is then moved rapidly to 'A' it can be seen that at this instant.

$V_C = OV$ at $t = 0$ ..... eqn. 2.1

$I_C = V/R$ .....eqn. 2.2

As the capacitor charges, the voltage across the resistor falls and the current at any time t is given by:

$$V_C = V\,(1 - e^{-t/CR}) \qquad \text{---------- eqn. 2.3}$$

Where CR is called the time constants in seconds (C in Farads, R in ohms).

When $t = CR$

$$V_C = 0.632V \qquad \text{---------- eqn. 2.4}$$

In other words, the voltage across the capacitor changes by 63.2% over a period of one time constant and it takes several time constants before the voltage across the capacitor reaches the supply voltage V. Typically this time for the capacitor to fully charge is taken to be about 4 to 5 time constants. If we assume the capacitor is fully charge to voltage V and the switch is then rapidly moved from 'a' to 'b', the capacitor will then discharge V_a R towards zero volts. In this case:

$$V_C = Ve - t/CR$$

Again when T = CR the voltage across the capacitor will hence fallen 63.2% from its initial value V.

Most timing circuits, which naturally require repeatable accurate delays, use changes of voltage across the capacitor of not greater than 60% to 70%, since these points on the charge/discharge characteristics can be more easily defined. For example, in the popular 555 the external timing capacitor charges from 0V to 2/3Vcc to define the timing period in the monostable mode. The principle is illustrated in fig. 2.5 where a comparator has one input tied to a reference voltage set to 2/3Vcc and the capacitor is charged from zero forwards Vcc.

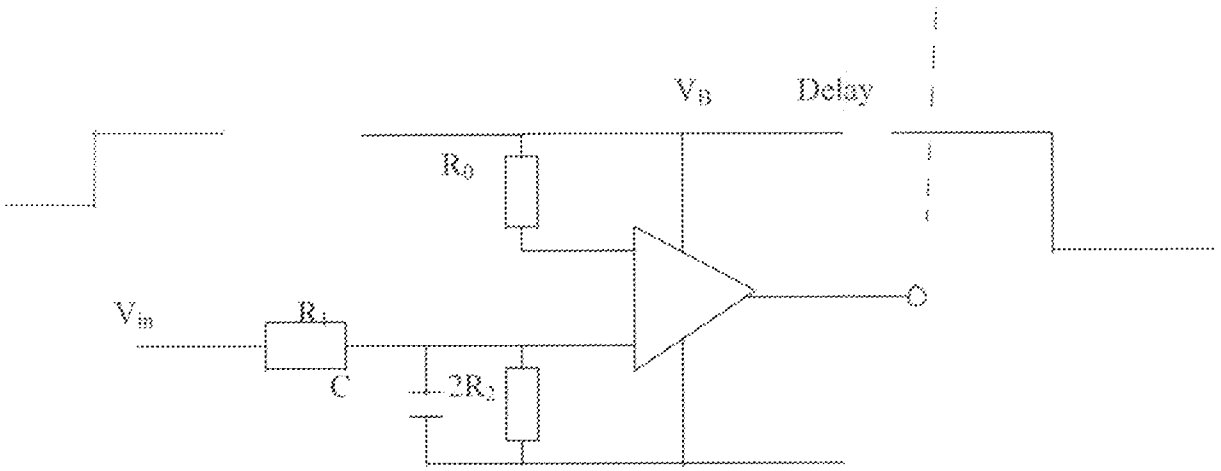


Fig: 2.5.

When the voltage across the capacitor exceeds 2/3Vcc, the output comparators switches sates. The timing period for this, relative to the CR value, can be found using:

$$VC = V\ (1 - e - t/CR)$$

Where in this case, VC = 2/3Vcc and V = Vcc

Therefore $2/3 = 1 - e^{-t/CR}$

$e^{-t/CR} = 1/3$

There t = 1.0986CR

This is usually rounded up as: t = 1.1CR ---------- eqn. 2.5

It is possible to calculate values of time delays for changes of voltage between defined points by using the two values for charge and discharge. This can be done using any ordinary scientific calculator.

If the trip points used to define the timing are derived from the same supply voltage as that charging the capacitor, changes to timing should not be caused by changes to the voltage rails supplying the circuit. It is the CR networks which will primary determine the accuracy and stability of the timing. With standard capacitor the tolerance is

typically ± 10%, whereas resistors of ± 10% tolerance are readily available. This means that it is often the capacitor that is the limiting on accuracy and if accuracy`s of better than ± 3% are required part of the tuning resistance may be made adjustable. Cement trim pots are best for this purpose. Silvered mica or polystyrene capacitors and cement or metal film resistors will prove the best choices for a long term stability and temperature stability of the circuit. Typical temperature coefficients for good quality capacitors are ± 100ppm/^{0}C and for resistor *.100ppm/^{0}C.

Consider an example using 100nf capacitors with a 200KΩ timing resistor.

The time constant CR = 20mins.

The temperature stability is found by adding together the two coefficients.

Therefore timing drift = 150ppm/^{0}C

For a 10^{0}C change in ambient the timing would drift by ± 1500ppm or ± 30μs. it is important to have a well regulated and ripple free supply especially when short term changes occur relative to the timing period. It is always use to have good decoupling at the timer 1C pins to eliminate noise and switching spikes otherwise there will be timing fitter.

TIMER IC'S

The most popular timer IC'S can be grouped under general headings as follows

Medium delay times

Microseconds to minutes: NE555

Dual version in the NE556

Low power versions 1CM

7555 1PA and the linCmos

TLC555

Long time delays

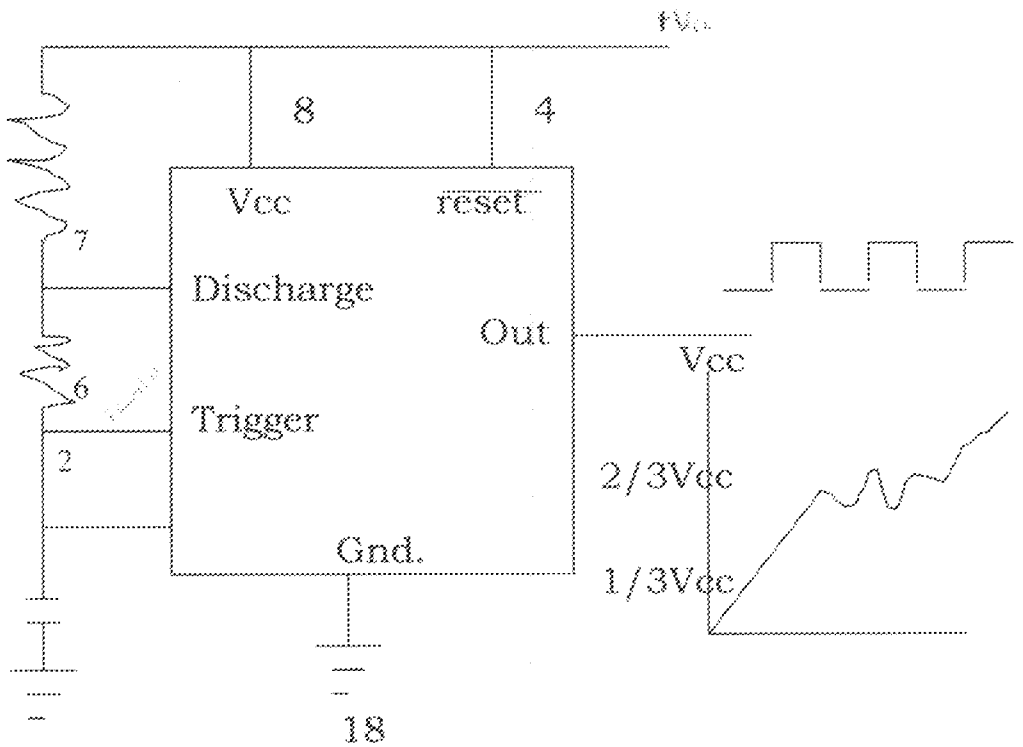
Milliseconds to days: ZN1034

Programmable delays

Microseconds to days: 2240

With these Ics and careful choice of external timing component, it is possible to generate delays, waveforms (square, triangle and saw tooth) with accuracy's of better than ± 0.5%. The classic timer chip is the 555. It is the most popular chip around but also the most misunderstood.

The operation is simple enough. The output gives high (near Vcc) when the 555 receives a trigger inputs and it stays there until the threshold input is driven at which fuse the output gives low (near ground) and the discharge transistor is turned on. The trigger input is activated by an input level below 1/3Vcc and the threshold is activated by an input level above 2/3Vcc. The easiest way to understand the working of the 555 is to look at an example (fig.2.6).



.6. **555** as Oscillator

When the power is applied, the capacitor is discharged, so the 555 is triggered, causing the output to go high, the discharge transistor Q_1 to turn off and the capacitor to begin charging toward 10volts through $R_A + R_B$. When it has reached 2/3Vcc, the threshold input is triggered, causing the output to go low and Q_1 to turn on, discharging C towards ground through R_B. Operation is now cyclic with C's voltage going between 1/3Vcc and 2/3Vcc, with period $T = 0.693 (R_A + 2R_B) C$. The output generally used is the square wave at the output. The 555 makes a respectable oscillator with stability approaching 1% it can run from a single positive supply of 4.5 to 16volts, maintaining good frequency stability with supply voltage variations because the thresholds track the supply fluctuations. The 555 can also be used to generate single pulses of varying width.

It can be deduced from the above diagram:

$$t_{on} = 0.693 (R_A + R_B)C$$

$$t_{off} = 0.693 (R_B C)$$

for a complete period

$$T = t_{on} + t_{off}$$

$$= 0.693 (R_A + 2R_B) C$$

$$f \propto 1/T$$

$$f = \frac{1}{0.693 (R_A + 2R_B) C}$$

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

Figure 2.7 shows a monostable multivibrator circuit made with 555 timer device.

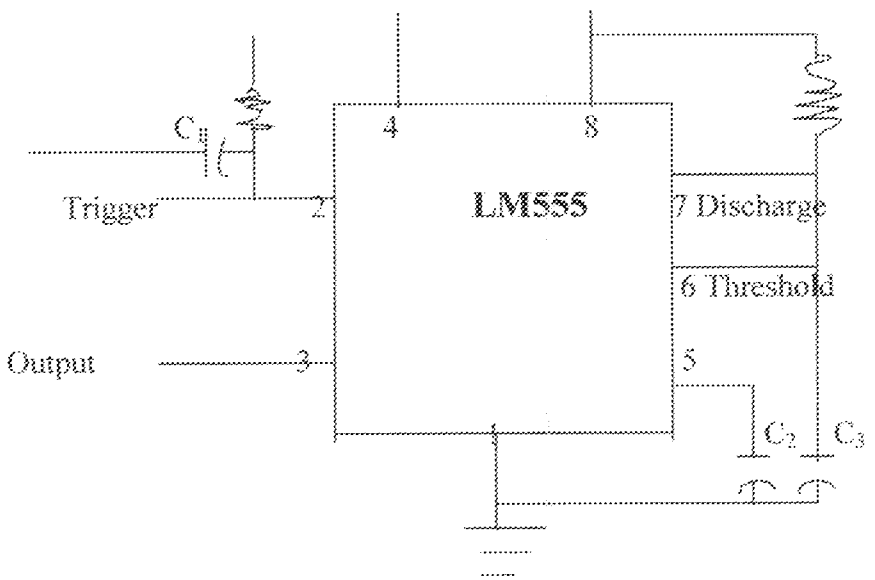


Fig. 2.7; **the 555 timer as a monostable multivibrator.**

The 555 in this circuit is triggered by applying a low-going pulse to its TRIGGER input (pin 2). When triggered, the 555 output (pin 3) will go high for time equal to 1.1RAXC. With a vcc of 5v, RA can have a value from 1kilo ohm to 6.6M ohms. The value of the capacitor can be between 500pf and several microfarads. For best results, low-leakage types of capacitor are used and extreme values of resistors and capacitors are avoided.

The trigger pulse width for a 555 must be shorter than desired time high for the output pulse. If the available trigger pulse is too wide, it can be coupled to the trigger input with a capacitor as shown by the ALTERNATE TRIGGER INPUT. A 555 is inexpensive

and works well for frequencies up to 100KH3 and pulse widths down to about 10 microseconds.

For higher frequencies and shorter-output pulse wilder application, TTL family devices such as the 74121 and the 74LS122 are used.

THE 555 TIMER AS AN ASTABLE MULTIVIBRATOR.

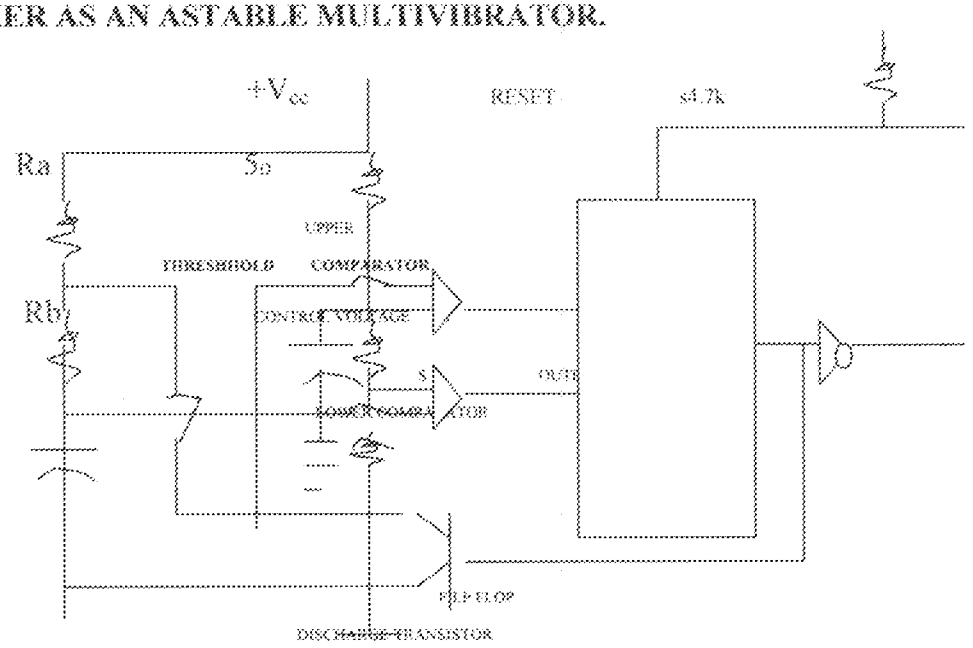


Fig. 2.8; **555 Astable configurations**.

Figure 2.8 shows the internal block diagram and the external components required to cause a 555 to operate as an astable multivibrator. The term multivibrator simply means that the output will continuously "alternate or vibrate" back and forth between a low and a high.

The frequency and duty cycle of the signal output by this astable circuit is determine by the values of resistors, RA and RB and by the value of the capacitor labeled c. The internal voltage divider of three 5-k resistor set a threshold voltage of 1/3 Vcc on the noniverting (+) 2/3 Vcc on the inverting input (-) of the upper comparator. If the voltage applied to the signal input (pin2) of the lower comparative is less than 1/3 Vcc, then the output of the lower comparative will be high. This will set flip- flop. With the

flip-flop in the set condition, the QI output will be low and the discharge transistor will be off. The inverting buffer connected to QI will produce a high on the final output.

If the voltage on the signal input of the upper comparator is greater than 2/3 Vcc, the output of the upper comparator will be high and the flip-flop will be reset. This will cause the discharge transistor to be turned on and the final output on pin3 to be low.

In the circuit in figure 2.8, the comparator input are both connected to the timing capacitor, c. when the power is first turned on, the capacitor has no charge, so the voltage on it is O.V. Since this is less than 1/3 Vcc, the flip-flop will be set, the discharge transistor will be off and the final output will be high. As time passes, the turning capacitor is charged through RA and RB. When the voltage on the capacitor passes 2/3 Vcc, the output of the upper comparator will go high and reset the flip-flop. This will turn on the discharge transistor and make the final output go low.

In the circuit in figure 2.8, the comparator inputs are both connected to the turning capacitor, C. When the power is first turned on, the capacitor has no charge, so the voltage on it is OV. Since this is than 1/3 Vcc, the flip-flop will be set, the discharge transistor will be off and the final output will be high. As time passes, the timing capacitor is charged through RA and RB. When the voltage on the capacitor passes2/3 Vcc, the output of the upper comparator will go high and reset the flip-flop. This will turn on the discharge transistor and makes the final output go low. When the discharge transistor is on it acts like a very low resistance, so the charge on the turning capacitor is drained off to the ground through RB.

When the voltage on the capacitor drops below 1/3 Vcc again, the output of the lower comparator will go high again and set the flip-flop. This will cause the discharge transistor to turn off and the final output to go high again. The circle repeats over and over as the capacitor is alternately charged to 2/3 Vcc and discharge to 1/3 Vcc.

To determine the appropriate resistor and capacitor values for a desired output frequency f, you can use the relationship.

$F = 1.49/ (R_A + R_B) C$

The duty cycle DC of the output waveform is calculated using the formula:

$DC = 9 (R_A+R_B)/ (R_A+2R_B) * 100\%$

Notes on the 555 as an astable:

Do not use a variable resistor for RB because if the variable resistor accidentally gets set at O ohms, the 555 may be destroyed!

The external reset input (pin 4) can be used to gate the circuit on and off. If the external RESET input of a 555 is made low, the output immediately goes low and stays low. When the RESET is made high the circuit starts pulsing again.

The CONTROL VOLTAGE input (pin 5) can be used to vary the output frequency of the circuit. A voltage applied to this will change the comparator threshold voltages.

And thereby change the frequency of oscillation. When operating with a VCC of +5v, the control input voltage can be varied from 1.7v to 5v.

If's the control input pin on a 555 is not used to vary the frequency. Then a 0.01 microfarad capacitor should be connected between pin 5 and around as shown in fig to prevent random noise from modulating the output frequency.

2.6 POWER SUPPLY

A power supply is an electronic circuit designed to provide various AC and DC voltages for equipment operation. A complete power supply circuit can perform these functions:

A. Step-up or step-down, by a transformer action AC line voltage to required voltage.

B. Change the Ac voltage to pulsating DC voltage by either half-wave or full-wave rectification.

C. Filter the pulsating DC voltage to a pure DC voltage for the equipment.

D. Provide some voltage division to meet the equipment needs.

E. Regulate power supply output in the proportion to the applied.

The standard power supply for the TTL circuit is 5v DC, considering other factors it must range between 4.5v and 5.5v DC. The source of power supply used in this circuit system is a 240V0-V ac source.

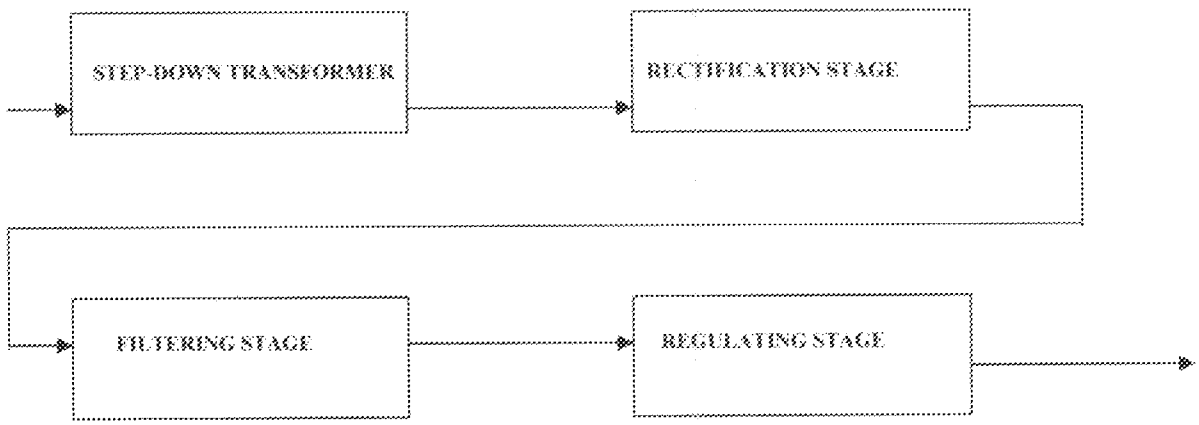


Fig.2.9; **Block diagram for the power supply.**

The advantages of using monolithic regulation are: (1) it is possible to distribute unregulated voltage through electronic equipment and provide regulation locally, for example an individual Vero boards or printed circuit boards. (2) Greater flexibility in voltage levels and regulations for individual stages, and improved isolation and decoupling of these stages.

Monolithic regulators are available that operate in the voltage range from 0-1000v and with external pass elements, the current range extends is 60amps or more. The pinout diagram of the LM 7805 is shown below;

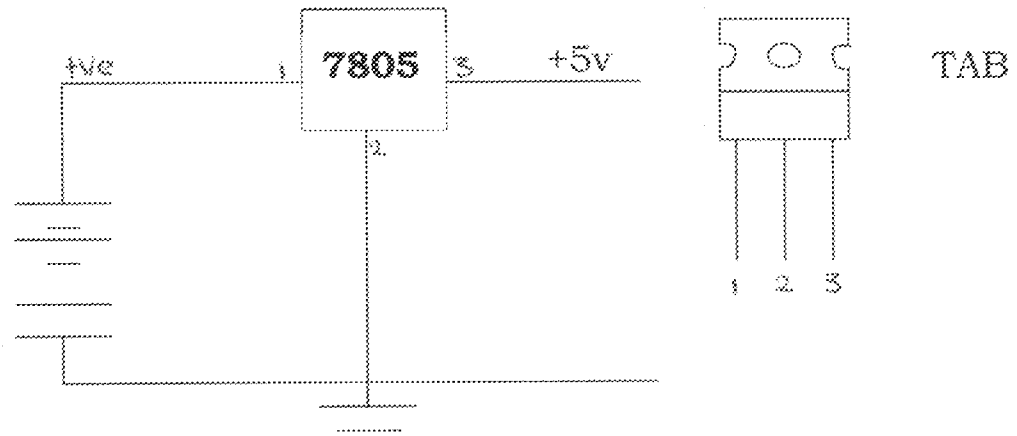


Fig. 2.10

CHAPTER THREE

CONSTRUCTION/ CIRCUIT DESCRIPTION AND TESTING

3.1 CONSTRUCTION/ CIRCUIT DESCRIPTION:

The complete circuit was constructed by breaking it into units, which are as follows;

*Power supply

*Oscillator

*Counter

*Multiplexer

*Display (LEDs)

*Alarm

Voltage Supply

In Fig 1.1, Block A contains the power supply unit. The power supply unit supplies power to all the unit of the system. It receives an ac input voltage (220 volts), and steps it down to 12 Volts using a step-down transformer. This 12V is passed through a rectifier which rectifies ac alternating voltage to dc voltage, and this is regulated to 5V using LM7805. The 5V is supplied to all units of the system.

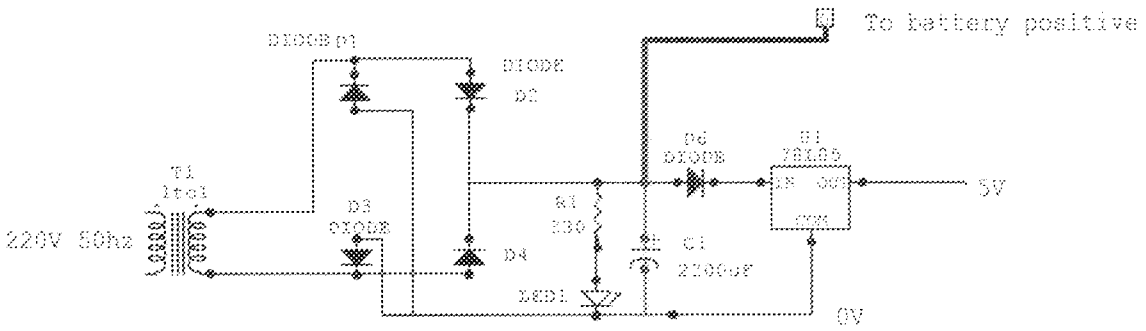


Fig 3.2 The Power Supply Circuit

3.2 CLOCK GENERATOR.

Block B shows a clock generator designed from an astable multivibrator circuit.

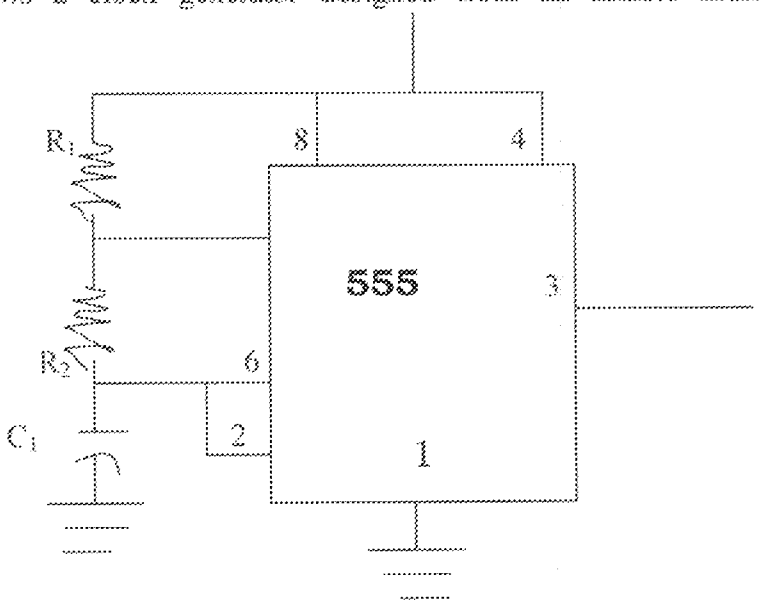


Fig. 3.1 Basic Astable Configuration.

Here pins 2 and 6 are connected so as to enable the circuit trigger itself during each timing cycle. In this configuration the chip functions as an oscillator and generates a square waveform at the output (pin3)

C1 charges through R1 and R2 but discharges through R2. The charge on C1 ranges from 1/3 Vcc to 2/3 Vcc. The oscillator frequency is independent of Vcc.

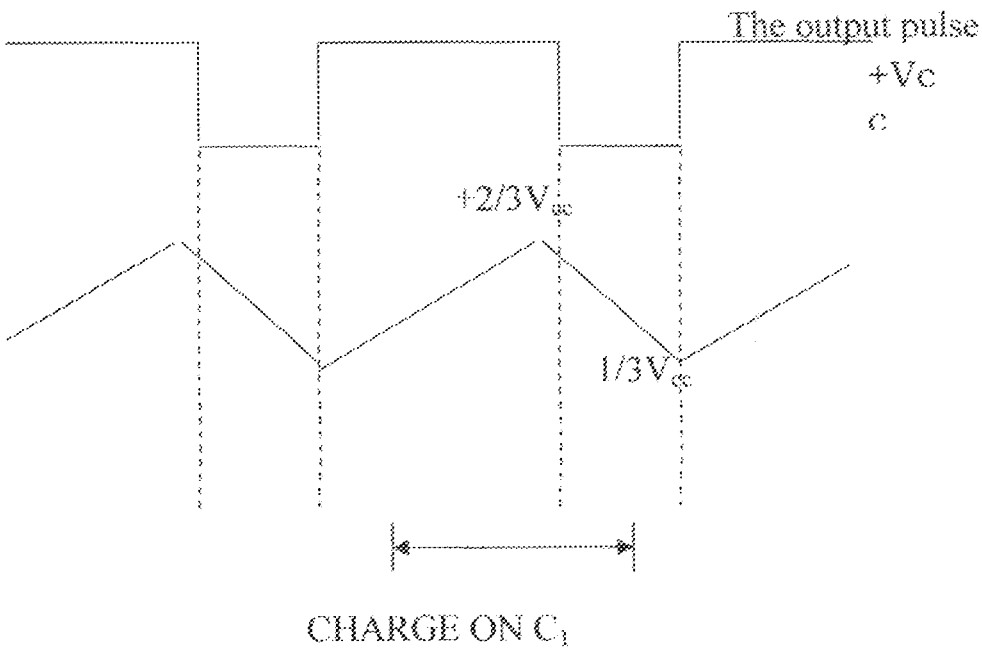


Fig 3.2: Capacitor and Output Waveform for Astable Operation.

By analyzing the equations for charging and discharging, we can derive the following formulae:

The capacitor charges through R = R1 + R2, the charge time constant is (R1 + R2) C.

As the capacitor charges, the threshold voltage increases. Eventually the voltage exceeds +2Vcc/3. Then, the upper comparator sets the flip-flop. With Q high (refer to Chapter 2,

Therefore, discharge time is R_2C. When the capacitor voltage drops to slightly less than Vcc/3 the lower comparator resets the flip-flop.

Thus,

$t_{on} = 0.693 (R1 + R2)C$

$t_{off} = 0.693 R_2C$

For a complete period

$T = t_{on} + t_{off}$

$= 0.693 (R1 + 2R2) C$

Pulse Width = 0.693 (R1 +2R2) C

The reciprocal of the period is the frequency:

$F = 1.44/ (R1 + R2) C$

Dividing the pulse width by the period gives the duty cycle:

$D = R1 + R2 / (R1 + 2R2)$

From our circuit R1 = 1MΩ, R2 = 100kΩ, and C1 = 100uF.

Thus,

$t_{on} = 0.693 (1M + 100k) * 100uF = 0.07623$ seconds

$t_{off} = 0.693*100k*100uF = 6.93 *10^{-3}$ seconds

$T = t_{on} + t_{off} = 0.08316$

$F = 1/T = 12Hz$

$D = (R1 + R2) / (R1 + 2R2) = (1M + 100k) / (1M + 2* 100k) = 0.9167$

This is equivalent to 91.7%

This means that the falling edge of the output pulse occurs 0.9167sec after the trigger arrives. You can think of this 0.9167sec as time delay, because the falling edge of the output pulse can be used to trigger counter.

Block C is basically a BCD decade counter. The BCD counters are MOD-10 counters but as can be observed in the circuit diagram, it is configured to be a MOD-8 counter. Pins 6 and 7 are tied to ground, and the output D (pin11) is tied to the reset terminals (pins 2 and 3). This is to enable the counter to reset after the count of 8.

The output (pin 3) of I.C 1 is fed into the input (pin 14) of I.C.2 of the counter.

The output of the counter i.e. pins 12, 9, and 8 are now used to address the inputs of the analogue multiplexer via the address pins of the multiplexer, i.e. pins 10, 9, and 11, (i.e. B, C, and A). These address inputs determine which input is selected at any instant. Any of the eight inputs is selected and routed to the output one at a time.
With the clock frequency set to be very fast the multiplexer can be made to scan its eight inputs within a second or less, thereby making the signal available at the output.

The output of the multiplexer (pin 3) is fed into a timer circuit designed in a monostable configuration.

3.3 THE ALARM CIRCUIT.

The 555 timer in Block F is configured in monostable mode which receives a trigger at point A shown in Fig. 3.3 in time, the output voltage switches from low to high as shown below.

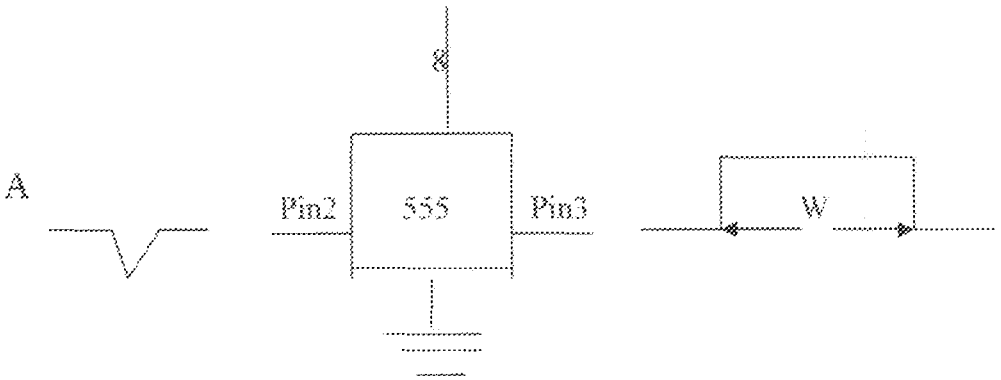


Fig.3.3. 555Timer (as monostable)

The output remains high for a while and then returns to the low state after the time delay W = 1.1RC. The output will remain in the low state until another trigger arrives.

Note that the above Timer is often referred to as one-shot multivibrator because it produces only one output pulse for each input trigger.

By analyzing,

W = 1.1 RC

= 1.1 (10M)(100uF)

= 1100s

= 18.33 minutes

= 0.3hr.

Here we have a pulse width of 0.3 hour. The falling edge of the pulse occurs after a time delay of 0.3 hour. Hence the output pulse (pin 3 of I.C4) is fed into pin4 of I.C5 in an astable mode of operation. These pulses activate the 555 timer (I.C 5) and the circuit will generate a rectangular output while frequency is determined by R1 (1k), R2 (22kΩ), and C1 (0.22uF).

The output from pin 3 drives a loudspeaker through a resistance. The size of this resistance depends on the supply voltage and the impedance of the loudspeaker. The impedance of the branch and the loudspeaker should limit the output current to 200mA or less because this is the maximum current a 555 timer can source.

Since the output pulse that drives the speaker is generated from an astable 555 timer circuit, the alarm sounds continuously until the reset button Rset is used to reset the circuit by pressing it. This reset Rset sends in a low making pin 2 and 3 of I.C4, and pin 4 of I.C5 inactive; assured grounded. The alarm circuit is shown below.

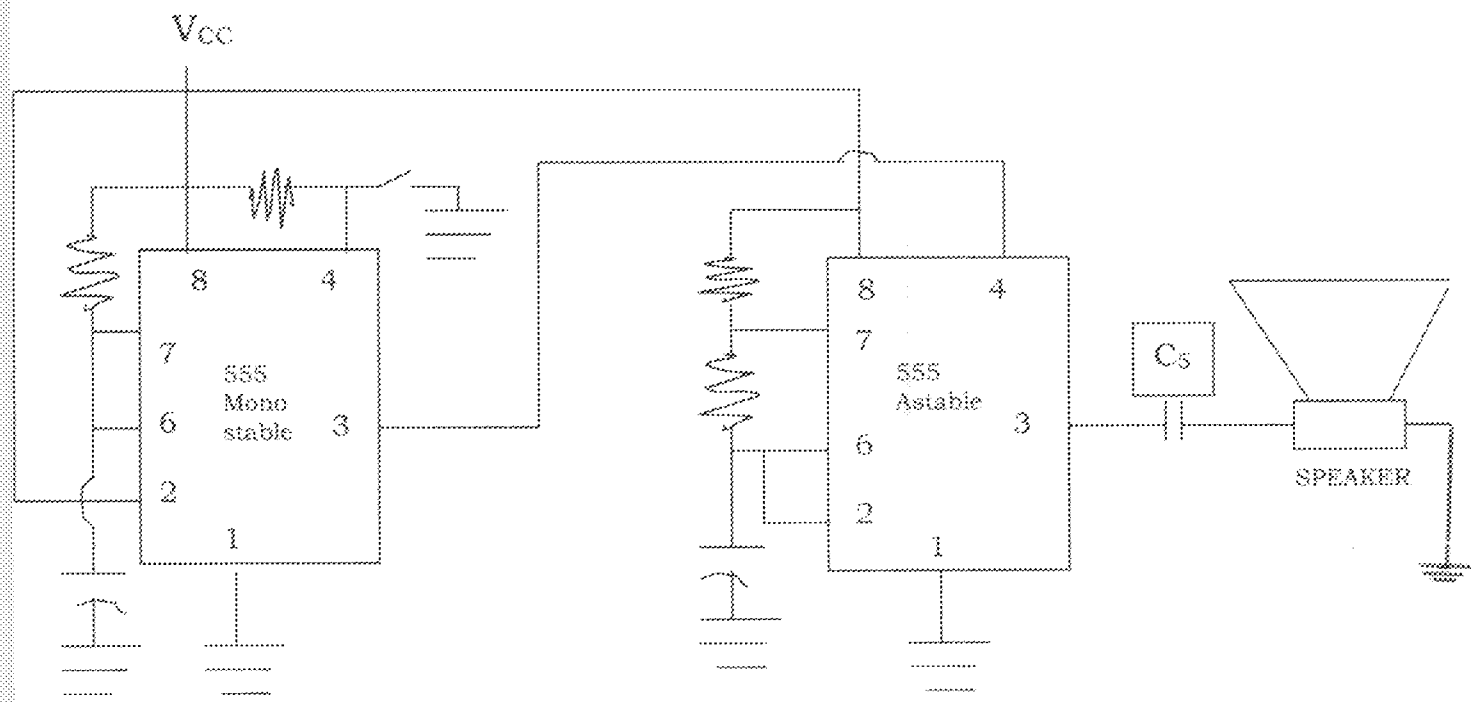


Fig. 3.4: Alarm circuit

CIRCUIT DIAGRAM

CHAPTER FOUR

4.1 MAINTENANCE

Maintainability is a measurement of the accuracy and time required to restore a circuit or system to its normal mode of operation once a failure or abnormal function is detected.

Mainly maintenance covers two general procedures which are corrective and protection maintenance, the first is the repair of failures defects while the second deals with normal or routine checks and servicing of equipment. Certain precautions should be taken in the design of any package to minimize unnecessary maintenance. wherever leads must pass though a hole in a metal chassis or bend around the edge of a bracket a clamp should be used to cause a short circuit.

High ambient temperature within enclosure can eventually cause component to overheat and fail so provision was made for vents and holes in the design to improve cooling within the system.

Enclosures, in addition to allowing circuits to function without overheating must also be tight enough to isolate components and wiring from dust and other contaminants that could accumulate in the circuit and cause failures.

Well designed enclosures minimize maintenance problems through the various types of circuit protection they afford. They can however, present problems in terms of accessibility. Ease of maintenance is directly related to component accessibility. By locating access terminals (e.g. doors) and openings near those components that are most subject to maintenance needs, repair and service can be achieved easily, quickly and accurately.

4.2 TESTING

After realizing the circuit for the first time on bread bound, the various modules were tested stage by stage and found them to be working.

After soldering and packaging the whole unit was tested by activating each of the sensors in turn and watching to see if the alarm would trigger. There was no problem here because the alarm responded to plan.

Furthermore, when there were no intruders, the alarm was quiet.

CHAPTER FIVE

5.0 CONCLUSION

This project is aimed at design and construction of a security system monitoring NAPE METER as well can monitor a medium sized residential building having tested all sages, it can be deduced that the monitoring system can be designed and constructed from the basic principles of multiplexing/demultiplexing and electronic counting/sequencing using counters, this aim has been achieved through with some technical difficulties.

Therefore to a large extend the objectives of the design and construction of a security monitoring system to display an intruder tampering with any of the METER of Doors/Gates, by the use of LED and an alarm circuitry was achieved.

Major problems were encountered in the area of obtaining the pulse frequency using the 555 timer IC which makes the clock to be either slower or faster them desired, components, also being able to find some of the standard LSI component needed in the circuit design in the market.

This situation forced me to use other components which were not all that well suited to do the job required.

All in all the desired objectives was achieved which I had in mind when I started out but since the design I've presented is a prototype, there is a lot of scope for further improvement. Also discovered that the final design is cheaper than most of the system performing equipment tasks in the market, but to be truthful is not of the same quality.

From the test carried out, theoretical calculated at design stage agrees with practical or measured values with few and vary little variation in the range of 10^{-1}.

5.1 RECOMMENDATION

It is recommended on the project that the power supply module incorporated with a charging unit in the power supply so that the battery can be charge whenever it is depleted.

In the same vein, a crystal oscillator is used in place of the 555 multivibrator IC. This is because crystal oscillators are stable and more reliable at accurate pulse generation.

The LED indicator for the display section can be replaced with seven segments display; also LCD display will be the most appropriate display as it has low power consumption.

Finally, depending in consumer requirements, amplifier can be incorporated in design to increase the output power so that the siren/alarm sound is louder.

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