DESIGN, CONSTRUCTION AND TESTING OF A MULTICHANNEL WIRELESS CONTROL SYSTEM

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CERTIFICATION

This is to certify that this project was carried out by **OLAKANMI JOHNSON** of the Department of Electrical and Computer Engineering of the Federal University of Technology under the supervision of **Mr. Eronu**

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Date

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Date

DEDICATION

This project is dedicated to Almighty God, the Supreme of all being.

ACKNOWLEDGEMENT

This project could not have been achievable without the help of Almighty God, my parents and most especially my elder brothers (Engr. Tunde Olakanmi, and Mr. Adepoju Olakanmi) whom through their unrelentive efforts have contributed immensely towards the success of my academic pursuit.

My special thanks also go to my supervisor, Mr. Eronu for all the assistance rendered towards the success of this project.

Special recognition to my project partner Mr. Steve and all my friends like Ogbonna Kelechi, Okzika Nwoke, Atinuke Ajani, Ezeife Kevin, Chika Uzoma, Edozie Ekwuibiri, Emeka (Guru), Adenike Shonubi and others for their friendly construction criticism and advice given towards the achievement of this project.

May God bless abundantly, all those contributed in one way or the other to the success of my academic carrier.

Olakanmi Johnson Osuolale

ABSRACT

The title of this project is "**Design, construction and testing of a multichannel wireless control system**" which can be achieved using the principle of transmission and reception. The project is aimed to design a transmitter as a remote control that can trigger **on** or **off** a system connected to a receiver. It is called a multi-channel because of the ability of the transmitter (remote control) to control more than one output devices connected to the receiver. However, the output devices used in the project are light emitting diodes (LED), whereby one light emitting diode corresponds to one channel. Altogether, there are six light emitting diodes and these correspond to six channels. Each channel been controlled from switches incorporated into the transmitter.

This design is applicable in control system such that a device to be controlled is connected to the receiver.

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CHAPTER ONE

GENERAL INTRODUCTION

DESCRIPTION OF PROJECT

Wireless control system as the name implied uses the principle of "wireless transmission" which can be described as a means of transmitting message (inform of mirowave) via air as the transmitting channel using the transmitting message to control a system.

Wireless transmission , as the basic principle used in this project has made it so possible irrespective of the distance barriers to send information and this is what the project is all about-"**DESIGN,CONSTRUCTION,and TESTING of MULTI-CHANNEL WIRLESS CONTROL SYSTEM**"

The project consists of two main parts, the transmitting part and the receiving part. These two parts also consist of different units carrying out different functions which are fully described in the subsequent chapters. However, given a brief description, the transmitting parts consists of unit that produces frequency whose state of transmission is determined by sequence of binary codes (high or low) generated by the logic units of the transmitting part.

This transmitted signal at the receiving end is processed and regenerate sequence of binary codes which have been used in transmitting the signal from the transmitting part. Subsequently, the regenerated codes are decoded by the logic units of the receiving part which can now be used to control a system connected to the receiving part.

The economic aspect of the project is that, it removes the cost of cables that would have been used in transmitter and receiver interconnection, which might not even be achievable.

The block diagram below shows the illustration of the system.

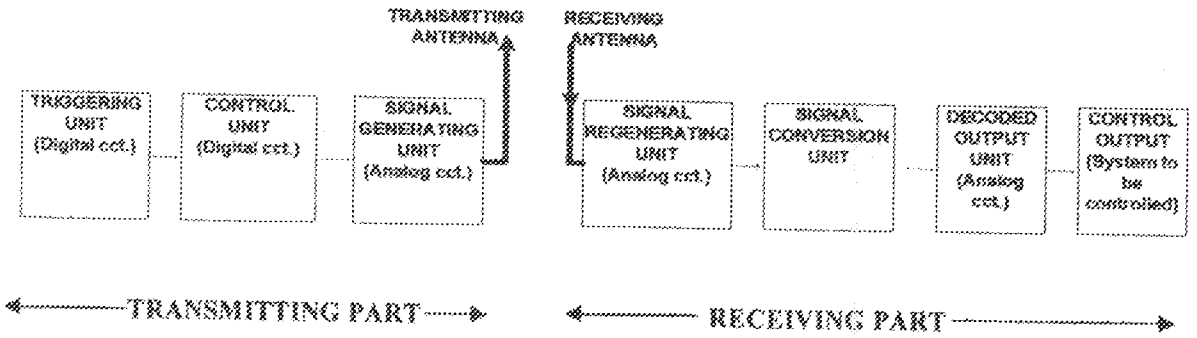


Fig. 1

HOW IT WORKS:

The operation of this system as being carried out in this project is such that the output of the receiver is connected to a system to be controlled.

Let us assume a design of a remote control system (transmitter) that controls a combination of electrical/electronics appliances connected to a point (receiver). This kind of system application can mostly be found in television and some other house electronics control system, whereby the use of remote system controls the operations of all these house electronics.

AIMS AND OBJECTIVES OF THE PROJECT

The aims and of objectives of this project are stated below;

- To eliminate distance barriers that could make transmission of information almost impossible.

- To minimize the bulkiness of cables used in any control system.
- To make system easily controllable irrespective of the distance.

LITERATURE REVIEW

Before the dawn of the digital age, 35 years ago, when analog electronics was still in a commanding lead, the only interference problem of concern involved transmitters and receivers. As the digital age took off in the 1970's, the interference problems began to be diminishing. Furthermore, as clock frequency of digital circuits started to increase in the 1980's and 1990's, the digital circuits became more pronounced. Analog and digital circuits became more applicable such as the one employed in this project.

The wireless nature of this project calls for the need for a transmitter and a receiver which both operate on the basis of electromagnetic wave as a medium for message traveling between the two systems (transmitter and the receiver).

This project has thus employed the researches made by some scientist like James Clerk Maxwell of London University, George F. Fitzgerald, and Hericular Hertz about electromagnetic waves as a radio wave.

Also, some information about digital circuits, electronics and their application were gotten from textbooks, such as Digital fundamental(6th edition) by Floyd, Elements of digital communication by D. Dupontel J.C, Introduction to Electronics by R. A.Sparks,and Wireless communication design by Reinado Perez.

CHAPTER TWO

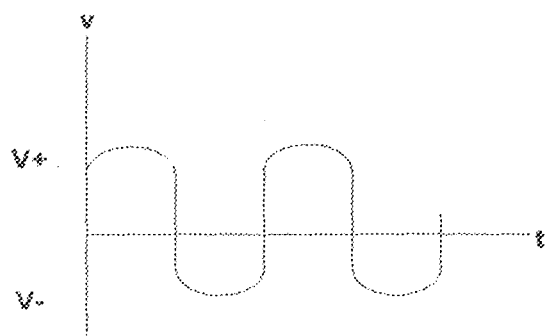
DESIGN AND ANALYSIS OF THE PROJECT

The design of this project basically employs generation of binary codes sequence (high or low), which is then used for transmission of signal from the transmitter to be received by the receiver.

In order to have a clear understanding of the project design, fundamentals of digital systems briefly have to be taken into consideration.

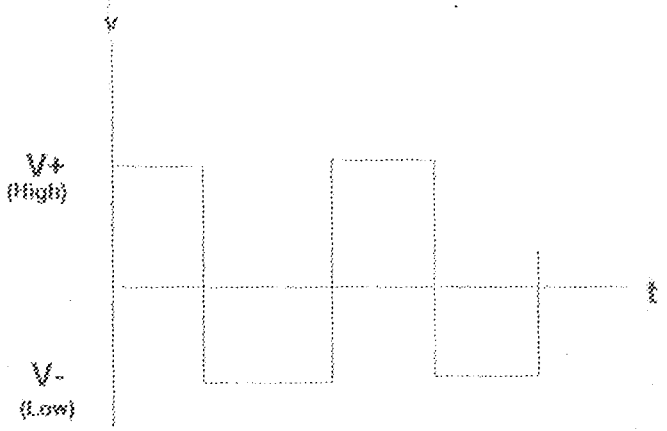
Electrical signal could either be discreet or continuous. When electrical signal is continuous in nature, we say, it is **analog**. However, the signal is said to be **digital** whenever it is discreet.

The graphs below show the waveforms of both analog and digital signal.



Analog representation of Electrical signal

fig.2.0a



Digital representation of Electrical signal

Fig.2.1a

Shown in fig 2.0a and fig 2.1a are the electrical representations of both analog and digital signaling respectively? Considering fig 2.1a, V could take a value of V+ or V- (1 or 0) and that V+ is positive while V- is negative. We may also say that V is "high" or "low" as indicated. As a matter of fact, we can select any two words; assign one word to one voltage level and the other to the second level.

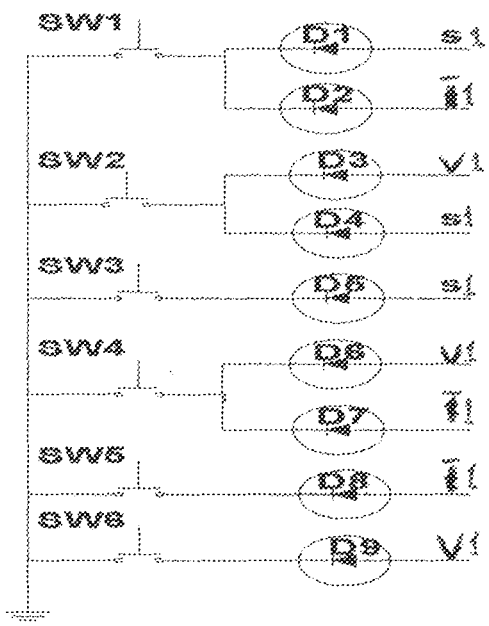
However, in a particular digital system like this project, we may encounter many binary variables which operate between two voltage levels 0v to 9v. In addition to digital system, decimal numbers can be expressed in binary by means of decimal system. For instance, decimal number 6 can be written in binary as 110.Therefore, we can see that when dealing with digital system like this project, we are dealing with binary values of 1s and 0s.

We thus begin our analysis from where the whole system is activated.

THE SWITCHES AND THE POWER DIODES

Activation of the whole system starts from this unit and the unit is composed of push-down buttons and low power diodes as shown below in the circuit diagram.

CIRCUIT DIAGRAM



THE SWITCHING UNIT

Fig.2b

CIRCUIT ANALYSIS

Fig. 2b shows the switching unit which consists of the combination of six push-buttons and nine low power diodes. Activation of the whole system starts from this unit.

The labels **s, t and v** are the output from the power diodes. These are respectively connected to the input of the next unit (inverter unit). The operation of each push-button is similar. However, different buttons operate different output.

For the purpose of better understanding, let us base our analysis on when a switch button (SW1) is pressed. This causes electrical signal to flow from diodes 1 and 2 which subsequently affects what happens to the next unit of the system. The flow of this electrical signal is made to be unidirectional because of the biasing of the diodes.

INVERTER AND REGISTER UNIT

The inverter used in this project is a 4069 IC while the latch is a 40174 IC, a shift D type flip-flop register.

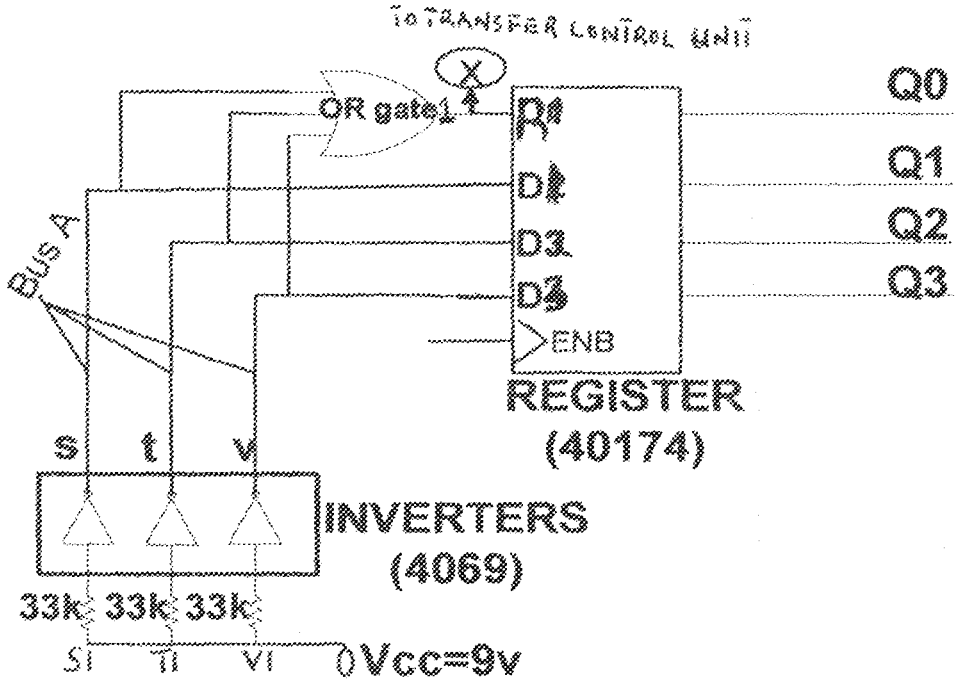
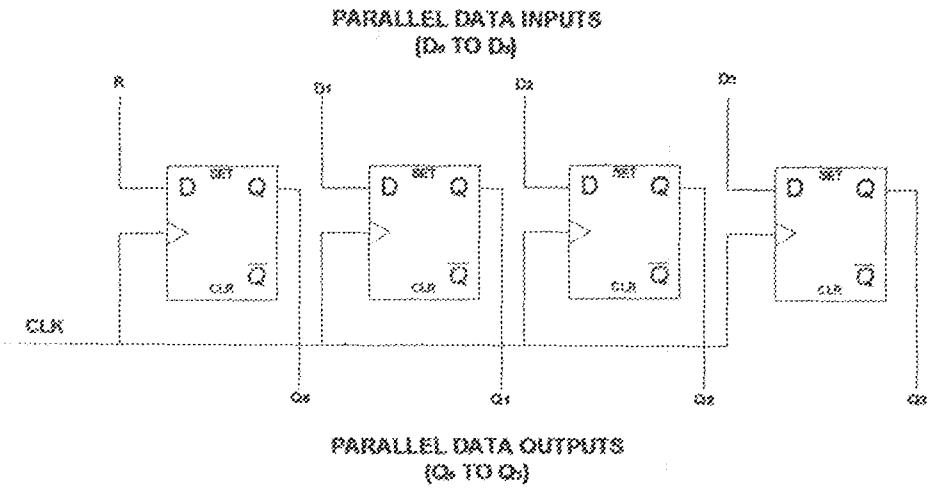


Fig 2c: **INVERTER AND REGISTER UNIT**



INTERNAL DIAGRAM OF THE REGISTER

Fig.2d

OPERATION

Shown in fig 2c is the inverter and the register unit while fig 2d shows the internal diagram of the register (shift register). The input codes into the shift register are simultaneously entered and they are simultaneously available at the output as shown in fig. 2.d (the internal circuit diagram of the register). This type of shift register is known as parallel in/parallel out D type shift register. The name is given because of its ability to receive sequence of binary codes in parallel form and output the same set of codes in parallel form

ANALYSIS

From fig.2c, Vcc= 9v. That is,the input to the inverter at its normal stage is 1.This implies that the three input to the inverter at normal stage will be 111(**S1, T1, and V1**).

However, when button 1 from the switching unit is pressed, signal flows from diode 1 and 2 which in turn goes to the input of the inverter through label **T1, S1**.Button 1 pressed makes **T1** and **S1** become 00 while V1 still remains 1.That is, input to the three

inverter now become 001.The inverters going by their own operation will invert the output codes at data bus A to become 110.

The truth tables below show a better interpretation of input to the inverters before a button is pressed, the input and output of the inverter whenever a button is pressed, and the input and output of the register.

INVERTER

NORMAL STATE

Push-button	s	t	v
SW1	1	1	1
SW2	1	1	1
SW3	1	1	1
SW4	1	1	1
SW5	1	1	1
SW6	1	1	1

Table 2a

OPERATIONAL STATE

	INPUT			OUTPUT		
Push-Button	s	t	v	s	t	v
SW1	0	0	1	1	1	0
SW2	0	1	0	1	0	1
SW3	0	1	1	1	0	0
SW4	1	0	0	0	1	1
SW5	1	0	1	0	1	0
SW6	1	1	0	0	0	1

Table 2b

REGISTER

	INPUT				OUTPUT			
Push-button	R	D1	D2	D3	Q0	Q1	Q2	Q3
SW1	1	1	1	0	1	1	1	0
SW2	1	1	0	1	1	1	0	1
SW3	1	1	0	0	1	0	0	1
SW4	1	0	1	1	1	1	0	0
SW5	1	0	1	0	1	0	1	0
SW6	1	0	0	1	1	0	0	1

Table 2c

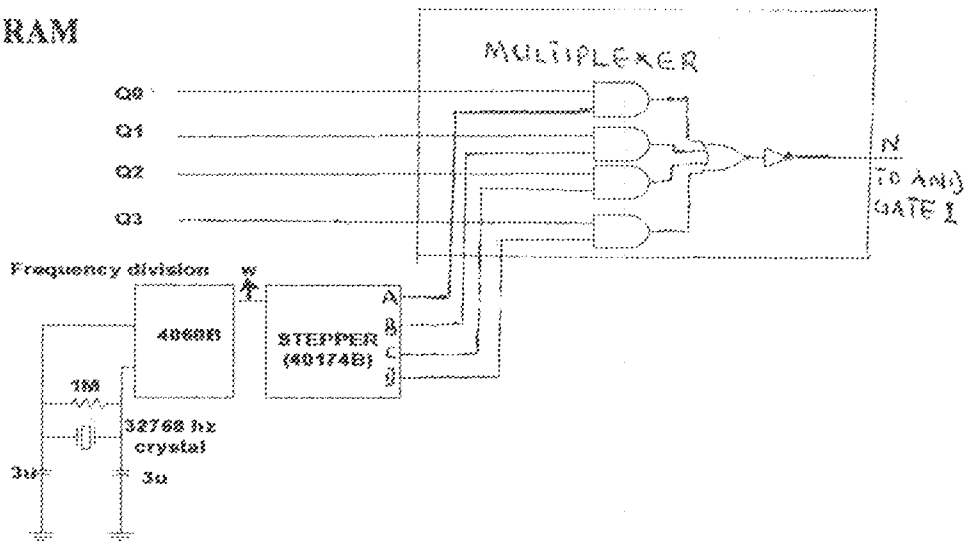
The output from the inverters by pressing SW1 will be 110 as shown in the table 2b. These three codes are passed on to the register through the data bus A as shown in the circuit diagram 2a. The **OR gate** sums up the output from inverter and its function is to give an output whose level of code controls the transmitter from repeated transmission of signals.

The shift register, as earlier mentioned is a D-type flip-flop and is chosen for this project in order to have a delay unit that causes output to follow the input but delayed by a single data input (D) and a clock input. At a time of specific clock transition, the outputs take on the value of the D input. That is, the input bits are placed on the D-lines and with the arrival of a clock pulse, the input data are transferred to output Q0, Q1, Q2 and Q3 (1110) and to the next device. Once the clock pulse has triggered the input gates of the flip-flop, any further changes in the input states will have no effect on the output. This greatly minimizes errors in the transfer of binary data to other unit of the logic circuits.

MULTIPLEXER AND STEPPER

This project employs a multiplexer of AND-OR gates as shown in the circuit diagram.

CIRCUIT DIAGRAM



STEPPER AND MULTIPLEXER UNIT

Fig.2e

A Multiplexer as the name implies is an electronic device that performs the function of a very fast rotary switch. It has several input lines from which a line is selected to one common output line. The input lines share a single communication line with each line having a certain amount of time to be selected. This time-sharing technique is known as time multiplexing.

The input are selected one after the other by application of input address lines (data select).That is, address lines select any one of the input lines.

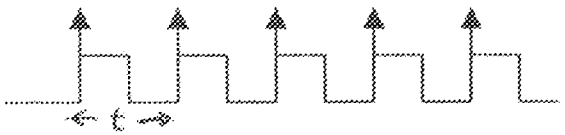
From the above description of multiplexer, it can be concluded that multiplexers are used as parallel –to- serial data converter and this is the feature that made it useful in this project. That is, the output codes from the shift register given in parallel are converted to a serial output.

The input address line used for input line select in this project is known as **JOUNSON STEPPER**. The speed of this stepper is controlled by clock pulses obtained from 4060B. That is, the 4060B is a frequency divisor component IC which divides the frequency generated by the crystal oscillator. The clock pulses also controls the movement of data around the various elements of the system and determines the speed of the operation. The stepper works in such a way that it generates a four bit codes at a period of 0.5 second. That is, from the clock pulses of 8 Hz, we can obtain a period of 0.125second (1\8) to generate a bit code. Therefore, a four bit codes will be generated at the period of 0.5 seconds.

The truth table below shows the truth table of the stepper

Clock Pulses	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Table 3.0: Truth table for Stepper



t = 0.125 second

Fig.2f

The stepper as earlier described does the work of input line(channel select) address which makes the codes to be transferred from the register to the multiplexer and from multiplexer to the next unit to be under control..

Using fig. 2g below, we can have a better understanding of how stepper and the multiplexer work

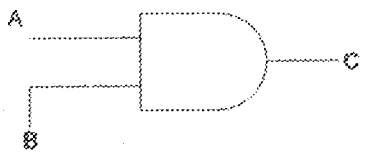


Fig.2g.

From the figure 2g above, B must be 1 so that the logic level, 1 or 0, at A is transferred to C. But when B is 0, C remains 0, despite the logic level at A. Subsequently, the AND gate is disabled.

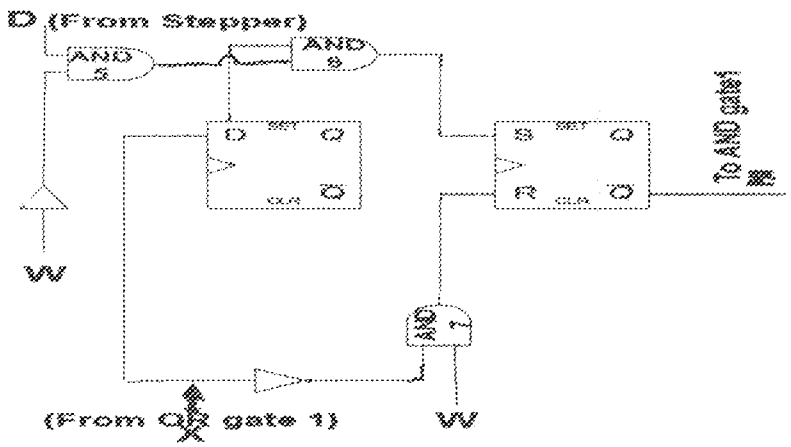
Relating the above fact to the multiplexer used in this project, if the codes from register are to be serially transferred, then they must do so by channel selection. Therefore, the first set of codes from stepper that select the first line of the multiplexer must contain a binary code of 1 as shown in table 3.0

However, it is seen from the truth table that the initial clock pulse allows an output of 1000 which makes output at A to be high. Output A becoming high will therefore cause a line to be active (DA) at the input of the multiplexer. At the second clock pulse, 1000 will be transferred from the output at B and this in turn allows the multiplexer to select another input line (DB).Subsequently, DC will be selected and lastly DD.This is how the stepper send codes in series of cycle to select an input data to multiplexer.

It is observed that the period it takes to send one complete cycle of codes is 0.5 second, since it takes a code, a period of 0.25 second to be transferred. Finally, the output of the multiplexer is fed to the next unit whose action determines the operation of the transmitter.

TRANSFER CONTROL LOGIC UNIT

The transfer logic control consist combination of different logic gates, which include D type flip-flop, RS flip-flop and AND logic gates as shown in the circuit diagram.



TRANSFER CONTROL LOGIC UNIT

Fig. 2h

Fig.2h shows the circuit diagram of transfer control logic unit and is responsible to control any repeated transmission of signal from the transmitter to the receiver, despite the stepper aims to send the code in series of circles.

OPERATION

From the circuit diagram, label **X** comes from OR gate 1 of the inverter and the register unit whose function is to notify, whether a code is present to the system or not. When a code is present, **X** will be 1 and 0 for absence of code.

The **D type flip-flop** acts as a code register which stores the presence or absence of the last code to the latch. The output of the **D flip-flop** is fed into the **AND gate 6**.

For the **AND gate 6** to have a "high" (1) output, output of **AND gate 5** must be "high" (1).The two input to **AND gate 5** are the clock pulse that clock the stepper and the last output from the stepper. That is, the transfer of codes from the stepper, which notify that the last code has been transferred by the multiplexer.Therefore,if actually there is presence of code as earlier said, the output of **D type flip-flop** will be "high"(1) and the output of **AND gate 5** will also be "high" as long as the clock pulse is active. Subsequently, **AND gate 6** will be high "high" (1) which now sets the RS flip-flop to have a "low" (0) output at **Z** through **Q**. The output at **Z** is connected to input of another AND gate (**AND gate 1**), which disenables the transmitter from repeated transfer of signal to the receiver (even if hand is still on the push-button 1).On the other hand, **AND gate 7** will generate a "low" (0) output which makes the Reset button to be inactive. On the other hand, let us consider a situation where by no code is present at label point **X.** That is, when no switch is pressed, inverter output will be 000, making the output of OR

gate to be 0.This makes X to have a code 0, the output of D flip-flop to go "low" and subsequently makes the output of the **AND gate 6** to be "low" (0).Then, the overall output at **AND gate 6** and **AND gate** 7 will now reset the RS flip-flop for the next codes to be transferred.

AND GATE 1

The inputs to **AND gate 1 (4073B IC)** are three; one from the multiplexer, one from transfer control logic that controls the system from a repeated transmission of codes (transmitter to the receiver), and the third input from the crystal oscillator which generate frequency and clock pulse.

Considering the codes from the multiplexer cannot be easily decoded by the decoder at the receiving end. For this reason, the clock pulse has to be used in transmission in order to have a perfect decoded output at the receiving end. For the output of **AND gate 1**, to be "high" (active), the three input i.e. (n),(z) and (w) must be "high", and this subsequently triggers **on** the transmitter. However, if any of the input to **AND gate 1** is "low", then the output of the **AND gate 1** will be "low" (inactive) and triggers the transmitter **off**. Therefore, the output at AND gate1 determines the state of the transmitter, whether **on** or **off.** If **on**, there will be transmission while there will not be transmission if **off.**

CIRCUIT DIAGRAM

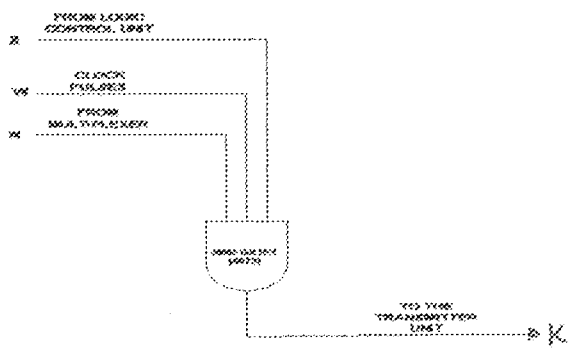
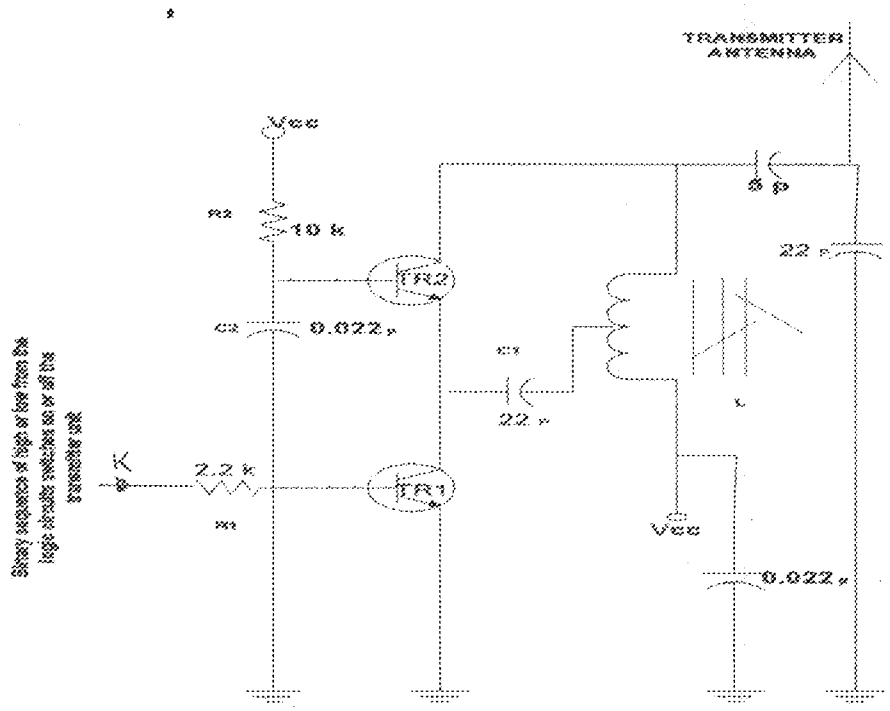


Fig 2f : AND GATE 1

TRANSMITTER UNIT

The transmitter unit is basically the unit that generates the signal to be transmitted.



TRANSMITTER UNIT

Fig.2j

Fig.2j above shows the transmitter unit whose state of operation is determined by the output state of the logic units.

For instance, pressing push-button 1 (SW1) generates sequence of binary codes (high or low) and subsequently these codes pass through different logic units unto the transmitter unit.

In the transmitter, the LC oscillator generates a resonance frequency given as $f=1/2\pi\sqrt{LC}$. This implies that the generated frequency can be varied by varying the inductor as shown in fig 2j. This is necessary in order to generate a frequency that should be in resonance with the receiver. **TR1** is used as a switching element for the oscillator and it does this whenever signal flows through its base and this is what cause the generation of frequency in the oscillator tank. The flow of signal continues until **TR1** reaches its saturation stage and cuts off. At this stage, there will be feedback signal to **TR2** through capacitor **C1** and therefore turns on the transistor (**TR2**).The output of **TR2** is amplified and transmitted by the transmitter antenna.**R1** is used to control the flow of signal into **TR1**.

ANTENNA

This is the last unit in the transmitting part, and its function is to cause the generated signal from the transmitter to transmit to the receiver. It does this by radiating the signal generated from the transmitter unit into the atmosphere as electromagnetic wave that can be picked up at the receiving end by the receiving antenna.

The transmitting antenna may transmit several kilowatt of power while the receiving antenna may receive a few milliwat dissipated in it. The reason been that not all signal radiated from the transmitting antenna will be able to get to the receiving antenna.

THE RECEIVING PART

The receiving part consists of different units as it is in the transmitting part. The analyses of these units are given in accordance of their functions.

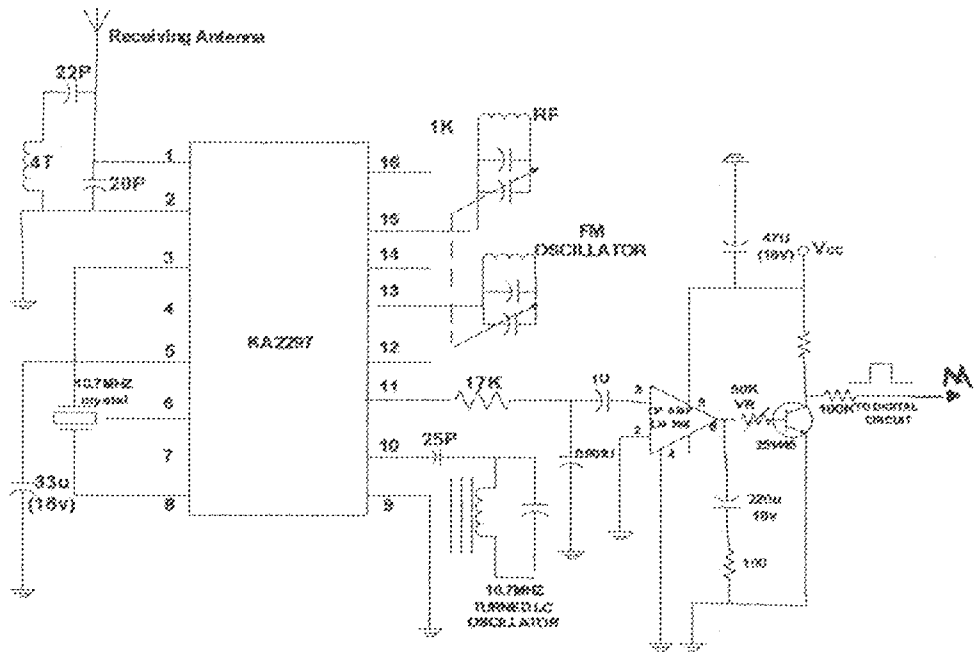
ANTENNA

This receives the electromagnetic waves radiated from the transmitting antenna.

RADIO FREQUENCY RECEIVER UNIT

This unit selects the wanted signal transmitted and extracts the intelligence contained in the transmitted signal in order to produce frequency output of sufficient power.

CIRCUIT DIAGRAM



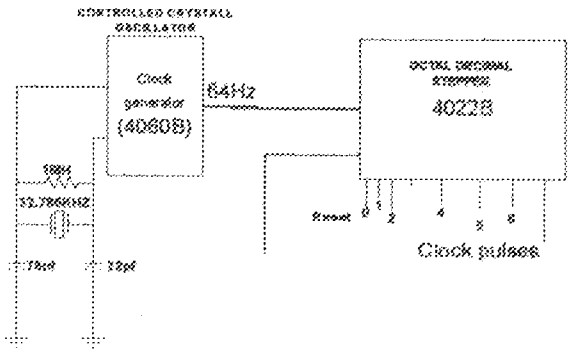
Receiver circuit

Fig 2k

Fig. 2k shows the circuit diagram of the radio frequency receiver. The receiving antenna receives the radio frequency and passes it to the local oscillator of KA2297 IC. This radio frequency (RF) is then mixed up with the frequency generated by the local oscillator of the IC to produce an intermediate frequency (IF). As shown in fig. 2k, the IF is filtered out through pin 3 of the IC into the 10.7 crystal. Pin 8 of the IC recollect the frequency and this further filtered by the tuned LC oscillator. The signal is finally amplified by the **Operational Amplifier** (LM 386). This amplified signal is passed through the NPN transistor (2S1445). The operation of the transistor is such that it switches on whenever there is signal through its base and switches off when there is no signal. The output of the transistor is therefore a square waveform which is fed into the next unit of the system (the logic units) as sequence of binary codes.

CRYSTAL CONTROLLED OSCILLATOR AND STEPPER

This is one of the logic units in the receiving part and its function is to generate frequency and clock pulses that are used for timing purpose of all the logic components



CRYSTAL CONTROLLED OSCILATOR AND STEPPER UNIT

Fig. 2l

The operation of the oscillator is the same as it is in the transmitting part. The octal decimal stepper is however different in the sense that it divides the clock pulses generated by the oscillator into eight equal parts. Also, the operating frequency is 64 Hz which means that the period is 0.016 sec. (1/64).

As seen from the circuit diagram, the octal decimal stepper divides the frequency from the frequency generator to obtain clock pulses. Each pulse will now be used to clock any of the logic circuit according to the operation of the circuit.

RS FLIP-FLOP

There are two SR flip-flops used in the receiving part. These are 40B and 4013 ICs. The 40 B is used to reset the receiving system after a complete transmission of first set of signal from the transmitting part while the 4013 is used in any phase-error correction between the transmitter and receiver.

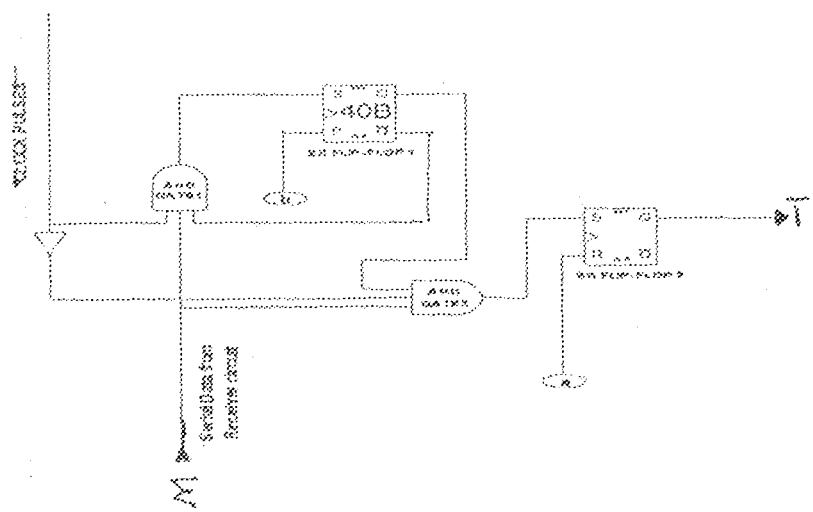


Fig.2i

The flip-flops as shown in the circuit diagram are flip-flop1 and flip-flop2.These can be enabled or disabled by AND gate1 or AND gate2.

As earlier said, flip-flop 1 reset the receiving part after every complete transmission between the transmitter and the receiver. While the flip-flop 2 is used to improve the level of output generated from the transistor.

Note that whenever AND gate 1 is enabled, AND gate2 is disabled and vice-visa. Also, a high clock pulse enables gate1 and disables 2.

The output from SR flip-flop 2 is fed into the input of a "shift register" which forms the next unit of the logic circuit.

SHIFT REGISTER AND THE LATCH

The shift register is a 4015B IC while the latch is 40175 IC.

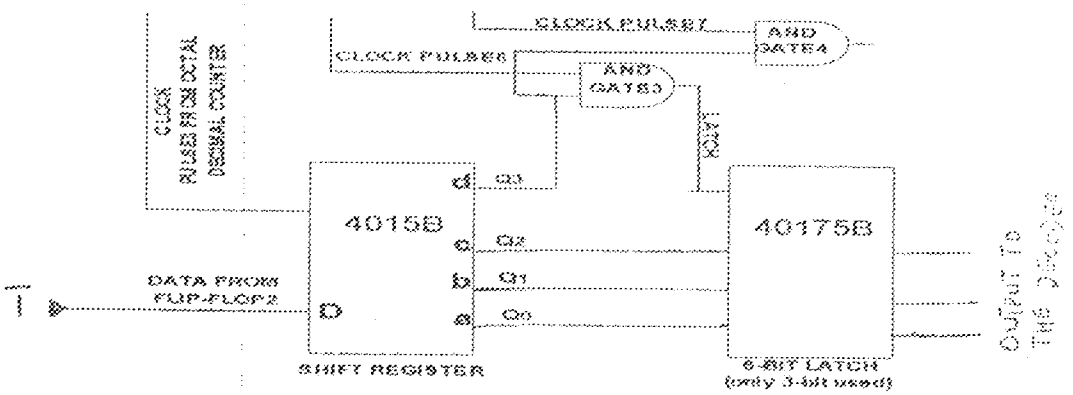


Fig.2j

A brief analysis of shift register has been given in the transmitting part. However, the shift register used in the receiving part is different. That is, this is a serial in/parallel out shift register. The circuit diagram below shows the internal circuit diagram of the shift register.

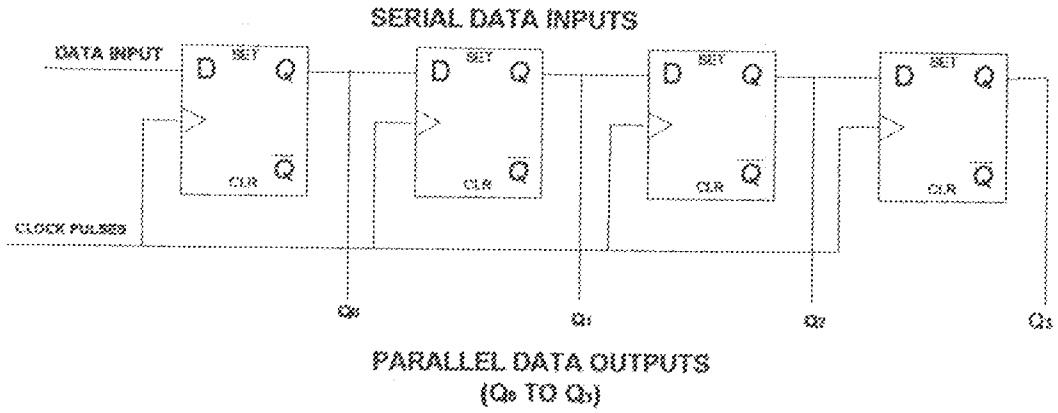


Fig.2&

INTERNAL CIRCUIT DIAGRAM OF THE SHIFT REGISTER

As indicated in the circuit diagram, the data input to the four flip-flops are in serial. That is, for any clock pulse generated, data is entered into the first flip-flop thereby shifting whatever is in the flip-flop to the next flip-flop. However, data output of the register is such that the data are simultaneously available at the output.

Relating this to system design, the output from flip-flop2 is fed into the shift register at the period of third (3) clock pulse from the octal decimal stepper. Subsequently, the rest of the data is stored into the shift register (serially) until the last data is stored in the fourth flip-flop. At the fourth code (data) transfer, the code leading logic must have been shifted to d output of the shift register. The transfer of code to d output

and the clock pulse 6 from the stepper enable AND gate3. The output from AND gate3 now latches the codes coming from the shift register to the 6-bit latch (40175B).

DECODER

Generally, a decoder operates in such a way that the input signals are treated as a binary number and select the one output line corresponding to that binary number. If the other outputs are "low", then the selected output goes "high"; if the other outputs are "high", then the selected output goes "low". Then, the input binary number is said to have been decoded. Ignoring the control inputs, the number of output line is determined by the number of input line. Generally, with n input lines, a decoder will have 2^n output lines.

The decoder used for this project is **4028B** IC and this is shown in the circuit diagram below.

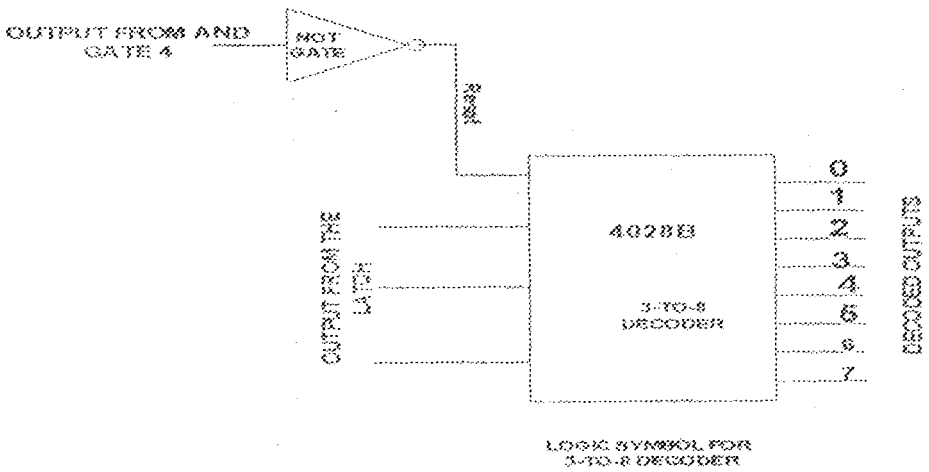


Fig.2m

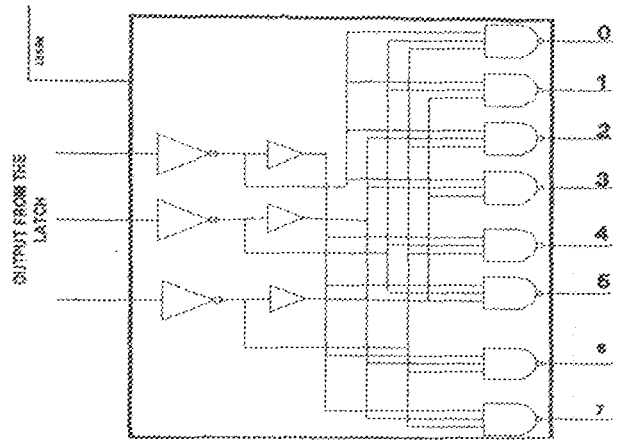


Fig.2n

INTERNAL CIRCUIT DIAGRAM OF THE DECODER 20

From fig. 2p above, the decoder has three inputs, while the number of output is 8. This is simply called a 3-to-8 decoder. However, as far as this project is concerned, only 6 output lines are utilized. These six output lines are connected to the next unit of the logic circuit. Also shown in fig 2m is the reset line. This controls the input levels by which the output lines are being selected.

JK FLIP-FLOP

The JK flip-flop is a versatile device and is one of the most commonly used flip-flops. It is similar to SR flip-flop, but different in that it has no invalid state as does the SR flip-flops .In JK flip-flops, all conditions of inputs (J and K) are possible.

A JK flip-flop can have a common input of "high" state. Whenever a JK flip-flop operates in this way, it is said to operate in toggle state and this is the principle that has been employed in making use of JK in this project.

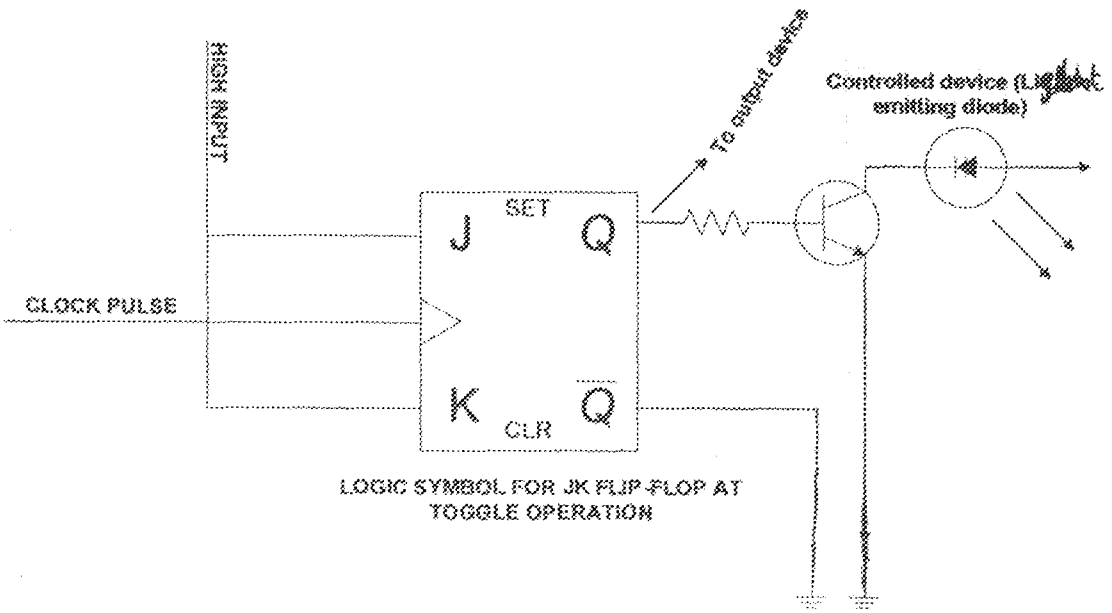


Fig.2p

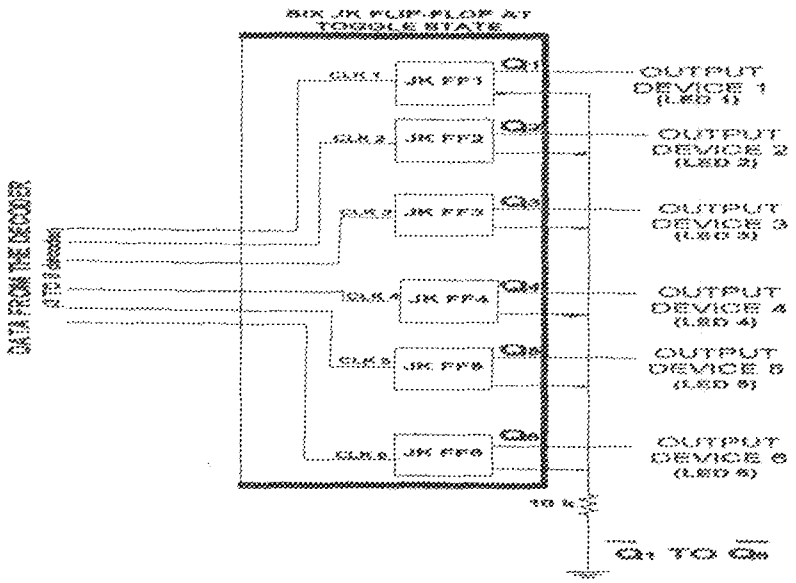


Fig.2q: LOGIC SYMBOLS SHOWING COMBINATIONS OF SIX JK FLIP-FLOPS AT TOGGLE STATE

Fig 2q shows how JK flip-flop at toggle state are been used to operate device from circuit diagram. The outputs from the JK are Q and $\overline{Q}$. While the outputs Q are connected

to a device to be controlled, the outputs $\bar{Q}$ are grounded. From fig 2p, the output line Q feeds the transistor (TR4) whose state of operation controls the light emitting diode. For a better understanding of how the LED operate, let us assume a situation when a push-button e.g. SW1 is pressed from the switching unit of the transmitting part. Transmission between the transmitter and the receiver is established. This establishment causes coded signal transmission from transmitter and decoded signal in the receiver. The decoding is done by any decoding device, a 3-to-8 decoder in case of this project. The decoded signal will now be fed into JK flip-flops. Therefore, whenever there is a "high" output from Q of the JK flip-flop, the transistor (TR4 is switched on and allows flow of signal through the collector of the TR4 which finally switches the LED "on". On the other hand, whenever there is a " low " output from Q of the JK flip-flop, TR4 is switched off and no current flows. This finally switches "off" the LED.

CHAPTER THREE

CONSTRUCTION, TESTING AND RESULTS

This chapter discusses the construction and testing of the project whose design has been analyzed in chapter two. It also lists out the tools and components used in the project as shown below.

CONSTRUCTION

The construction of the project was carried out using the steps that have been designed. Construction took place by assemble the entire components one after the other on a breadboard. Following the assembly of components on the breadboard was testing. Immediately after this was the laying and soldering of the components on the Vero board. During soldering, great care was taken to avoid short circuit and minimize components damage. After soldering, the digital circuits were tested again by powering the ICs, while the analog circuits, such as transmitter unit in the transmitting part was tested by using multimeter to test the conditions of all the resistors and the capacitors.

CMOS ICs were used for the construction of all the digital circuits. CMOS ICs were chosen because of the fact that they have low power consumption. As such, the power supply to the whole system is a battery source (9v).

A wooden casing was also constructed in order to house the board containing the components.

TESTING

Series of testing that were carried out include the test for output voltages at all the units by the use of digital multimeter.

Continuity test were also done to avoid short circuits.

The transmitting part and receiving part were tested by connecting the two parts together using a wire. This was done in order to be sure if there is transmission between the two parts. Also, the transmitting part was separated and tested by the use of a radio receiver to sense the signal transmission of the transmitter.

RESULT

Various results were obtained for various testing. For instance, there was transmission between transmitter and the receiver when they were connected using wire.

Also, a radio receiver sensed the signal from the transmitter by making a noise when the transmitter was switched on.

When the transmitter and the receiver were separated a push-button pressed from the transmitter triggered on or off a light emitting diode connected to the output of the receiver.

DISCUSSION OF RESULT

From the design, results obtained at various stages show that the expected results were satisfactory except for the fact that the distance between the two was not much. This could be as a result of component malfunctioning and the tuning of the frequency between the transmitter and the receiver.

CHAPTER FOUR

CONCLUSION

From the design, the project was constructed and tested through which the aim of the project was achievable. That is, using the principle of wireless transmission, transmission between two system (transmitter and receiver) could be established and this can be used to control a device connected to the output of the receiver

RECOMENDATION

Due to some difficulties encountered during the cause of this project, some recommendations are given below:

- The practical orientation of the students should be taken more serious in order to eliminate poor design of students' final year projects.
- Government should be assisting students by providing research centers where projects enquires can be made.
- To design a more effective and efficient control system which can be used at home or in other places, the frequency generated from the LC tank of the transmitter should be of a high range.
- The University system should make available equipment that can be used to test various components used in the project design.

TOOLS AND COMPONENTS USED

TOOLS

Breadboard, Vero board, Digital multimeter, Soldering iron and soldering lead, Lead sucker, Hammer, Cutter, Drilling machine, Nails and Copper wires.

COMPONENTS

ICs: - 40174, 4060B, 4017B, 4022B, 40175, 4028B, 4027, 4013, 40B and 4069.

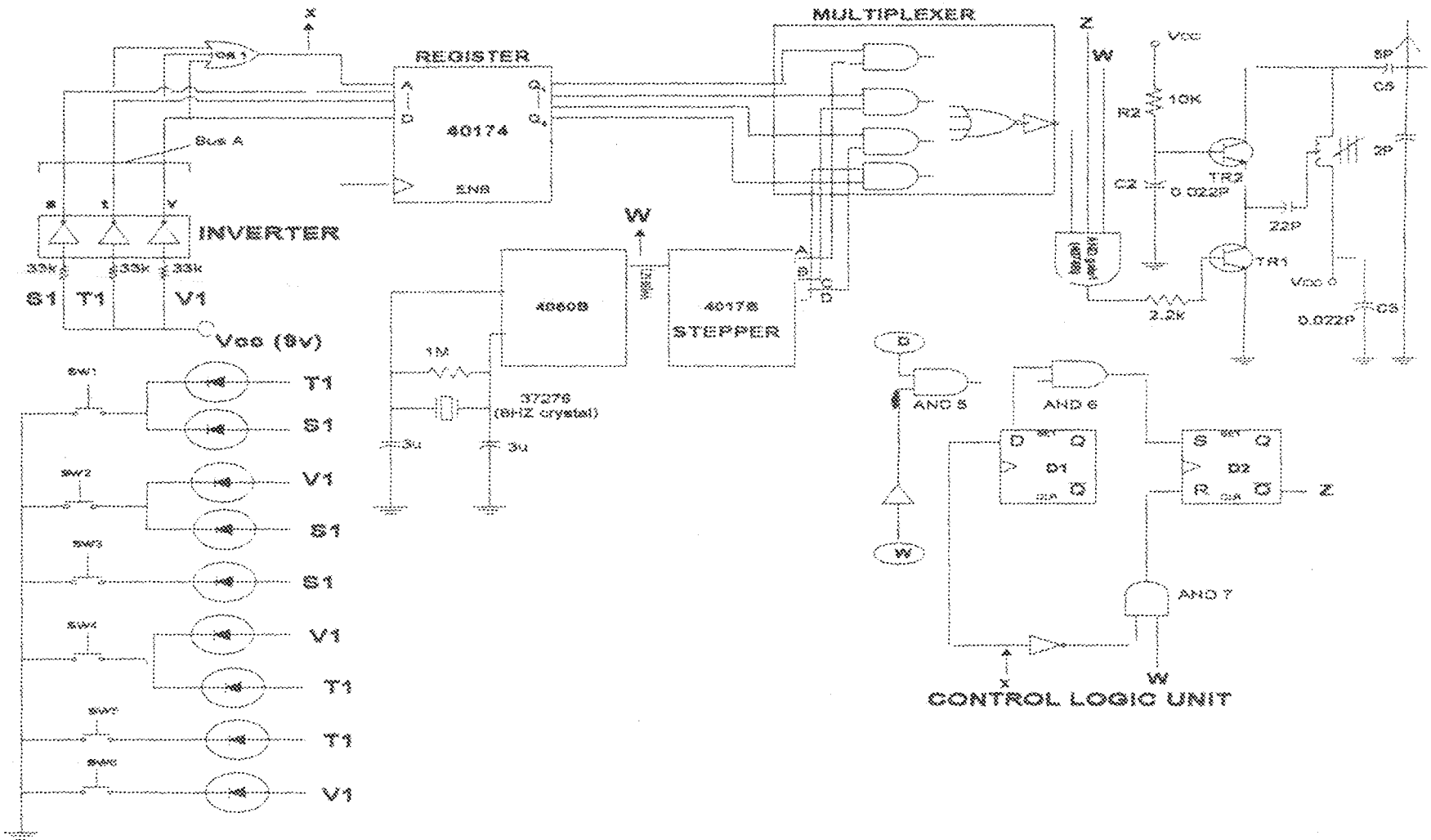
CAPACITORS: - 0.022pf, 2pf, 5pf, 20pf, 22pf, 25pf, 25pf, 27pf, 30pf, 75pf, 47pf, 33pf, and 5pf.

RESISTORS: - 100, 10K, 50K, 100K, 17K, and 1M all measured in ohms

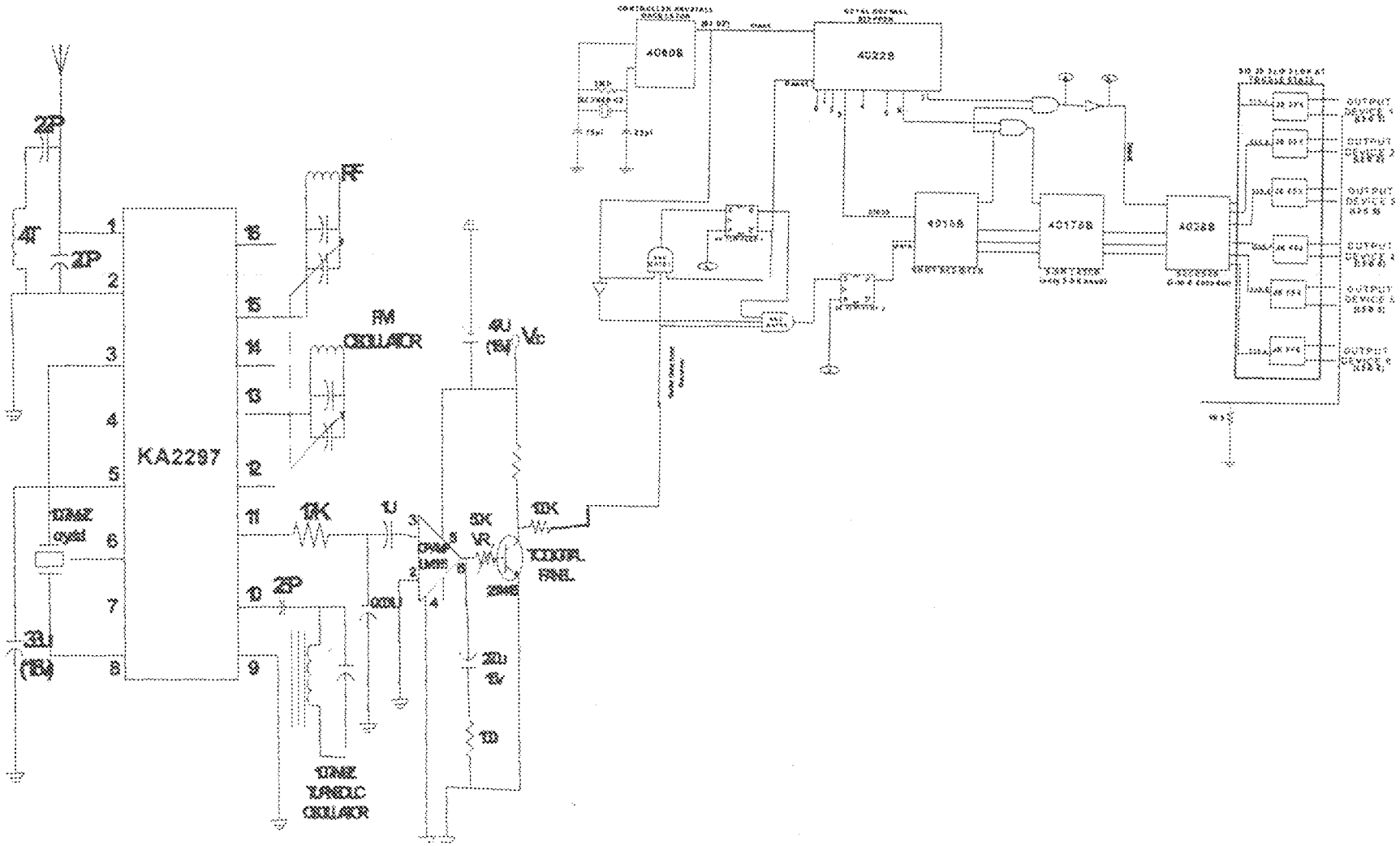
DIODES: - Nine power diodes and eight light emitting diodes.

VARIABBLE and **FIXED INDUCTOR**

SWITCHES: - Six push - button



COMPLETE TRANSMITTING CIRCUIT DIAGRAM



COMPLETE RECEIVING CIRCUIT DIAGRAM

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