Design And Construction Of Digit Combination Sequential Door Lock With Burglar Alarm

BY

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MARCH, 2000

TITLE PAGE

THE DESIGN AND CONSTRUCTION OF A-DIGIT COMBINATION SEQUENTIAL DOOR LOCK WITH BURGLAR ALARM

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A PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY

FEDERAL UNIVERSITY OF TECHNOLOGY

MINNA, NIGER STATE

MARCH 2000.

DECLARATION

I, Nwaiwu Chima Mathias, hereby declare this project in its entirety and originality is designed and constructed by me under the supervision of Mr Paul Attah and I also affirm that it has never been presented else where in this form as a final year project in any high institution.

Sign 27/03/2009

Nwaiwu M.C Date

CERTIFICATION

I hereby attest and certify that I approved and supervise this project work which was considered to meet the standard in scope and quality for award of Bachelor Degree in Electrical and computer Engineering.

Federal University of Technology Minna.

MR PAUL ATTAH

SUPERVISOR 24/03/2020

SIGN **DATE**

DR. Y. A. ADEDIRAN
HEAD OF DEPARTMENT 24/3/2020

SIGN **DATE**

DR. J.O.ONI
EXTERNAL EXAMINER ....

SIGN **DATE**

DEDICATION

This project is dedicated to my beloved sister Ijeoma for the role she played in my career .Without God nothing good would have been achieved. Therefore, I say thanks to God for giving me the skill and ability to make this project a reality.

This project is also dedicated to my darling brother Mr C. A.S Nwaiwu for his immense contribution in what I am today and what I shall be in future.

Finally, Lilian Odimma, my heartthrob, is Fondly remembered here and I pray that God who led us through this thin years shall also lead us through in the thick years ahead.

ACKNOWLEDGMENT

I am indebted to Almighty God for his untold love and guidance during the course of my study and most wonderful is His boundless grace and life which was abundantly showered on me. May His name be glorified for ever and ever.

My unquantifiable appreciation goes to my elder brother Mr C. A. S Nwaiwu for the role he has played in my life. May his effort be rewarded in many folds.

Again, my air of appreciation goes to my beloved sister Ijeoma. A for spearheading the whole process and may her seed be grown in a soil enriched in fertility. I rejoice fully thank God for given me wonderful brother like Mr Jerald Nwaiwu and his family, My sisters Mrs Augustina Igbem and Mrs Benedicta Anyanyi. Their brotherly and sisterly love will always remain evergreen in my memory. Again, my wave of gratitude also blows to Miss Mary Eze for her relentless effort in ensuring that my report is ready ahead of schedule. All my relatives and other brothers and sisters are also thanked for their numerous contribution too many to mention. My field day and moment with my friends scattered all over Nigeria is not ignored and I say, God bless each and every one of them. I thank Mr Oluegbuniwe for his financial support and pray for God's blessings in his life.

My inexpressible gratitude goes to my sweet parents Nze B.O Nwaiwu and Lolo B. Nwaiwu for being the focus of my existence and the unlimited love and care they rained on me. I sincerely promise them to uphold the virtues of the family and to make them proud.

I heartily thank my project supervisor Mr Paul Attah for all the support and encouragement he gave me for the realization of this project. I also thank Mr Nnamdi Onyebuchi for his assistance during the course of this project. I pray God to water their seed.

My special appreciation goes to my friends Mr Desmond Ekwebelem for his timely assistant, Mr Paul Nwohiri, Mr Festus Abazie and his family and Mr Chika Ogu for all the good deed. My pround regard to miss Lilian odimma and her family for their inspiration and encouragement. I pray for God to grant us life to see our joint dream fulfilled.

Finally, I thank my friends and fellow classmate and the entire staff of electrical & computer engineering depatment.

TABLE OF CONTENTS

CHAPTER FOUR: CONSTRUCTION,TESTING AND RESULTS

CHAPTER FIVE: CONCLUSION, APPLICATION, RELIABILITY AND RECOMMENDATION

ABSTRACT

The ease with which hoodliums break into houses, vault of companies, banks and corporate bodies calls for urgent attention. This evil act by men of underworld has brought misery, hardship, agony, pain and death to its victims. To help check the activities of these evil people and to restore the human dignity is the design and development of this project. It is a door locking and unlocking device which in the right combination of the digits effects the locking and unlocking process. It also incorporated in its system an alarm keys randomly spaced among the right keys. Any of this alarm keys when impressed has the ability of triggering of the alarm. This could be concealed in a security office or by generating a loud sound that will attract the attention of neigbours and passers by. By this, the culprit/s may be caught redhanded.

As the title implies, it is a project that functions by the sequencial combination of encoded digits which could be as many as the designer desires. In this project, there are four right keys, two foolproof keys and two resetting keys. Intrusion by trial and error of the key are dangerous and dictated by the alarm system However, the system is limited by failure due to unreliability of power supply in Nigeria.

It compose entirely of memory chips, timer chip for synchronization, electromagnetic relay, Loud speaker, and solenoid which pull-in and push-out the hook for unlocking and locking operation.

Chapter four is the construction and the detailed description of the system. It also included the choice of casing and general assembly of project. Errors encounttered and prevention are also discussed.

Chapter five tells the reader the conclusion of the project, application and reliability of the project. It further included the recommendation and references.

CHAPTER TWO: SYSTEM DESIGN

2.2.0 POWER SUPPLY UNIT

This unit supplies the stipulated and regulated power to the entire system. It converts ac power supply to regulated d.c voltage thereby aiding the device to function properly.

The power supply unit is designed to meet up with the need and requirement of the device in its circuitry.

This is further illustrated for easy understanding by the block diagram in fig 2.10

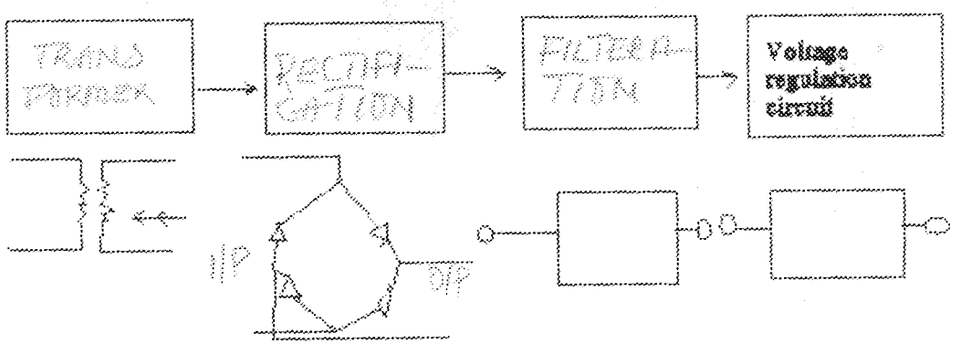


Fig 2.10 The power unit block Diagram

2.2.1 Design and specification of power supply.

2.2.2 The Transformer

In the transformer stage the 240v ac supply from mains is reduced to 15volts ac by the step down transformer. This is to suit the requirement of the solid-state electronic devices and circuit fed by the dc power supply. It also provides isolation from the supply line.

2.2.3 RECTIFICATION

2.2.3 Bridge rectification stage

This is the most commonly available and frequently used circuit for electronic dc power supply. It consist of four diodes in one device inside a four terminal case.

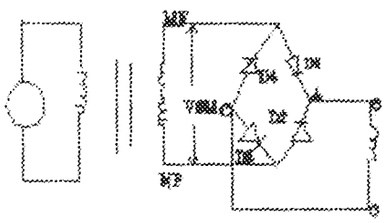


FIG 1.1

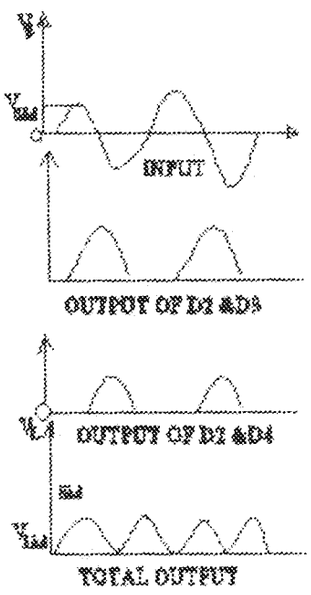


Fig 2.21a

2.2.4 The Working of the full Wave Bridge Rectifier.

During the positive input half cycle, terminal M of the secondary is positive and N is negative as shown in figure 2.21 D1 and D3 become forward biased and hence (ON) whereas D2 and D4 are reverse biased hence (OFF). This makes current to flow along MEABCFN producing a drop across Rl. During the negative input half cycle secondary terminal N becomes positive and M becomes negative. D2 and D4 are forward Biased, circuit current flows along NFABCEM as shown. Hence we found that current keeps flowing through load resistance RL in the same direction AB during both half cycles of the ac input supply. Consequently, point A of the bridge rectified always act as an anode and point c as cathode. The output voltage across RL is as in fig.2.21b.

AVERAGE AND RMS VALUES

$$V_l = V_{Lm}/\sqrt{2} = 0.702\,V_{Lm}$$

$$V_{l\,DC} = 2V_{Lm}/\pi = 0.6364$$

$V_{l\,AC}$ = **Rms value of ac components in the output voltage.**

$$= \sqrt{V_l^2 - V_{l\,DC}^2}$$

Similarly, $I_m = \dfrac{V_{Lm}}{R_l}$

$$I_L = \frac{I_{Lm}}{\sqrt{2}} = 0.707\,I_{Lm}$$

$$I_{AC} = \sqrt{I_L^2 - I_l\,(DC)^2}$$

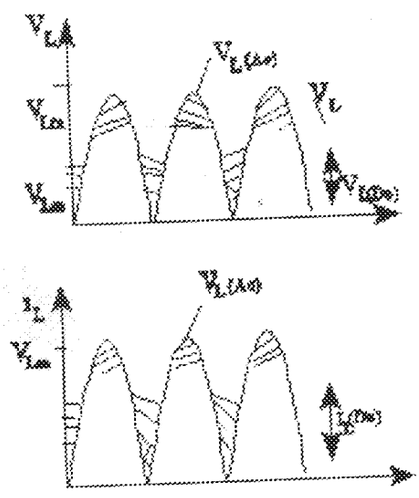


Fig 1.1b

Fig 2.21c. The Ripple factor

RIPPLE FACTOR

$$R = \frac{V_{L(Ac)}}{V_{L(Dc)}} = \frac{V_{R(Rms)}}{V_{L(Dc)}} = \frac{0.305V_{LM}}{0.636V_{LM}} = 0.482$$

2.2.5 Why I Preferred Full-Wave Bridge Rectifier

There is no centre-tap on the transformer

much smaller transformers are required

it is suitable for high voltage application

It has less P1v rating per diode

2.2.6 FILTERATION

The main function of a filter circuit is to minimise the ripple content in the rectifier output. This is as the result of the pulsating output of each rectifier. This type of output is not useful for driving electronic appliance and therefore require a steady output like that of a battery's output.

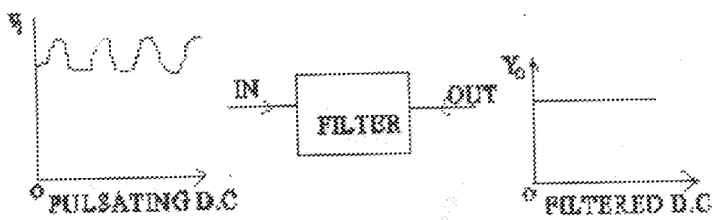


Fig 2.22

2.27 SHUNT CAPACITOR FILTER

Here, the single capactor is connected across the rectifer in parallel with the load RL to achieve filtering action. This is called shunt capactor input filter. Filteration by capacitor depends on the property of a capacitor to charge up during conducting half cycle and discharge during the non conducting half-cycle. When this is connected as described above over a pulsating d c voltage, it tends to smoothen out the ripples as shown below.

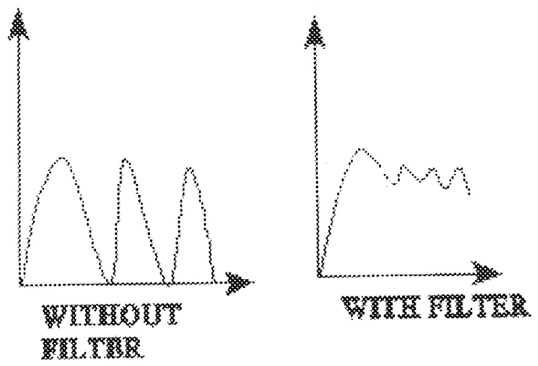


Fig. 2.2.3

2.2.8 VOLTAGE REGULATION

In an unregulated power supply, output voltage changes with the input supply voltage or load resistance changes. The change in voltage from no-load to full load condition is refered to voltage regulation. The work of the regulator circuit is to reduce this variation to zero or to the minimum possible value.

$$\text{Percentage regulation} = \frac{V_{Max} - V_{Min}}{V_{Min}} \times 100$$

Where V_{Max} - Maximum dc output voltage

V_{Min} - Minimum output voltage

CHAPTER THREE:SYSTEM CONSTRUCTION

3.0 The Block Diagram

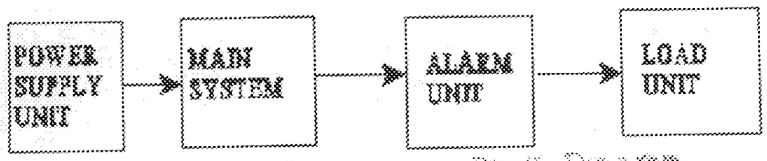


Fig 3.0 The system Block Diagram

3.1.0 CIRCUIT OPERATION

The flip-flops which constitute the memory section is connected serially with the output of the first flip-flop connected to the input of the second one and in that order. In the first positive edge triggering of the clock, the output from the first flip-flop becomes high as seen in the table 4.3. Thus forms the input of the next flip-flop. Again, when the clock of the 2nd flip-flop is triggered by using the 2nd key switch, the output becomes high and forms the input of the next flip-flop. This sequence continues till it gets to fourth and last flip-flop . The outputs from these flip- flops are connected to a NAND gate which provides the triggering input to the 555 timer monostable oscillator. The oscillator remain at this signal level till a threshold input is driven, at which time the output goes low.This triggering input is activated by an input level below 1/3 Vcc and threshold is activated by an input level above 2/3 Vcc. In its characteristic manner, the oscillator will function to produce a regularly spaced time interval. In the application in which it is required in this project, it will give an output voltage which is periodicaly high or low. This is connected to the seloniod which causes it to be magnetic due to magentic field created in the coil of the solenoid. This inturn, will magentize a small metal rod attached to it. This magnetic ability of the solenoid bring about the pulling and releasing action of the system

3.2.0 THE FLIP-FLOPS

This is a memory device that not only depends on the immediate input state but also on the past history. There are many types of flip-flop such include edge trigger type D flip-flops, master-slave flipflops, clocked flip-flops and the jk flip-flops. In my design work I used the master slave jk flip-flop (4027) CMOS. As can be seen fom the diagram below, the flipflop uses two SRFFS together with input gating logic. The output of the second or slave SRFF is fed back

to the input logic of the first SRFF (master). The most important feature is the inverter in the clockline. The clock is directly connected to the master but passes through an inverter before entering the slave When the clock is high, the inputs switchs the master and the feedback from Q2 and Q2 prevents S1 and R1 from being simultaneously one. The slave inputs S2 and R2 remain at zero owing to the inverter in the clock line inhibiting the output of gates 3 and 4. As the clock switches to zero, data can be input to the slave as its clock, CL2, now becomes one The slave input is the output of the master which remains constant because CL1 is zero and no new data can enter the master. The output of the master is detenined by the sate of the master which is gvoerned by the value of J and K the instant the clock switches from one to zero. The master slave system can therefore be considered as a J KFF which is switched by the data on the inputs at the instant a falling edge occurs on the clock line. Only one change of state, Q, can occur for each clock pulse.

THE CIRCUIT DIAGRAM OF A MASTER-SLAVE jK FLIP-FLOP

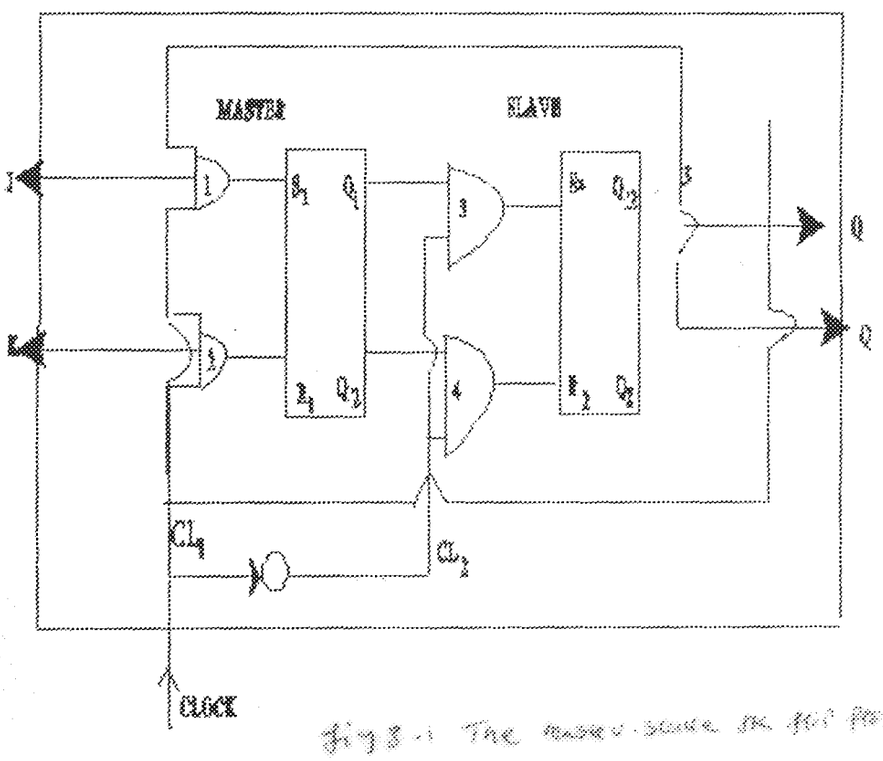


Fig 3 :- The master slave JK flip flop

3.3.0 THE INVERTER

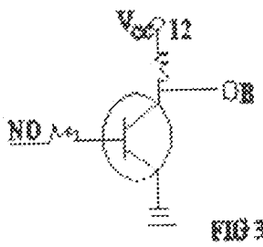


FIG 3.1.1 The transistor inverter

An inveter circuit is that which can invert the input signal or evaluate the complement of the input signal. It is realised in this project using transistor as shown in the figure above. With this arrangement, the output from the NAND gate is inverted or disable by this circuit in order to automatically reset the system or the flip-flop system.

3.3.1 The NAND

It is infact, a NOT-AND gate. It is obtained by connecting a NOT gate in the output of a NAND gate as shown below.

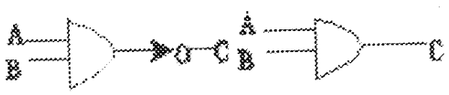
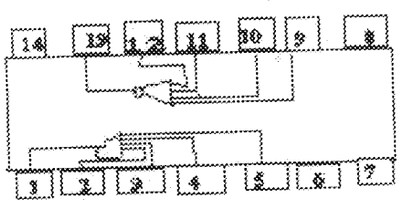


Fig 3.1.2 The NAND gate

The outputs from the flipflops are connected to 4012 ic NAND gate whose configuration is illustrated below



4012 NAND GATE CMOS IC

FIG 3.1.3 4012 CMOS IC NAND gate

3.4.0 THE TIMER SECTION

3.4.1 OSCILLATORS

Within nearly every electronic instrument it is essential to have an asicillator or waveform generator of some sort.

Apart from the obvious cases of signal generators,function generators and pulse generators themseles, a source of regular ocillation is necessary in digital instruments.

For instances, oscillators are used in digital multimeters, osciloscopes, radio frequency receivers, computers, counters, timers, calculators and host of other devices too many to mention.

Depending on the applications, an oscillator may be used simply as a source of regularly spaced pulse, e.g a "clock" for a digital system in which is the area of my concer. Again, other uses or application can result from osicillators ability to be stable and accurate, or its capacity to produce accurate waveforms e g the horiontal sweep ramp generators in oscilloscope.

Among the various types of oscillator available, a timer chip; the 555, is used which is an advancement in the monostable multivibrator oscillator. Its simplified schematic diagram is shown below.

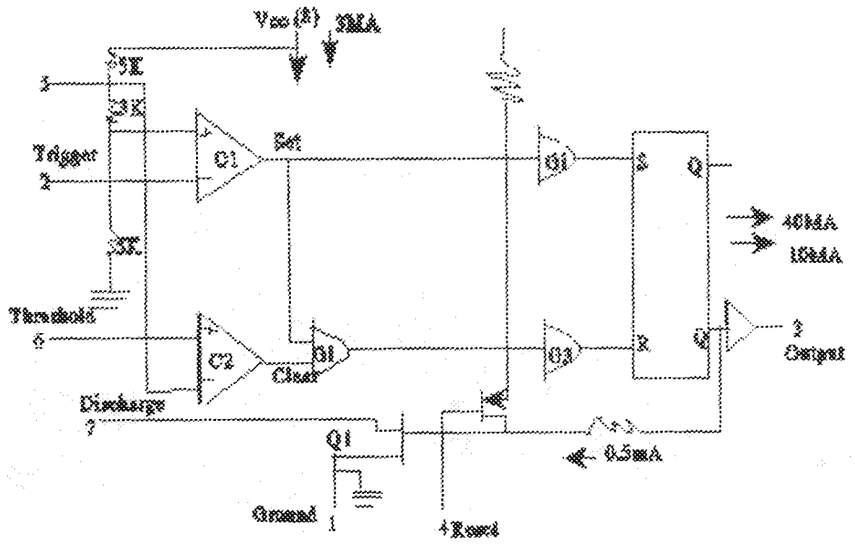


fig. 3.1.4 . The schematic diagram of 555 Timer

3.4.2 THE 555 CONNECTED AS AN MONOSTABLE MULTIVIBRATOR

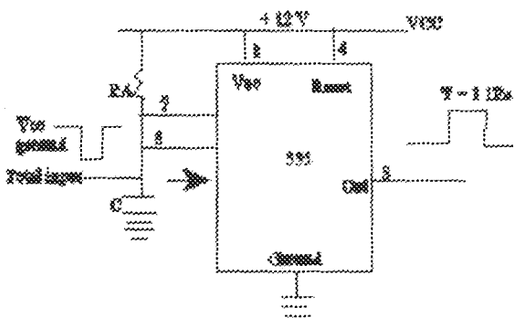


FIG 3.1.5 - 555 Timer used as a monostable multivibrator

3.4.2 OPERATION OF 555 TIMER

The ouput goes high (near vcc) when the 555 recieves a trigger input and it stays there until the threshold input is driven. at which time the output goes low (near ground) and the discharge transistor is turn on. The trigger input is actvated by an input level below 1/3 Vcc and the threshold is activated by an input level above 2/3 Vcc.

When power is applied, the capacitor discharged: so the 555 is triggered, causing the output to go high. the discharge transistor Q1 to turn off, and the capacictor to begin charging toward 12 volts through RA+RB. When it has reached 2/3 vcc, the threshold input is tiggered, causing the output to go low and Q1 to turn on, discharging c toward ground through RB Operation is now cyclic, with C's voltage going between 1/ 3 Vcc and 2/3 Vcc with period T. 0.693 (RA+2RB) C. The output generally used is the square wave at the output.

3.5.0 THE ALARM SECTION

The Alarm section is the special feature of this locking deivce. It consists of four 555 timer chips, a relay and a loud speaker

3.5.1 THE TIMER

Both the schematic diagram and the connection diagram of the 555 timer oscillator has been drawn on the section 3.1. Just as was explain, the 555 timer is a monostable multivibrator generating a periodic pulses whose frequency is determine by the passive components used

The period is given by;

$T = 0.693 (R+2RB) c$

From the relation above it can be seen that the period of the pulse can be adjusted by altering any value of either the resistors or capacitor. Depending on the alarming sound the designer want to obtain, this can be achieved by altering the period of the timer. In my case I achieve nitle telephone pattern with the arrangement shown in the circuit diagram

3.5.2 THE ELECTROMAGNETIC RELAY

Relays are electrically controlled switches. In its operation mode a coil pulls in an armature when sufficient coil current flow. There are many varieties available. The stepping relays are used for telephone switching stations and they are still popular in pinball machines. There are many others especially used in remote switching and high-voltage switching. It work to keep electronic circuits electrically isolated from the ac power line.

In my design for the alarm it controls the sound so that it will be disconnected from the power supply and the alarm will stop.

3.5.3 LOUD SPEAKER

The loud speaker is a device that reponses to the pulses generated by the timer by producing a sound according to the shape of the pulse. The duration is dependent on the period of the pulse.The speaker has an impedance of 8 ohms and has the ability to convert the electrical signal from the timer to accoustic energy in the air.

This speaker has the ability to do this because of the speech coil wound in a cylindrical former which is positioned symmetrically in radial field of a magnet M. A thin cardboard cone D is rigidly attached to the former and loosely connected to a large bauffle board B which surrounds it. When C carries audio frequency current. It vibrates at the same frequency in the direction of its axis. This is due to the force on a current carrying conductor in magnetic field, whose direction is given by fleming's left hand rule. Because the surface area of the cone is large, the large mass of air in contact with it is disturbed and hence a loud sound is produce.

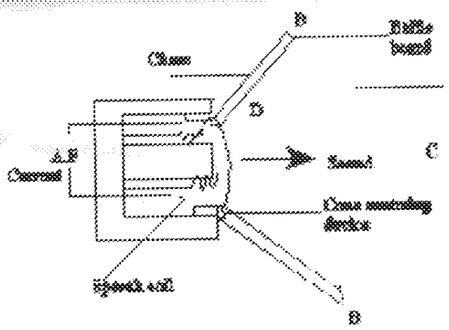


Fig 3.16 The loud speaker

3.6.0 SOLENOID

This is a device which has the ability to be magnetic when a curent passes across it. On the triggering stage of the system, a voltage of 12 volts passes across the solenoid thereby making it to magnetise the appended hook rod. This special ability of the solenoid to magnetise is applied in the locking and unlocking mechanism of the system. This rod perform two distinct functions, it locks the door by the relaxation of the solenoid when in the disable state and it unlocks the door when in enable state by pulling mechanism of the coil.

These two function is performed in a period given by T= 0.693 (Ra+2 RB)C

The power from the output of the 555 timer is ampified by the NPN transistor (D1163A) before getting to the load

The inversion circuit which consist of inversion transistor automatically resets the flip-flop and brings about synchronisation. When this is achieved, the flip-flops are distabled and also the whole device.

In the event of wrong sequence of the keys, the owner can reset the system by pressing the two reset keys provided. However, if the alarm key is pressed, either by act of omission or commission instead of the assigned keys, the result is alarm. By doing this, the device, which is rare ,help check the rate of intrusion.

CHAPTER FOUR: CONSTRUCTION, TESTING AND RESULTS

4.0 SYSTEM CONSTRUCTION

First, the project was carried out on a breadboard because it offers temporary and solderless connection of circuit components with the aid of the circuit diagram. Its distinct flexibity gives room for easy correction of mistakes made in the course of components connection.

The connection in the breadborad, in accordance with modern technique is done in modules. On connection of each part, it is tested stage by stage to affirm its workability before transfering to the veroboard for final soldering. The verobard is electrical conductive board which is arrange in lines of the same potential and seperated from other lines of different potential by a gap. Tested circuits in breadboard are transfered to veroboard for onward soldering.

The first module on the veroboard is the power supply unit which supplies power to the diferent units of the system. All the appropriate connection of the power unit components are made and is finally tested to check its confirmity to the expected result. As this is certified, I went ahead to solder the alarm units and as stated before, the same procedure was followed and the final testing was done to attest its workability. I was very careful in ensuring that the i.c did not breakdown due to excessive heat from the soldering iron. The same procedure was followed in the rest modules such as the timer section, the key pad etc. I used IC sockets for the ICS easy fixing and unfixing. Again, one IC was not handy during the construction and its space was provided by using I.C socket. The space for the solenoid was provided because it was available during the time of initial construction.

The door used here is made from wood and the dimensions is as shown fig 4.1

4.1.0 TESTING

When all the necessary connection has been concluded, the system was then tested. The relay in the alarm unit automatically magnetise as soon as the alarm keys are depressed. This was followed by a sound from the loudspeaker indicating danger and the perfect harmony of the system. Again, the keys for the operation of the system was equally effected and as expected, there was magnetising ability of the solenoid which reflected its capacity to lock and unlock the key.

The totality of the outcome seen above proves the harmonization and agreement of the theoritical work with practical exhibition.

4.2.0 THE RESULT

INPUT					OUTPUT		
CL	L	K	S	R	Q	Q	Q
√	1	X	O	O	O	1	O
√	X	O	O	O	1	1	O
√	O	X	O	O	O	O	1
√	X	1	O	O	1	O	1
√	X	X	O	O	X		
X	X	X	1	O	X	1	O
X	X	X	O	1	X	O	1
X	X	X	1	1	X	1	1

1= HIGH LEVEL

O= LOW LEVEL

⌂= LEVEL CHANGE

X= DON'T CARE

4.2.1 DISCUSSION OF RESULT

From the values in the result it could be seen that the output is high when the j input is high and K input don't care what its input is about. This is exactly at the stage at which this project has been designed and constructed. When the clock input is at the edge at the positive going transition of the clock pulses, that is, the period the output is one . This is illustrated in the table above. It can also be observed from the table above that the set or reset is independent of the clock and this can be accompanished by high level on the respective input.

Finally, the inputs can be adjusted to give a desired output as can be seen from the table of result.

4.3.0 THE WOOD CASING

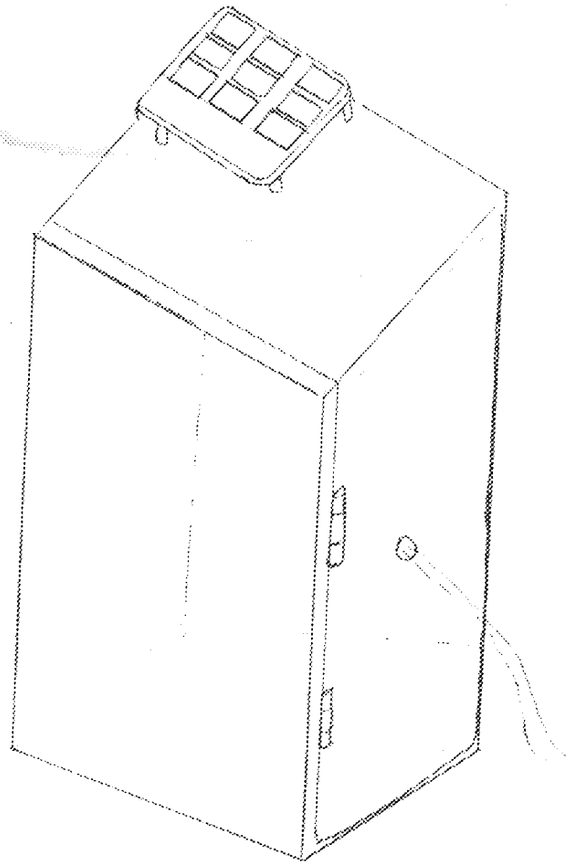
To realise the project, I use Iroko wood with the dimension given below.Any other kind of wood can be used. The block here represent the block wall or steel surroundings of a save or any

other thing that can be used for the purpose for which the project has been based. The wooden door here is hinged to the body of the casing by a hing connector which allows the door to be opened freely and closed freely with the least resistance. The different parts of the box is joined to one another with a nail to form the rectangular shape.

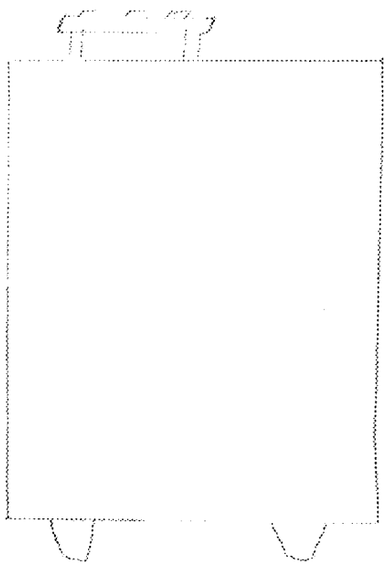
The diagram of the prototype is shown in the next page.

4.4.0 ASSEMBLING OF THE PROJECT.

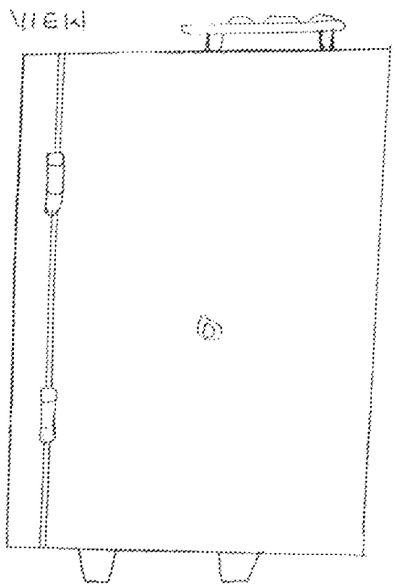
The whole project is packaged in a small wooden box with the key pad on the top of the box while the power cord is brought out ready to be pluged-in in a power socket. The circuit verobard is screwed to the box with screw nails.



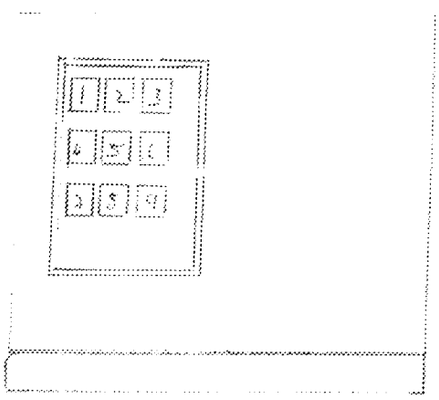
FRONT VIEW

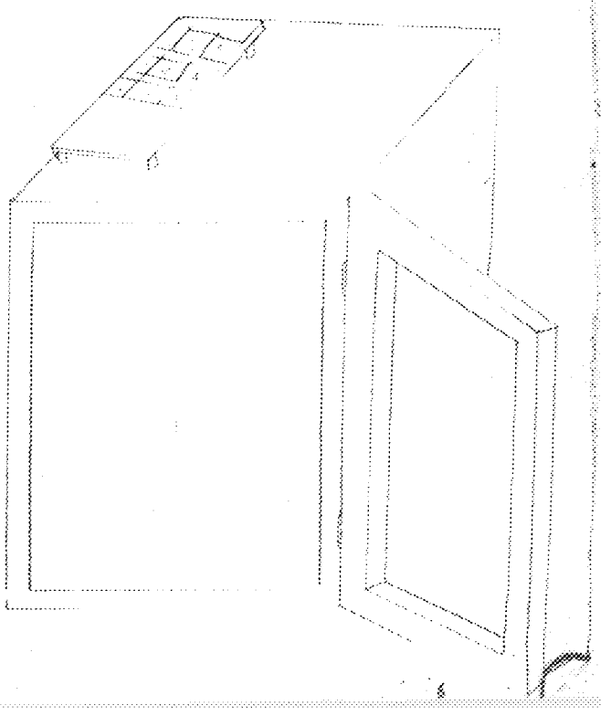


SIDE VIEW



PLAN VIEW





LENGTH — 18.00 cm

BREADTH — 14.00 cm

HEIGHT — 26.50 cm

fig 6.1

CHAPTER FIVE: CONCLUSION, APPLICATION, RELIABILITYAND RECOMMENDATION

CONCLUSION

This project has been designed based on the existing theories relating to digital system which has been acquired in my course of study over the years. It is a project aim at curbing and reducing the incidence of crime in the society.

The memory section is designed with J,K master slave flip-flop which has the ability to record and preserve not only the immedate signal at the input but also the internal state of the flip-flop. By so doing it is able to hold data till the flip-flops from which the project is designed are impressed. This effect the locking and unlocking mechanism via the auming gate

The design sophistication meets an acceptable standard and can be compared to existing project in all ramification. Furthermore, the availability of materials used and lowcost expended in the realization and construction of the device is an advantagous factor in the economy of its production. The electronic companies in Nigeria should capitalise on the vital and enssential low cost of this project to embark on its mass production

However, this project has limitations and therefore open to critism and investigation. I was unable to realise lock and unlocking the device with different set of digit numbers conbination and I will urge future designers to research more on it. If investigation and critism is done without sentiments, Nigeria will have unprecedented height in the field of technological development.

5.2.0 APPLICATION AND RELIABILITY OF THE DEVICE

5.2.1 APPLICATION

This project can find its usefulness in:

1. Bank vault for safequiding the contents of the vault.
2. It can be used in industries were high degree of safety is in demand
3. It can be used in minting and printing companies for security purposes.
4. It can be used in security houses.
5. It can be used in private homes for the safety of lives and properities.

5.2.2 RELIABILITY AND FEATURES OF THE DEVICE.

The probability that this design will perform under stated conditions for a given period of time is a function of the system reliability. In any case, every component of the design has enjoyed the manufactures reliability on the ic manufacture. The reliability of these integrated circuit in the project has increased the overall reliability of the design.

The following precaution should be taken when dealing with the device.

(I) It should not be subjected to extreme temperature, high humidity and too much dust can cause high failure rate.

(ii) Severity of handling and carelessness of use will endanger the device and consequently exposes it to high failure rate and reduce reliability.

(iii) Both amplitude and frequence vibration has been taken care of and therefore it should not be subjected to any form of vibration.

(iv) Failure should be taken to a qualified technician .

RECOMMENDATION

For further pursuant in the development f the project. I will table down the following recommendation for the intervested students:

- the keys used for this project are only eight and this can be improved to accomadate more key especialy the fool prove keys.
- the project can only lock and unlock with the same type of key but can also be hareness to lock and unlock with different keys as the users desire.
- The project is realised with separate inverter circuit but can be done to include an incoraperated inverted at the NAND gate i.c
- I designed my alarm circuit with more 555 timers ic and believe it can be done with reduced number of 555 timers i.cs.

The loudnesss of the alarm can be increased by amplifing the signal at the loud speaker end.

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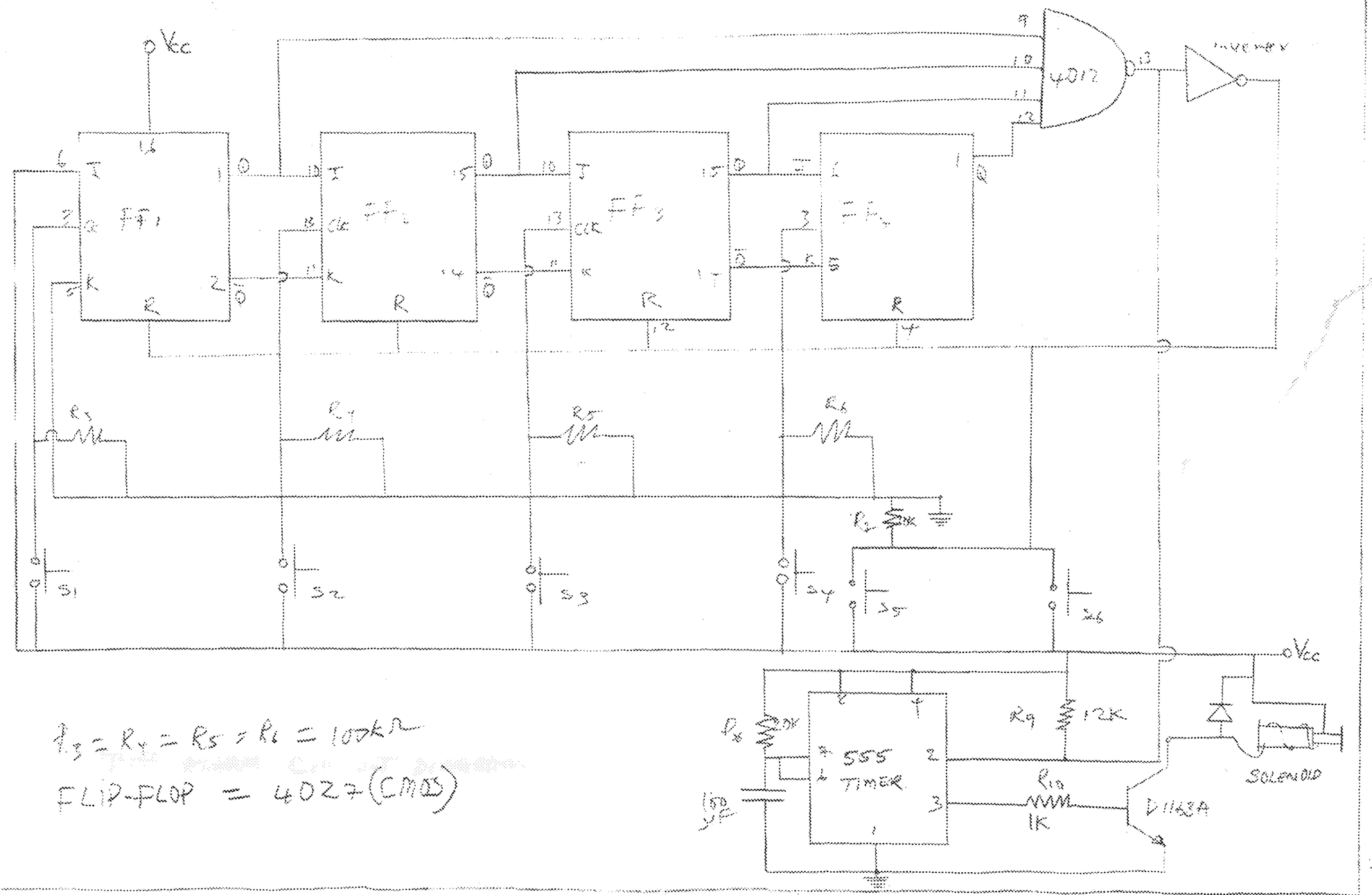
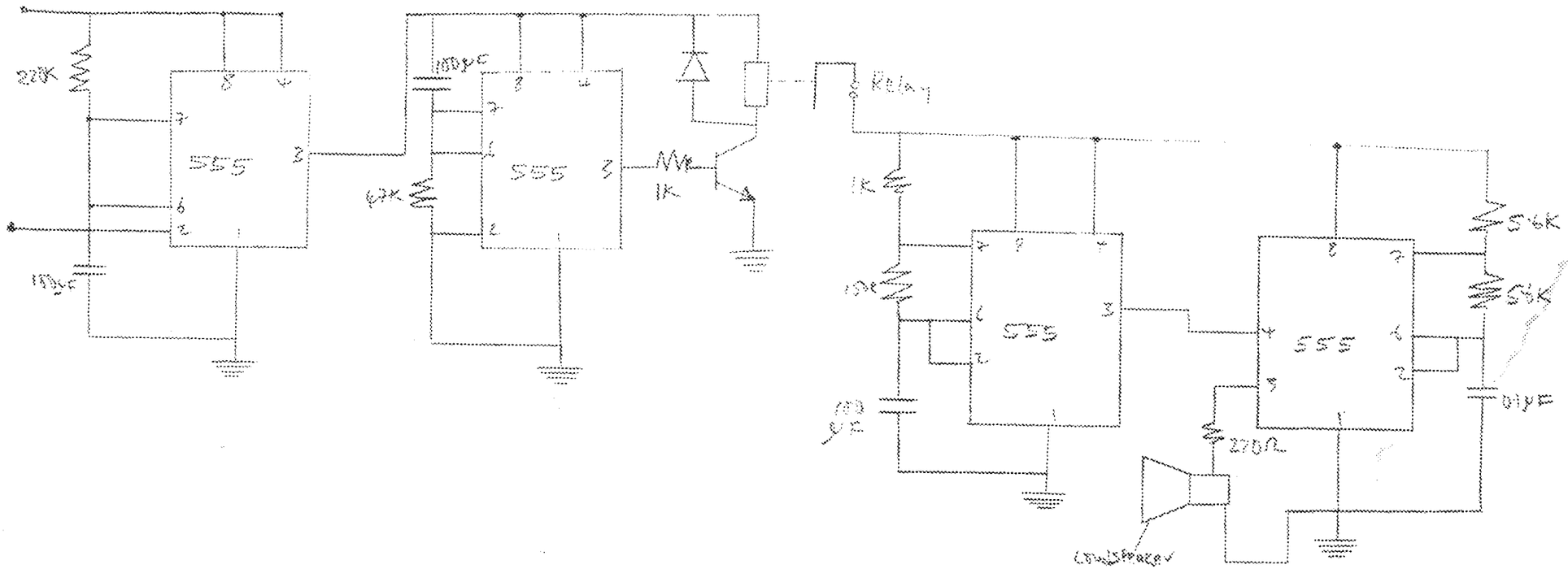


$R_1 = R_2 = R_3 = R_4 = 10k\Omega$

FLIP-FLOP = 4027 (CMOS)



THE ALARM CIRCUIT DIAGRAM