DESIGN AND CONSTRUCTION OF AN ELECTRONIC DICE

BY

OOYE BENJAMIN OLUWASEMILORE

MATRICULATION NO. 2000/9907EE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

SCHOOL OF ENGINEERING AND EGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY MINNA NIGER STATE.

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF BARCHELOR OF ENGINEERING DEGREE B.ENG IN ELECTRICAL AND COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY. FEDERAL UNIVERSITY OF TECHNOLOGY MINNA NIGER STATE

OCTOBER 2006.

DEDICATION

This project work is dedicated to Almighty God for his grace and the knowledge he has granted me to design this project. I also dedicate it to my loving parent Rev and Mrs Nathaniel Idowu Ooye.

DECLARATION

I Ooye Benjamin Oluwasemilore hereby declare that this work was done by me and has never been presented elsewhere for the award of a degree. I also hereby relinquish the copyright to the Federal University of Technology Minna.

Ooye Benjamin Oluwasemilore
....
(Name Of Student)

....
(Signature & Date)

Mr. O.D. Ahmed
....
(Name Of Supervisor)

....
(Signature & Date)

Engr. M.D. Abdulahi
....
(Name Of H.O.D)

....
(Signature & Date)

....
(Name Of External Examiner)

....
(Signature & Date)

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With humble mind and sincere heart, I express my gratitude to Almighty God for having preserved my life till date and for giving me wisdom to work on this project.

Things don't just happen they are made to happen. Sincerely certain people have made it happen in my life and I would not fail to acknowledge and appreciate them.

I am greatly indebted to my supervisor, Mr. O.D. Ahmed who not only encourages but was also there to check my manuscript with great perseverance. I am indeed grateful to my parent Rev. and Mrs N.I Ooye for their love, advice, financial and moral support. Also am pleased to thank my HOD, Engr. M.D. Abdullahi for his advice and directions.

My gratitude also goes to my lecturers. I am especially grateful to my siblings: Steve and Boluwatife for their love, encouragement, and sincere wish, for the success of this project. I wish to express my deep gratitude to my friends: Ogunbiyi Omotayo (Senator O.O), Adedoyin Temitayo for their help and support .My gratitude also goes to every body who participated in one way or the other to the successful accomplishment of this project

ABSTRACT

The project is concerned with the design and construction of an electronic dice. The olden day's equipment has been modified due to improvement in modern day's technology. This project: design and construction of an electronic dice, can be used to represent some numbers from one – six which are used to display the numbers of dice. An up/down counter was used which is incorporated into the frequency generator or monostable multivibrator.

This project comprises of four sections: the frequency generation, the counting section, the decoder as well as the display section.

Calculations were carried out in order to achieve the desired frequencies and values for effective design of this project.

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CHAPTER ONE

1.0 INTRODUCTION

Role playing and simulation games have introduced dice in non-cubic shapes, but the traditional spotted cube has endured the test of time. In fact, dice are credited by several historians as the oldest gambling device invented by man [11]. I would like to take some time to give the humble cube another more detailed look.

For many years now, the game of dice has been a popular hobby. Therefore, people have devised different way of using the substance dice to play games. Some use it for gambling, by throwing it up and expecting the highest number to show up when it landed on an agreed surface. Other uses it to play the popular ludo game, and many more. Another very interesting use of dic is its use in the "guess the number game".

This project is about the electronic dice. The rolling dice as we know has to be casted whereas an electronic dice is controlled by a switch. There is a provision for LED's, which keep on flickering for the particular counts, and when the switch is released the corresponding number counts are aye. The count displayed may be of the numbers one, two, three, four, five or six.

1.1 AIMS AND OBJECTIVES

It is a great delight to put to all that have been thought by lecturers into practical application to realize a useful working system such as this designed system. Design procedures are used in designing many devices and systems in the field of electronics. This project exposes the details of the top down design methodology.

It is aimed at providing the fundamental knowledge required to design digital system using digital electronic integrated circuits as the fundamental elements.

Hence the aim of this project is to design a system that can save energy, limit the vigorous shaking of a dice in a cup when you play a dice game and also provide an electronic dice that will affordable to many if not all the hobbyist.

1.2 SCOPE / METHODOLOGY OF THE PROJECT

The electronic dice is implemented by using frequency oscillator, preloadeable counter, decoder/driver, seven segment display and logical circuit to display numbers from on through six randomly.

This project consists of five chapters. The first chapter gives an introduction to the project topic and the scope of the project. The second chapter deals with the necessary theoretical background, brief historical background and previous works of others on dice.

The third chapter deals with analysis and design of individual modules, which make up the electronic dice. While chapter four give the construction techniques, and step by step testing of each of the modules that make up the overall circuit. The last chapter contains the construction and recommendations.

CHAPTER TWO

2.0 LITERATURE REVIEW

Out of all possible games that are play today, dice game remains the oldest and surprisingly the most popular type of game available. Dice game data back thousands of years, while most other gambling games were developed in the mid- 18^{th} century and onward [11, 9].

Dice game can be quite simple or they can be complicated, yet dice games are still some of the most exciting games available to play.

2.1 ANCIENT TIME DIE

In an ancient time the throw of dice was not just considered to be luck, the outcome was believed to be controlled by the gods and casting dice was a way of dividing inheritance, chosen ruler and a method of prediction

Before standard cubical dice became common ancient people would use fruit, stone, and set of flat sticks, sea shells, nut shells and pebbles to get random result from games [11]. Animal ankle bones were the next step in the evolution of dice, the Greek and Romans used sheep ankle bones as well as the more developed cubical spotted dice. The Romans called the four – sided ankle bones Tali and the standard six – sided dice Tesserae [11].

2.2 PRESENT DAY DIE

In the recent time, it is not surprisingly that there are several different types of dice that can be used to play variety of different dice game that are available today. Although these are special types of dice available, most people chose to play with either standard dice or casino dice which both of these types of device may look the same.

2.3 STANDARD DIE

Standard dice are the type of dice that suit most people's needs. These dice are shaped like a cub with six sides and each side labelled with one to six dots. As part of being a regular dice, all opposing sides of the die should add up to seven [9].

2.4 POLYHEDRAL DIE

Polyhedral dice are dice with more or fewer than six sides; they are usually made of plastics, wooden and semi precious stones. Early polyhedral dice from the 1970s and 1980s were made of soft plastics that would easily wear as the dies were used [12].

Typical wear and tear would gradually round the corners and edges of the dice until it was unstable. Modern polyhedral dice are typically made of high- impact plastic and can withstand years of use without visible wear.

2.5 ELECTRIC DIE

This type of die is metallic one side or have metal slugs in the spots on one side. These are used with an electromagnet under the playing surface. Greedy Chuck, a luck operators sometimes use them under the counter or chuck cage and special craps tables where manufactured to incorporate the magnet [12,9,11].

Electric dice are not as commonly used as they once where due to the fact that many dice players carried a magnet to test for them. If a die is stick to a magnet then without doubt it is crooked.

2.6 ELECTRONIC DIE

Further modifications on the primitive system of playing the game led to the development of several of game of chance. One of these versions is the electronic dice game that is played till date.

The electronic dice eliminates all the problems and disadvantages encounter by the ancient dice and it has a high degree of accuracy, less power consumption and very cheap. With the advent of electronic components such as MSI devices, design and construction of electronic game become a matter of concern to many engineers. This resulted in the development of many versions of electronic games such as computer games and all other types of electronic game.

Electronic dice is one of the tremendous achievements of engineer over recent years that allow indoor recreation at most convenient time and conducive atmosphere or environment.

CHAPTER THREE

3.0 DESIGN AND IMPLEMENTATION

3.1 OPERATING PRINCIPLE OF THE ELECTONIC DICE

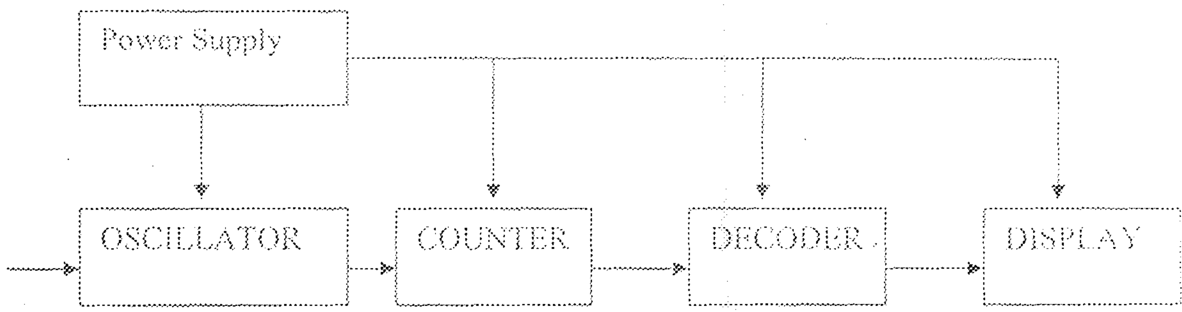


Fig 3.0 Block diagram of an electronic dice

The most basic representation of an electronic dice is shown in the above figure 3.0.The electronic dice is based on the principle that a random number is not generated by using a CMOS three – input NOR gate as an oscillator, the frequency being determine by R4 and C2, R5 and C3 respectively. The value chosen causes an oscillation at about 40 KHz and 90 KHz. The output (on pin 6) goes to IC2 a preloadable counter.

Each time the signal from the oscillator changes from low to high level, the counter increments by 1. The number appears on pin 6, 11, 14 and 2 as a binary number Output 2, the most significant bit, is connected to the prowied input goes high, the number represented by pin 4, 12, 13 and 3 are loaded into the counter. These pins are wired as binary number 0001

As a result, the counter will count 1(=0001), 2 (=0010), 3(=0011), 4(=0100), 5(=1010), 6(=0110). The next signal from the oscillator will cause it to count to 7(=0111), but this causes pin 2 to go high which immediately preloads the (0001) into the counter again. The binary number from IC2 goes to IC3 which decodes it into the six (6)

3.2 CMOS LOGIC FAMILY

For the purpose of this project all the ICs used belong to the CMOS logic family. Complementary metal - oxide semi conductor is another common integrated circuit technology which uses the MOSFET as its basic element and is called complementary MOS logic. The phrase "metal - oxide semiconductor" is a reference to the nature of the fabrication process originally used to build CMOS chips. This process created field effect transistors having metal gate electrode placed on top of an oxide insulators, which in turn is on top of a semi conductor material.

Instead of metal today, the gate electrodes are almost always made from a different material, polysilicon but the name CMOS nevertheless continues to be used. CMOS is selected for use in this project due to the following advantages:

1 Consumes little power and were perfect for battery operated electronic device.

2 High noise immunity

3 It is readily available in market

4 Moderate cost.

3.3 THE PULSE GENERATOR MODULE

The main clock pulse generator used in this project is basically the HEF 4025B IC, which provides a periodic waveform that, serves as a synchronizing signal for the overall system of the electronic dice. The HEF4025B is a CMOS compatible IC, it is basically a switching circuit that has two distinct output level LOW or HIGH logic level. A single narrow trigger pulse produces a single output pulse whose time duration is controlled by RC time constant.

Two HEF 4025B were used in this project, both were performing the same function of generating a clock wave from though at different frequencies. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

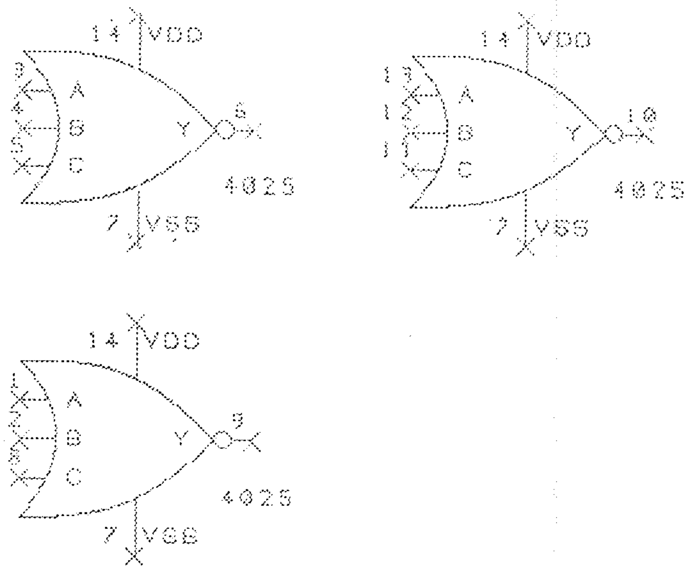


FIGURE 3.3 LOGIC DIAGRAM FOR HEF 4025B [7]

Table 3.3 3-input NOR gate truth table

Input C	Input B	Input A	Output Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

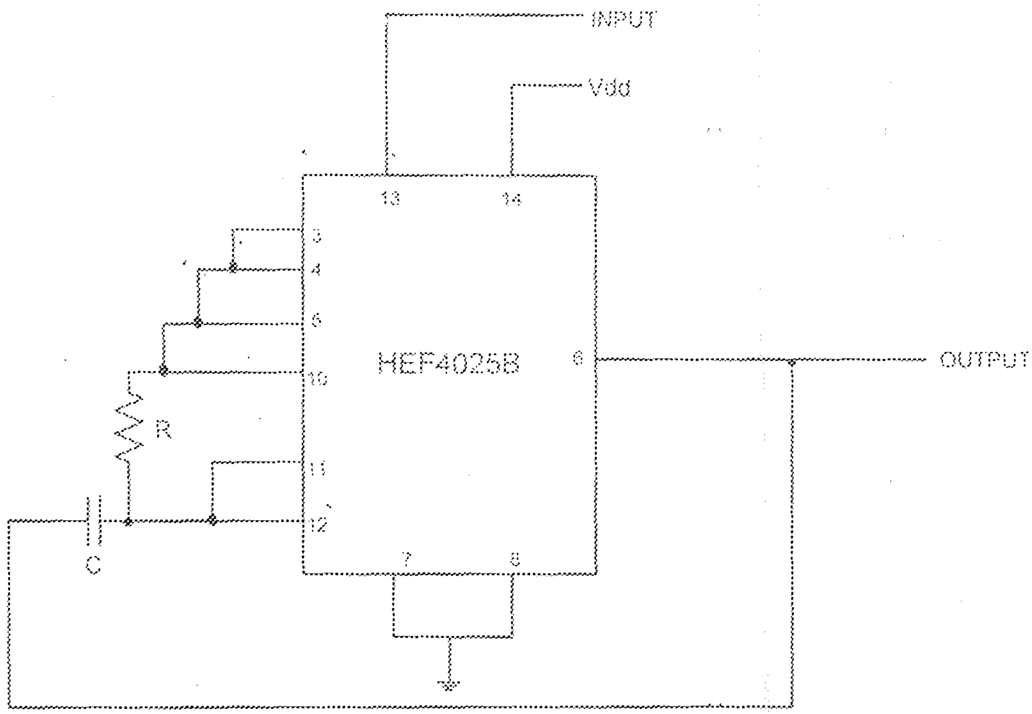


Fig 3.3b: Pin Layout and Configuration for HEF 4025B [10]

3.4 CLOCK FREQUENCY CALCULATION

The frequency formula for HEF 4025B output is given by:

Frequency (F) = 1/ Period (T)

While period (T) = 1.1 RC

To obtain frequency of 40 KHz

C = 220pf, R = 100K

This implies: T = 1.1 RC = 1.1 (100 x 103 x 220 x 10^-12)

T = 2.42 x 10^-5

Freq (F) = 1/T 1/ 2.42 x 10^-5 = 41.32 KHz

To obtain frequency of 90 KHz

C = 100pf, R = 100K

To obtain frequency of 90 KHz:

C = 100pf, R = 100K

Period (T) = 1.1 RC , = 1.1 (100 x 10^3 x 100 x 10^-2)

= 1.1 x 10^-5

Freq (F) = 1/ T 1/ 1.1 x 10^-5 = 90.90 KHz.

3.5 THE COUNTING MODULE

One of the most useful and versatile subsystems in a digital system is a counter, a counter been driven by a clock is used to count the number of clock cycles since the clock pluses occur at known intervals as well as generating numbers. There are basically two different types of counters, the synchronous and the asynchronous counters.

In this project I will explore the capabilities and operation of the type CD4029BC CMOS counter IC which is a synchronous counter and capable of counting up and down and in either decimal or binary mode. It can also be preset with any initial count, and it's designed so that multiple 4029 ICs can be cascaded and still maintain fully synchronous counting either up or down.

The CD4029B is a three (3) bit synchronous counter s, when the binary / decimal input is at logic "1" the counter counts in binary, otherwise it counts in decimals. Similarly, the counter counts up when up / down input is at logic "1" and vice versa.
Logic '1' preset enable signal which allow information at 'jam' input to preset the counter to any state. The counter is advanced one (1) count at the positive- going edge of the clock if the carry in and preset enable inputs are at logical '0'. Advancement is inhibited when either or both of these two input is at logical '1'. The carry out signal is normally at logical '1' state and goes to logical '0' state when the counter reaches it's maximum count in the 'UP' mode or minimum count in the 'DOWN' mode provided that

the carry input is at logical '0' state. All inputs are protected against static discharge by diode damps to both Vdd and Vss.

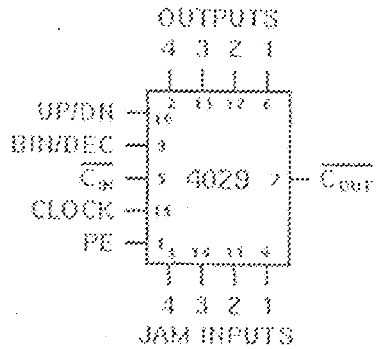


Fig 3.3 Functional Diagram of 4029 [7]

The internal schematic diagram of the 4029 is quite complex, as it involves a gating structure that will allow counting up or down, in binary or decimal, and with parallel inputs to preset a count. However, we can't reach the internal circuitry in any case, so the functional diagram is far more useful for our purposes.

The up/down input, for example, tells the counter to count up if it is a logic 1, or down when it is logic 0. In the same way, logic 1 to the binary/decimal input causes the counter to operate in binary mode, while logic 0 switches it to decimal (sometimes called *decade*) mode. If multiple 4029s are cascaded for a larger count, all up/down pins are connected together and driven from a common signal, as are all bin/dec lines.

The C_{IN} and C_{OUT} lines form the means of cascading counters and still keeping a fully synchronous count. If C_{IN} is logic 1, the counter won't count at all When C_{IN} goes to logic 0, the counter operates normally. Then, when the counter reaches its terminal count (9, 15, or 0 depending on the states of up/dn and bin/dec),

C_{OUT} goes to logic 0. This is connected to the C_{IN} line of the next IC to allow the next higher order of magnitude to count once. Then C_{OUT} goes to logic 1 again. The first counter IC in the set, representing the least significant digit, has its C_{IN} line grounded to logic 0 so it will always count.

The clock input, like up/dn and bin/dec, is fed to all 4029s in an extended counter circuit. This is the signal that represents whatever is to be counted. Any 4029 that is enabled by having its C_{IN} line at logic 0 will change state to the next count when the clock rises from logic 0 to logic 1. Any changes to the C_{IN} and C_{OUT} lines will occur just after that rising edge, and so will be ready for the next clock pulse.

The pe input is the preset enable line, and is also shared with all 4029s in the counting set. When this line is logic 0, the counter operates normally. However, when pe becomes logic 1, the logic signals present on the four jam input lines get copied directly to the four bits of the counter, overriding any prior count. These inputs are not always used, and many applications ignore them. However, there are some applications that do use these inputs to advantage. For example, if we want to count for a multi-digit interval in seconds, we can set the jam inputs to the decimal number of seconds to be counted and configure the circuit to count down. When the counter reaches zero, the final C_{OUT} line falls to logic 0 and can be used after inversion to preset the count again to the selected number, or to stop the count and signal the end of the timing interval.

The four outputs, of course, are the current count as either a binary or BCD number, depending on the state of bin/dec. Output 1, often designated Q1, is the

Least Significant Bit (LSB), while output 4 (or Q4) is the Most Significant Bit (MSB).

All inputs and outputs are standard CMOS design, and operate in the normal manner for CMOS ICs.

3.6 FEATURES OF CD4029B

1. Wide supply voltage range (3 – 15v)
2. High noise immunity
3. Low power
4. Parallel jam input
5. Binary or BCD decade up/down counting
6. Fan out of 2 driving 74L or 1 driving 74Ls.

3.7 THREE BIT UP/DOWN SYNCHRONOUS COUNTER

Describing the working principle of three bit up/ down synchronous counter, which advances upward through it sequence (0,1,2,3,4,5,6,7) and then can be reversed so that it goes through the sequence in the opposite direction (7,6,5,4,3,2,1,0) is an illustration of up/down sequential operation.

In general, most up/down counters can be reversed at any point in their sequence. For instance, three bit binary counter mentioned can be made to go through the following sequence. 0,1,2,3,4,5 4,3,2. 3,4,5,6,7, 6,5.e.t.c.

TABLE 3.7 TRUTH TABLR FOR 3 – BIT UP/DOWN COUNTER

CLOCK PULSE	UP	QA QB QC	DOWN
0		0 0 0	
1		0 0 1	
2		0 1 0	
3		0 1 1	
4		1 0 0	
5		1 0 1	
6		1 1 0	
7		1 1 1	

The table above shows the complete up/down sequence for a three bit binary counter. The arrows indicate the state – to – state movement of the counter for both its down mode of operation. An examination of QA for both the up and down sequence shows that FFA is on each clock pulse. So the J and K input of FFA are

$$JA = KA = 1$$

For the up sequence, Qb changes state on the next clock pulse when QA = 1. For the down sequence, Qb changes on the next clock pulse when QA = 0.

Thus, the J and K inputs of FFB must equal 1 under the conditions expressed by the following equation.

$$JB = KB = QA.DOWN$$

For the UP sequence, QC changes states on the next clock pulse when

$$QA = QB = 0.$$

Thus the J and K inputs of FFC must equal 1 under the condition expressed by the following equation:

$$JC = KC\ QA\ .\ QB\ .\ UP + QA\ .\ QB\ .\ DOWN$$

Each conditions for the J and K inputs of each flip flop produces a toggle at the appropriate points in the counter sequence.

The figure below show a basic implementation of a three bit up/down binary counter using the logic equations just developed for the J and K inputs of each flip – flop. The UP/DOWN control input is HIGH for UP and LOW for DOWN [5].

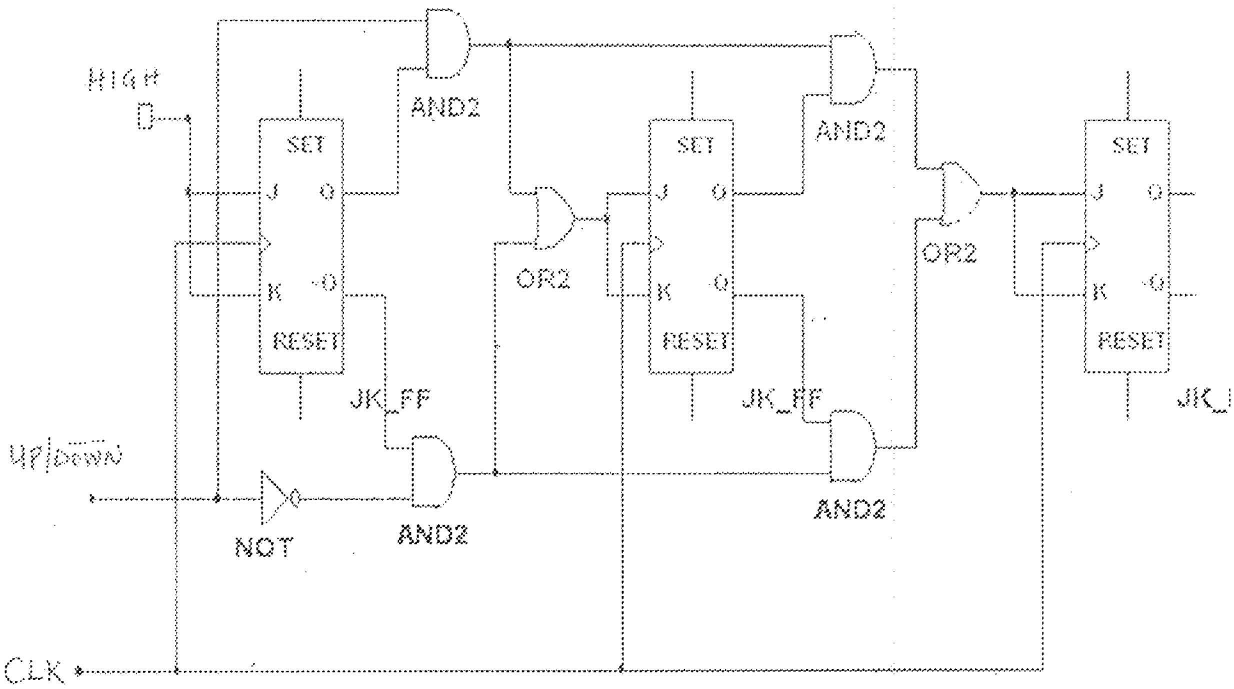


Figure3.7 Basic circuitry of three bit Up/Down Synchronous Counter

3.8 THE DECODER MODULE

In digital electronics, all operations are carried out in binary form. The information at the output of the counter are in binary form therefore, it is necessary to find a way of converting this information in binary to form suitable for man to interpret and a circuit required for this purpose is known as a "DECODER".

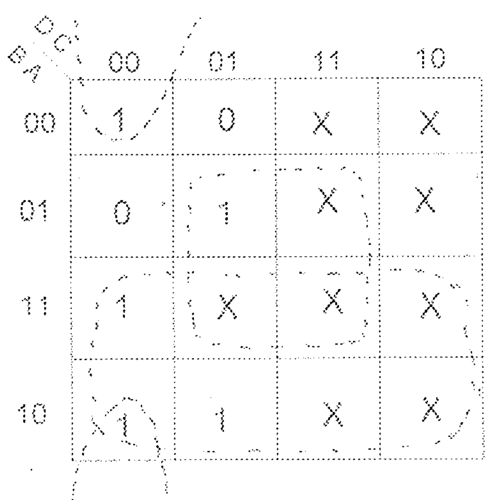
For this purpose of this project a special decoder known as BCD – to seven segment decoder/ driver is used because of it ability to accepts 'n ' input lines of the BCD code on it's input and provide maximum of 2^n unique outputs lines to energize seven – segment display device in order to produce a decimal read-out.

3.9 SEVEN SEGMENT DECODER

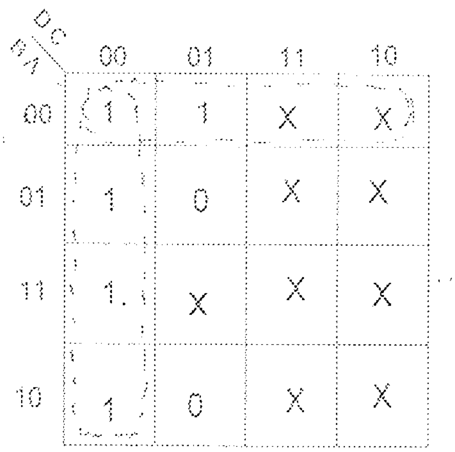
TABLE 3.9 Truth Table For The Seven Segment Driver.

	INPUTS				SEGMENT						
	QD	QC	QB	QA	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	X	x	x	x	x	x	x
8	1	0	0	0	X	x	x	x	x	x	x
9	1	0	0	1	X	x	x	x	x	x	x

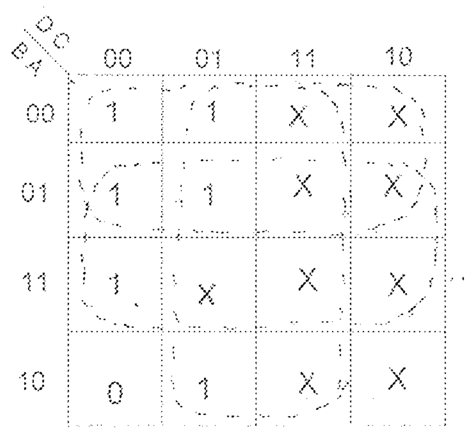
Table 3.9b: K – Map for the seven segment decoder



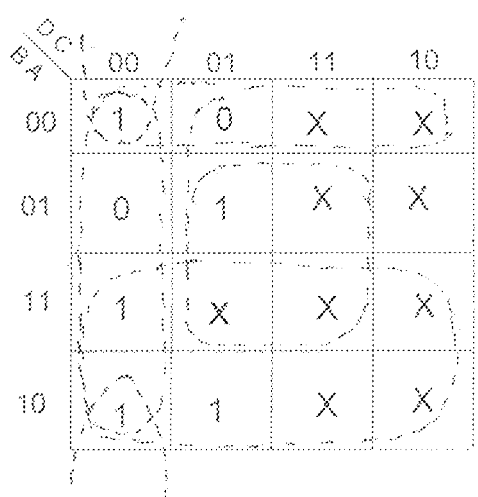
$a = \overline{DCA} + CA + B$



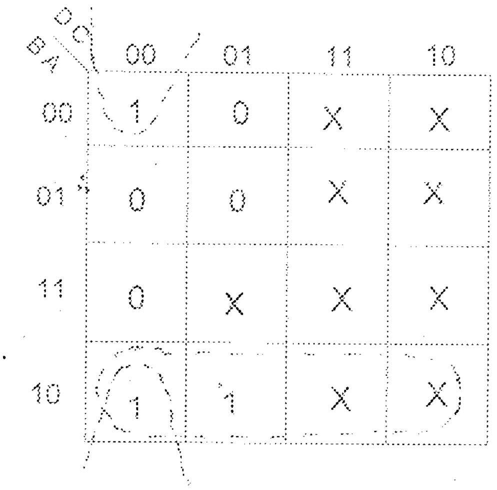
$b = \overline{DC} + \overline{BA}$



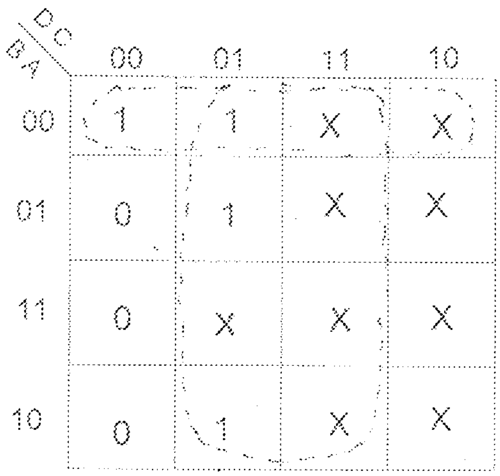
$c = \overline{B} + A + C$



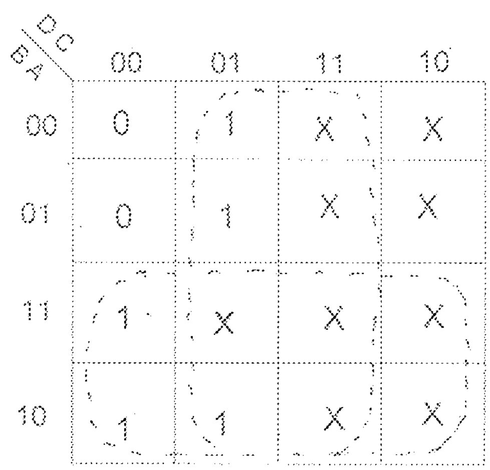
$d = \overline{D}\,\overline{C}\,\overline{A} + CA + B$



$e = \overline{DCA} + BA$



$f = \overline{BA} + C$



$g = C + B$

3.10 CHOICE OF DECODER/DRIVER IC [CD4511BC]

As it can be seen in figure 3.4.1b if one is to implement this circuit using single scale integrated circuit, the number of components required is enormous. For example, this project required two seven segment decoders. If two of such circuit are to be implemented at the end of the day, the cost of production would be very high. Therefore, it would be wiser to go for circuit that are less costly and most effective and such circuit comes in a medium scale integrated circuit. e.g. CD4511CB. It is a decoder/driver used to drive a seven segment display in this project.

A CD4511CB is a CMOS-chip which is able to take a binary signal in, and use it to display a number on a seven segment display. This chip has the ability to drive a standard display, which is why it is termed a "driver". This device accepts a digital number signal and sends a high and low value to each of the seven segments on the display.

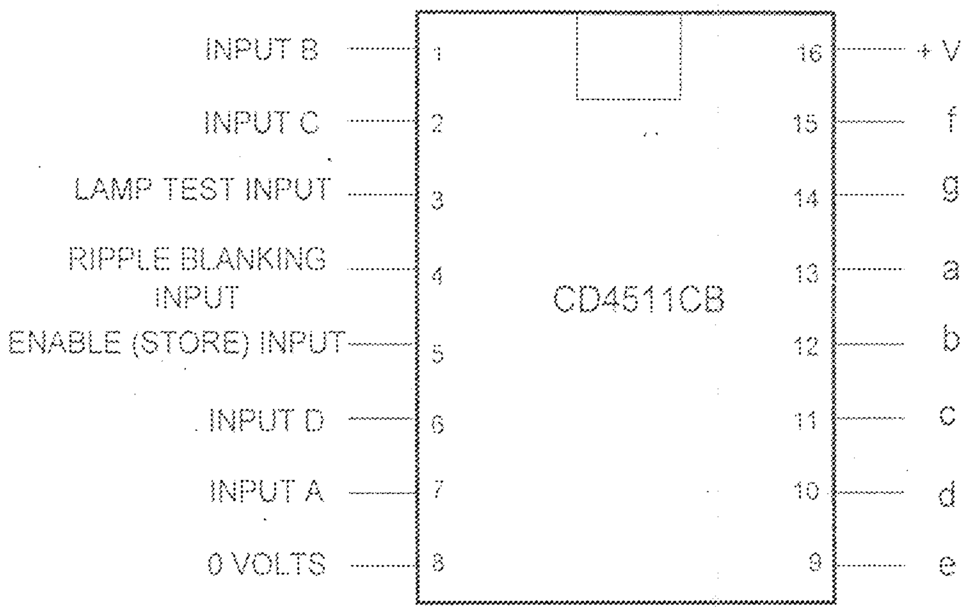


Fig 3.10 A Seven segment Decoder IC [7]

The figure shown above is a 4 – to – 7 line decoder. It has four data input lines i.e. A, B, C, D, and seven active high outputs. a, b, c, d, e, f, g. if a binary six i.e. D = 0, C = 1, B = 1, A = 0 are present at the data inputs the output a, b, c, d, e, f, g would be at active High state since the display used in this project is a common – cathode, only the segment to which these outputs are connected (a, b, c, d, e, f, g) are turned ON, therefore a decimal six is then displayed.

3.11 BASIC OPERATION OF CD4511CB

When the lamp test input pin 3 is made Low, all the segment output go HIGH regardless of all other input conditions, with lamp test HIGH, if the ripple blanking input pin 4 is made Low, all the segment output are forced Low. This input can be used to blank leading zeros in a multi – digit display.

The enable input controls the action of a 4 – bit latch inside the 4511, with enable Low, the output of the latch follow the logic states of the BCD inputs and the seven segment output change accordingly. If the enable is made High, the logic state present on the BCD inputs are stored. The seven segment outputs remain unchanged until enable is made Low once more. This action allows the display to be update at intervals.

3.12 DIGITAL DISPLAY MODULE

The display employed in this project is the seven segment display which is widely used as a read out for modern digital equipment. There are three types of seven segment display. These are:

1 Light emitting diode. (LED)

2 Liquid crystal display (LCD)

3 Gas discharge display (GDD)

However, the seven segment indicator in this project are basically Red light emitting diodes (LED) constructed on a Vero board in a geometrical pattern.

depicting the shape of decimal numbers from 0-9 depending on which segment is selectively illuminated as shown in the figure below. The LED is chosen, because it was cheap and available in the market.

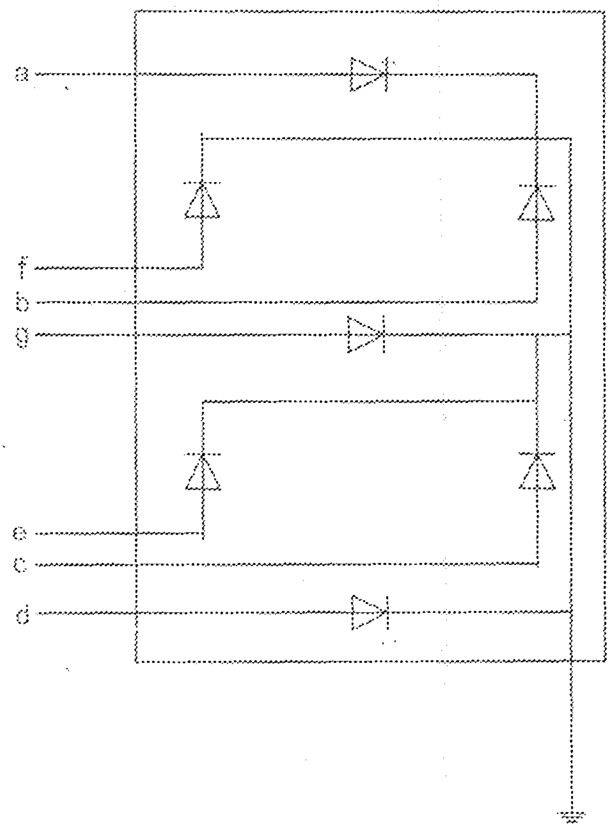


Figure 3.12a Common cathode seven segment connections.

The LED seven segments is a common- cathode display in which all cathodes are connected while the anodes are independent as shown in figure 3.0. To operate the LED display, all cathode terminals must be connected to the positive voltage supply. The current flowing through each diode must be limited to about 17mA which is the maximum amount of current that must pass through each diode for safety. Therefore, in order to prevent current passing through these diodes, as current limiting resistor must be introduced in series with each diode at their respective cathode, as shown below.

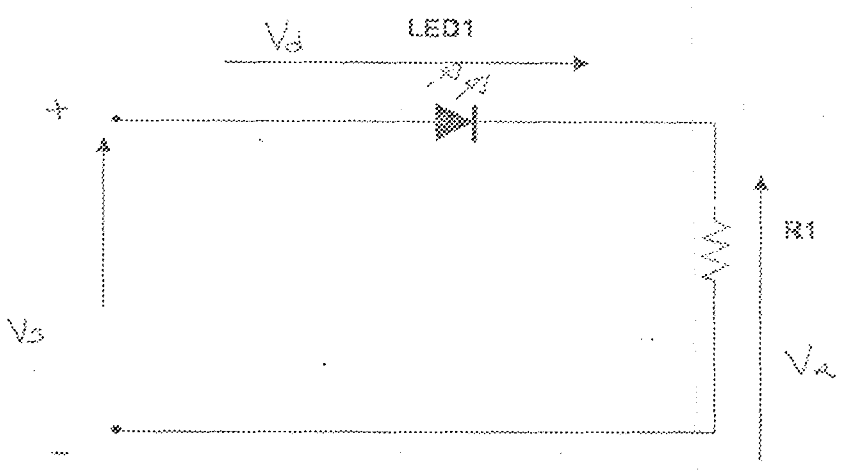


Fig 3.12b Limiting Resistor

The range of value of voltage drop in the diode is $1.0 \leq VD \leq 3.0$, where supply voltage is 9v.

The limiting resistor value = VR/ Id = Vs - Vd / Id

R = 9 - 1/ 17.02mA

= 8v/17.02mA

= 470 Ohms

3.13 POWER SUPPLY MODULE

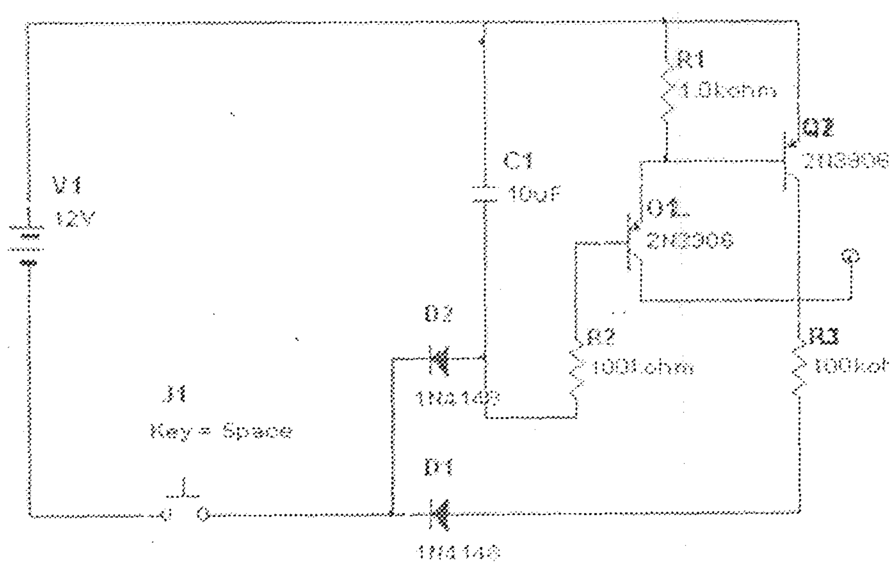


Figure 3.13. Power Supply Circuit Diagram

The power supply is from a 9v battery, the transistors Q1 and Q2 are used to power up the circuit while the button is pressed, and to keep it powered for a few seconds after the button is released. Q1 and Q2 are in what is called Darlington arrangement. The emitter of one transistor is directly connected to the base of the other, this result in higher current gain.

When the push button is pressed the cathodes of the diode are grounded. This pulls the anode of both diodes down to about 0.7 volts; this charges C1 and causes a small current to flow into base of Q2 via R2. As long as the button is pressed, C1 stays charged and current flows to Q2.

The high current gain of the Darlington makes the Q1 to be saturated and pull its collector voltage up to nearly full battery voltage. This provides power to the LEDs and other logic chips when the button is released. C1 is still charged, but slowly discharges through R2 and Q2. When it has discharged to a low voltage, there will be insufficient current in Q2 to keep Q1 saturated; the circuit then turns off.

Darlington pair

In electronics, the Darlington transistor is a semi conductor device which combines two bipolar transistors in tandem (often called 'Darlington pair') in a single device so that the current amplifier by first is amplifier further by the second transistor in the same configuration.

The use of separate transistors in an actual circuit is still common, as used in this project, even though integrated device are available. Darlington pair behaves like a single transistor with a very high current gain. The total gain of Darlington is the product of the gain of the individual transistors.

$$\beta_{Darlington} = \beta 1 \times \beta 2$$

A typical modern device has a current gain of 1000 or more, so that only a tiny base current is required to make the pair switch ON. The base – emitter voltage is also higher. it is the sum of both base – emitter voltages.

$$VBE = VBE1 + VBE2$$

To turn ON there must be ~ 0.6v across both base – emitter junctions which are connected in series inside the Darlington pair. It is therefore required more than 1.2v to turn ON. When a Darlington pair is fully conducting, there is s residual saturation voltage of 0.6v in this configuration, which can be lead to substantial power dissipation.

Another drawback is that the switching speed can be slow, due to inability of the first transistor to actively inhibit current into the base of the second device. This can make the pair slow to switch OFF. To alleviate this, a resistor R1 is connected between the second device base and emitter. [6]

CHAPTER FOUR

4.0 CONSTRUCTION, TESTING, RESULT AND TROUBLE SHOOTING

4.1 CONSTRUCTION

In order to construct the hardware of this project to operate faithfully according to the design, all the sections that made it up were constructed strictly to the specification of the design. Also all the components were connected according to the design with the use of flexible cable

To construct the power supply section, the entire components used were carefully selected based on the design calculation made. Breadboard was first used to connect the circuit and tested okay. The circuit was later transferred to Vero board where permanent soldering was made.

The next step is to construct the pulse generator section, varying the resistors and capacitors to get the desired 40 MHz and 90MHz respectively on the breadboard after which it was transferred to Vero board for perm ant soldering.

The counting circuit had to be implemented by using a breadboard,and later transferring the circuit to Vero board. The circuit tested okay on breadboard, therefore a permanent soldering was done on the Vero board.

Finally the construction of the decoder /driver and display section were connected using the output from the counter as its own input and limiting resistor of 470 ohms were used to limit the current from the output of the decoder/driver to the segment display which was constructed using the light emitting diodes. All these were first tried on a breadboard before soldering it permanently. However, the stages were arranged in such a way that the output of one stage serves as the input to the other stage.

4.2 TESTING

Each section were first tested one after the other on bread board and considerable time was given to each module under test to respond as desired so as to be sure of it reliability. After breadboard testing, each module wee then disconnected from the breadboard and transferred to the breadboard for permanent soldering. And proper soldering techniques were carefully observed.

However final soldering of the entire circuit was then tested section by section by using mutimiter to make sure that they are working as desired.

4.3 TROUBLESHOOTING

It is desired that in improving the maintenance culture, one should also be able to rectify some simple faults which might develop in the electronic dice.

To this end some common faults which could be easily develop in the system are enumerated and simple suggestions on how to go about rectifying them are enlisted in the table below.

Table 4.3

FAULT(S)	POSSIBLE CAUSES(S) AND SUGGESTIONS	TOOLS AND EQUIPMENTS TO USE
Supply mains switch ON, but power not working	If the battery has run down or any of the components	Mutimeter, oscilloscope, soldering iron."

	in power module has burnt. Carry out checks as appropriate on each and possibly replace with a new 9v battery.	lead/suckers.
Supply mains ON, power supply unit working but the dice is not working.	Seven segment display might have burnt, counter, pulse generator and decoder IC might have failed. Study the detail circuit diagram and carry out fault tracing as appropriate.	Multi-meter, soldering iron, IC extractor, lead/ sucker and plier.

CHAPTER FIVE

5.0 DISCUSSION OF RESULT, SUGGESTIONS AND CONCLUSION

5.1 DISCUSSION OF RESULT

For a single roll, the probability of rolling each value, 1 through 6, is exactly 1 in 6. For a double roll, however, the total of both rolls is not evenly distributed, but is distributed in a triangular curve, as follows:

Table 5.1a Probability Table for multiple roll of dice [11].

Total of Dice	2	3	4	5	6	7	8	9	10	11	12
Probability	$^{1}/_{36}$	$^{2}/_{36}$	$^{3}/_{36}$	$^{4}/_{36}$	$^{5}/_{36}$	$^{6}/_{36}$	$^{5}/_{36}$	$^{4}/_{36}$	$^{3}/_{36}$	$^{2}/_{36}$	$^{1}/_{36}$

For the total of rolls of three or more dice, the curve becomes more bell-shaped with each additional die (according to the central limit theorem)[11].

The probability of rolling the same random number repeatedly goes down by $^{1}/_{6}$ with each additional die:

Table 5.1b Table

No. of Dice	1	2	3	4
Probability	$^{1}/_{6}$	$^{1}/_{36}$	$^{1}/_{216}$	$^{1}/_{1296}$

The above list only applies if the number to throw multiple times in a row is randomly chosen.

The project is aimed at design and construction of an electronic dice with a high degree of accuracy and one that is less vigorous in its use for dice game. This aim was achieved though with some technical difficulties.

Problems were encountered in the area of getting a pulse frequency using the 4029 monoviberator IC. It was not so easy to get the accurate frequencies. Besides in the area of getting components for the project work, also some difficulties were met while some component got burnt at the course of construction, it become very difficult and costly to get them replaced and this waste a lot of times and causes delay in the construction.

However after the satisfactory job that has been done, the possible future improvements on this project are as follows:

1 Incorporation of alarm mode which will sound at each play.

2 Dual power supply can be constructed in such a way of using either AC mains or battery

Also going by my experience during the course of designing and constriction of this project, I hereby suggest:

That the university or the department should embrace the culture of helping and assisting student in getting the component for their project work and also they should try to relief student financial wise on their project.

Besides, I also suggest that student of the department should be made to start embarking on min-project work from 300Level upwards. This will go along way in exposing and preparing the electrical students for their final year project.

5.2 CONCLUSION

Since the aim of this project is to design and construct an electronic dice and this has been achieved then the project by all standards can be said to have been of immense success.

Finally this project will be useful in places like clubs, schools, casinos, Ludo game e.t.c and where people of all ages normally come together to catch fun and recreate.

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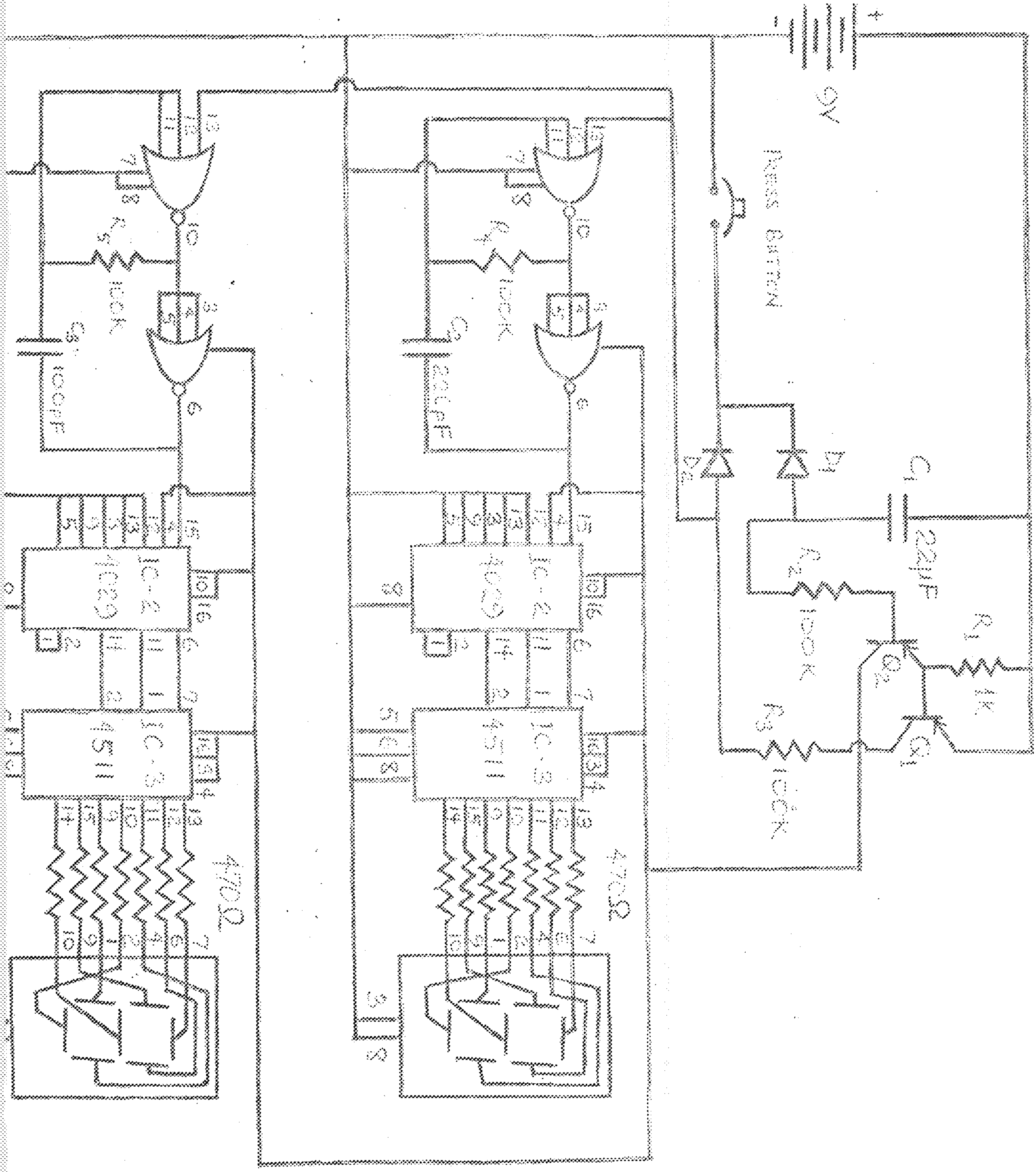
APPENDIX



ELECTRONIC DICE CIRCUIT DIAGRAM.