DESIGN AND CONSTRUCTION OF ELECTRONIC DOORMAN

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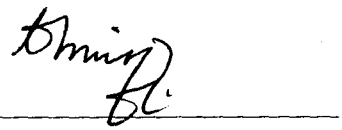
DECLARATION

I wish to declare that this project work titled "Design and Construction of Electronic Doorman" was carried out by me.



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Date

CERTIFICATION

This is certify that UKAH TOCHI. U of the Federal University of Technology Minna carried out this project under the supervision of Engr. (Miss) T. Reyaz and that the project is within scope for the award of a B.Engr in Electrical and Computer Engineering.

Engr (Miss) T. Reyaz	Date
(Project Supervisor)	
Engr M.N Nwohu	28/4/09 Date
(Head of Department)	
External Examiner	Date

DEDIDCATION

This project is dedicated to God Almighty for his grace and to my brothers Stanley, Nnaemeka, Anayo, and Chinedu and also to my sisters Adaku and Fechi.

ACKNOWLEDGEMENT

My profound gratitude goes to my parents Rev Canon Dr and Mrs. E. C Ukaha for their moral and financial support towards my academic pursuit.

In all sincerity, I acknowledge Engr Miss. T. Reyaz, my supervisor, whose directives guided me in all ramifications towards this project and who is at this moment in the United Kingdom for further studies.

I am also grateful to my HOD, Dr Y.A. Adediran, on whose counsels I relied throughout my period of study in the department.

My heart also goes to my friends Emeka, Chidozie, Telvin, Casmir, Felix, those not mentioned and the entire final year students of the department for a wonderful companionship.

Above all, my special thanks go to God almighty for his grace and endowment. Thank you Lord!

ABSTRACT

This report presents the design and construction of an intelligent monitoring device simply called ELECTRONIC DOORMAN. The report is divided into five basic chapters.

Chapter One introduces the concept of the project, provides a brief literature review on the project and also gives an outlined system specification.

Chapter Two gives a step-to-step design and analysis of the basic units of the system. Chapter Three deals with the construction proper and the necessary tests carried out during and after construction.

Chapter Four analyses/discusses the results obtained while Chapter Five gives recommendations on some of the possible improvements on the Electronic Doorman.

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CHAPTER ONE

GENERAL INTRODUCTION

1.0 INTRODUCTION

Counting is now an everyday activity as it is frequently done in schools, offices, homes, companies and equally countries at large as record is being kept on certain figures to maintain a stabilized system.

In most public places with heavy traffic of people during working hours, it is observed that at the end of the days' activity, people suffer being locked up in the building by security men. Such a consequence is the likelihood of not having a pre-knowledge of the people left in the building after closing hours. Thus, a potential problem becomes very visible and which needs an immediate solution.

To solve this problem however, digital electronics has devised schemes utilizing electronic devices, which monitors and keeps an accurate count of the people entering and exiting such buildings. One of such schemes is an intelligent monitoring assembly simply called the **electronic doorman.**

This project and write-up therefore incorporates the step-by-step design, construction and analysis of the scheme whose job is basically to monitor such activity as the number of people in a building.

1.1 LITERATURE REVIEW

Statistical work has always meant collecting, analyzing and presenting data. Only how this is done and types of data collected have changed.

Counting proper has undergone tremendous revolution ranging from the early days when bones and stones were used to the present technological era where sophisticated machines are employed.

In 1928, Hans Geiger a German physicist and Walter Müller, German American developed the Geiger-Muller counter used by scientists and surveyors for detecting the presence and intensity of radiation/particles.

In 1934, Cherenkov Pavel Alekseyvich (1904-1990), a Russian scientist discovered a phenomenon known as cherenkov effect used by radiation detectors called cherenkov counters.

Philip J. Sander designed a circuit that keeps track on the volume of people in an airport environment using a programming language known as labVIEW.

Andrew Mansson, 2000, designed a circuit that keeps track of the number of in a room using Schmitt trigger to turn the light if there are people in the room.

1.2 AIMS AND OBJECTIVES

The major aim of this project is for the system to be able to keep track of the number of people in a building. Hence, the system is expected to:

1. Provide a stable regulated dc power of 5V with sufficient current delivery to drive the various parts of the device.
2. Provide two infrared beams directed at two photodiodes, which will serve as human/machine interface. This is such that an obstruction in the path pf any of the beams is capable of producing a pulse sequence which will determine if it is an entry or an exit.
3. Provide circuitry for decoding such sequential pulses and provide distinct pulses on either pf two separate lines.
4. Provide for the counting, storage and appropriate display of accumulated pulses.

5. Be able to count up to 1000 people (000 - 999) at most and also have the flexibility to be extended when necessary.
6. Thus with all these in mind, a preliminary block diagram showing the different units of the electronic doorman is discussed below.

1.3 GENERALISED BLOCK DIAGRAM

Shown in figure 1.1 is a simplified block diagram of the electronic doorman. The blocks/units that make up the entire system have been grouped into four different parts viz, the power supply unit, the optical assembly, the logic control unit and the counter/display unit.

1.4 PROJECT OUTLINE

In this report, chapter one gives a brief introduction to the project, stating in an elementary nature how the project is expected to work, the literature review as well as the aims and objectives.

Chapter two gives a detailed outline of the step-by-step design and analysis while chapter three takes a look into the testing, construction and problems encountered in the progress of the work.

Chapter four however gives a brief discussion on the result obtained while chapter five concludes and gives certain suggestions as to how this work can be improved upon.

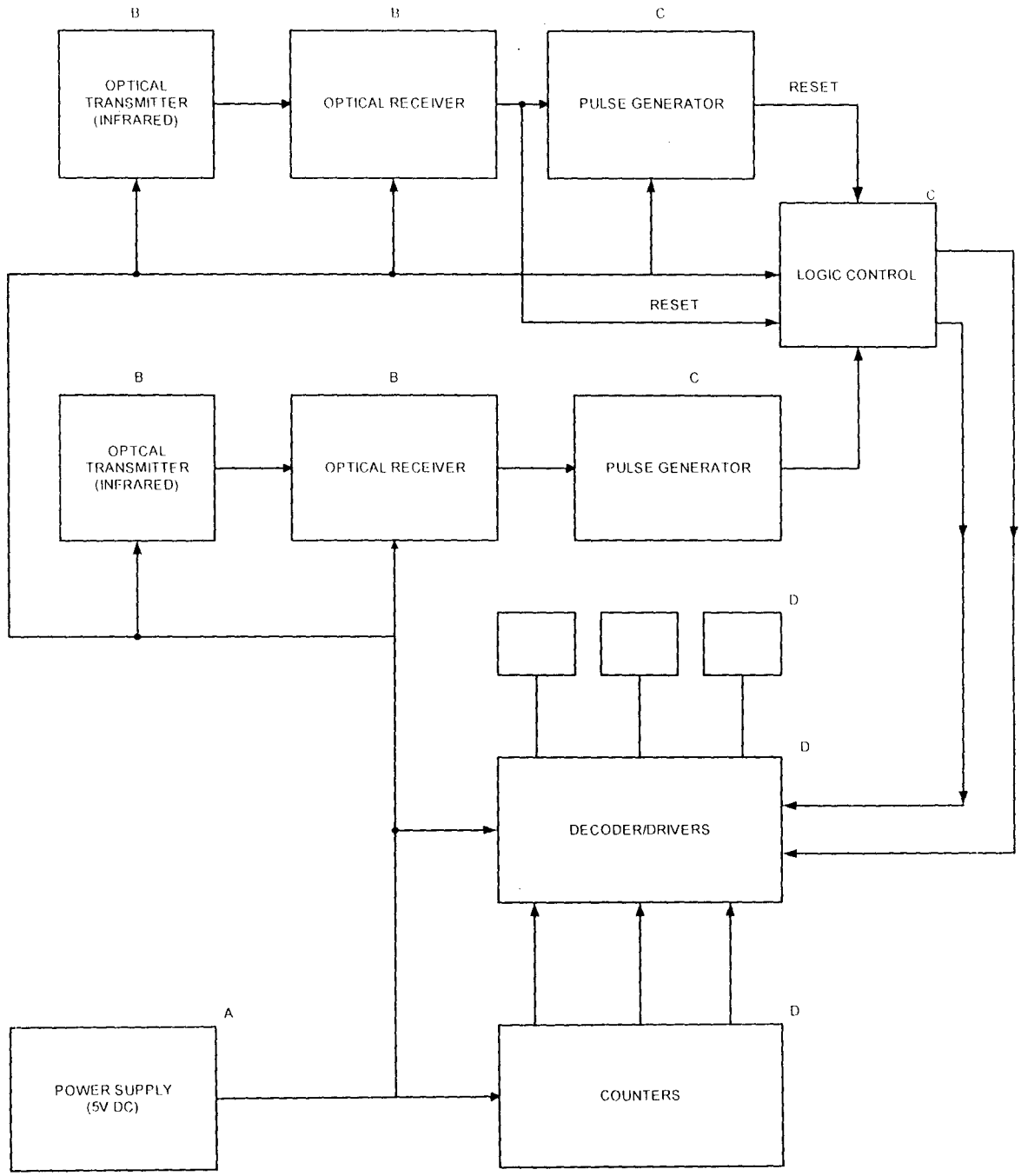

FIG 1 1 GENERALIZED BLOCK DIAGRAM

A - Power Supply Unit
B - Optical Assembly
C - Logical Control Unit
D - Counter/Display Unit

CHAPTER TWO

DESIGN AND ANALYSIS

2.0 PRINCIPLE OF OPERATION

The system uses the up/down count principle of the 74192 up-down counters to allow for up and down count when the beam is broken in an entry and exit respectively.

An infrared is projected to a receiver (photodiode) and the transducer is fed to an op-amp that gives a LOW logic level when the beam is broken. The LOW from the receiver is used to trigger a 555-timer monostable with a time constant of 1 sec. This clocks the counter and also sets the flip-flop to select proper mode of operation. The counter thus sends signals to the decoder that drives the output display (seven segment display).

2.1 OPTICAL TRANSMITTER

An optical transmitter could be seen as any light source. But it would not be of any importance if such a light source cannot be controlled. Thus an optical transmitter here is defined as alight source whose output could be controlled by some external electrical signal in such a way that it can carry information. There are basically two categories

viz, incandescent lamps and semiconductor devices. The semiconductor devices include light emitting diodes (LED), infrared diodes and the laser (light amplification by stimulated emitted radiation) diodes.

Hence, the infrared diode was chosen due to its availability and its ability to emit of invisible rays/beams.

2.1.1 INFRARED TRANSMIITER STAGE

The infrared stage involves biasing the infrared diode and controlling the transmission. The infrared stage is shown in fig 2.1 below

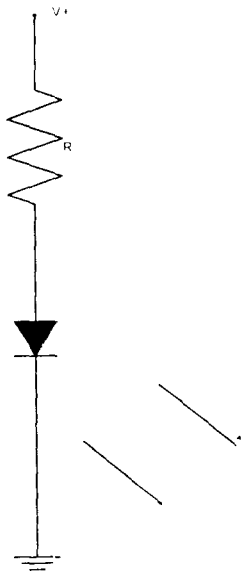

FIG 2.1 INFRARED TRANSMITTER STAGE

The infrared diode has a forward current I_F of 150mA and a forward voltage drop V_F of 1.7V.

Therefore, $$R = \frac{V^{+} - VF}{IF}$$

$$= \frac{5 - 1.7}{150mA} = 22\Omega$$

A preferred value of 33Ω was however used.

2.2 OPTICAL RECEIVERS

These are devices that convert optical signals into electrical signals. They are of different types that differ both in their internal structure, mode of operation and sensitivity.

However, their suitability for particular application depends mainly on their sensitivity, response time and cost. Examples are light dependent resistors (LDR), photodiode (used for this project), and phototransistors.

2.2.1 INFRARED RECEIVER STAGE

The photodiode was employed as the receiver because of its ability to resist daylight interference. The photodiode is operated in a reverse bias condition. In darkness, it has a high resistance (hence a low current) but when light (infrared) falls on the photodiode, the leakage current is increased in proportion to the amount of light falling on the pn junction. The infrared receiver stage is show in fig 2.2 below.

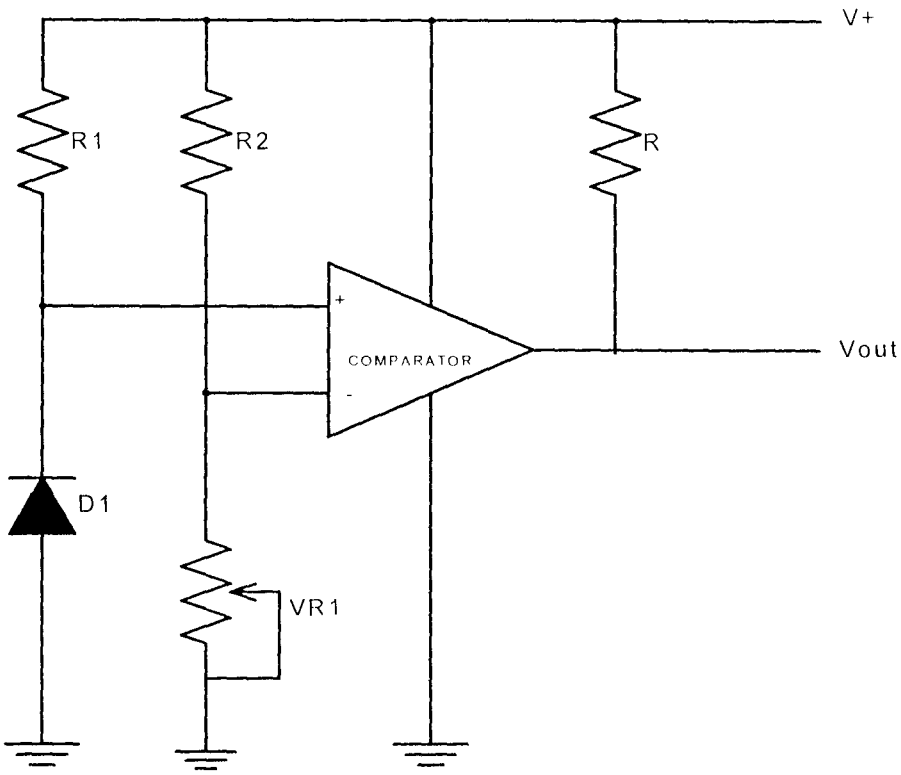

FIG 2.2 a INFRARED RECEIVER STAGE

Considering that the photodiode has a high resistance in darkness, which reduces as light intensity increases. By direct measurement, the resistance in darkness was obtained to be approximately 1MΩ while the resistance in light is 100KΩ (the reverse bias resistance on full transmission).

For darkness:

(See fig 2.2b overleaf)

$$V_D = \frac{R_{dark} \times V+}{R_{dark} + R1}$$

(V_D = 1.5V in darkness)

$$= \frac{1M\Omega \times 5V}{1M\Omega + R1}$$

Thus making R1 the subject, ---------

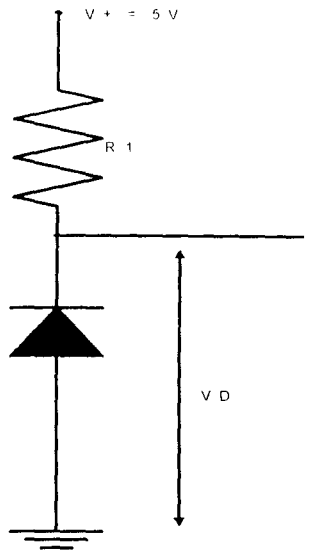

FIG 2.2b

----- $\frac{1.5}{5} = \frac{1M}{1M + R1}$

$0.3 = \frac{1M}{1M + R1}$ (cross multiply)

Therefore, $0.3M + 0.3R1 = 1M$

$0.3R1 = 1M - 0.3M = 0.7M$

Which implies that: $R1 = \frac{0.7M}{0.3} = 2.3M\Omega$

$= 2.2M\Omega$ preferred value.

LIGHT:

$$V_D = \frac{R_{light} \times V^+}{R_{light} + R1}$$

$= (100K \times 5) / (100K + 2.2M)$

$= 0.2V$

The output of the comparator stage is given by:

$$V_{out} = A_0 V_{in}$$

Where: A_0 is the open loop voltage gain

$V_{in} = V^+ - V^-$, and

V^+ = non-inverting input of the comparator

V^- = inverting input of the comparator

Since A_0 is very large (20,000), the comparator tends to saturate to V+ (5V) or 0V if there is a positive or negative difference respectively. Therefore setting a reference voltage from VR1 to be 1V, Vout will be approximately 0V when the beam is blocked (i.e. in darkness), and approximately 5V upon transmission of the beam. On this note, a dual comparator, LM 393, was employed to serve for the exit and entrance respectively.

2.3 MONOSTABLE STAGE

The most popular of the present IC timers is the 555 timer, which is mostly available in an eight-pin package. The 555 timer is relatively stable IC capable of being operated as accurate bistable, monostable or astable multivibrators.

The output of the previous stage (i.e. receiver/comparator) was designed so that trigger conditions for the monostables are met. To trigger monostable, trigger voltage must be less than or equal to 1/3 Vcc. Hence, the output of the comparator falls to approximately zero when the beam is broken. Fig 2.3 shows the monostable stage with the appropriate connection of the 555 timer.

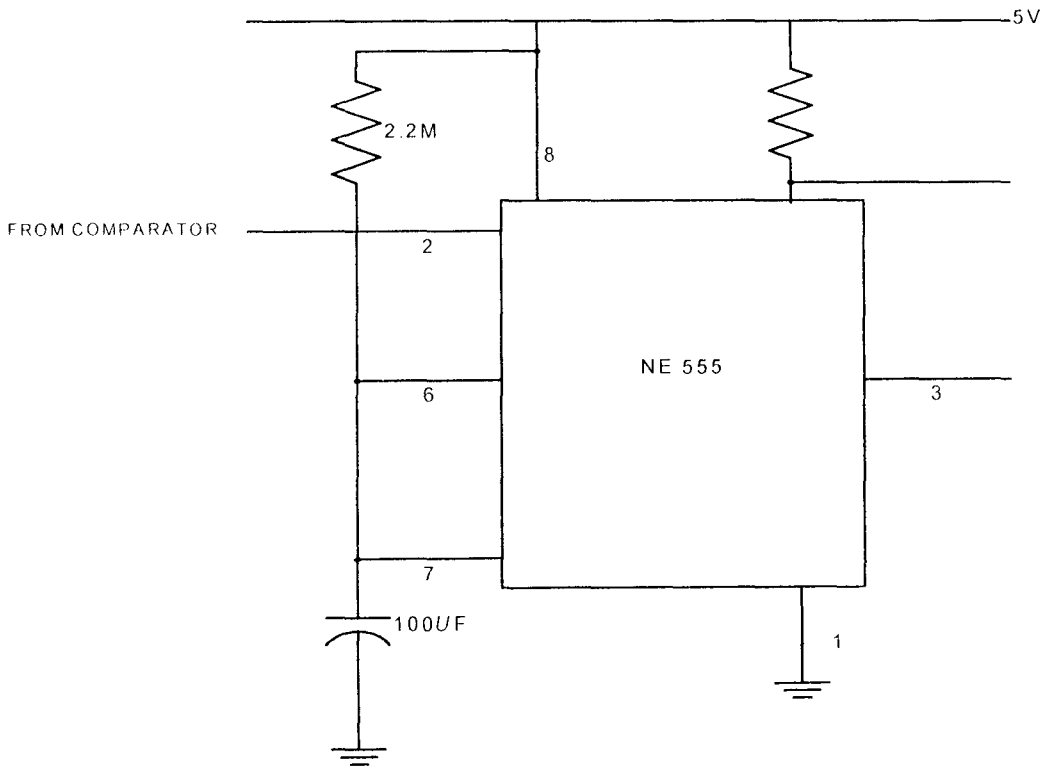

FIG 2.3 MONOSTABLE STAGE

Monostable time constant $T = 1.1RC$ ---------- (1)

A time constant of 1sec was employed to allow for proper counting even if the people entering or leaving are in a queue.

From (1), letting C= 100μF

$$R = T / (1.1C)$$

$= (1) / (100\mu F) = 9090.9\Omega$

$= 10K\Omega$ preferred value.

2.4 THE LOGIC CONTROL

The control logic uses a D-type flip-flop. The function of the flip-flop is to set the conditions for up and down count of the counter stage. The up and down count conditions are mutually exclusive hence, the Q and $\overline{Q}$ outputs of the flip-flop (7474) IC were used.

The operation of the flip-flop is best described with the truth table below. In this project, it was wired (designed) to operate in SET and ASYNCHRONOUS RESET modes.

OPERATING MODE	INPUTS				OUTPUTS	
	SD	RD	CP	D	Q	$\overline{Q}$
ASYNCHRONOUS SET	L	H	×	×	H	L
ASYNCHRONOUS RESET *	H	L	×	×	L	H
LOAD 1 (SET) *	H	H	×	h	H	L
LOAD 0 (RESET)	H	H	×	l	L	H

TABLE 1: TRUTH TABLE OF 7474 D-TYPE FLIP-FLOP

H = HIGH voltage level steady state

h = HIGH voltage level one step up time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

For SET mode, the high required for D input is achieved by connecting D permanently to V+ (5V).This automatically prohibits any synchronous mode. In SET mode, the output Q is high while Q is low. Fig 2.4 shows the circuit of the flip-flop and control logic stages.

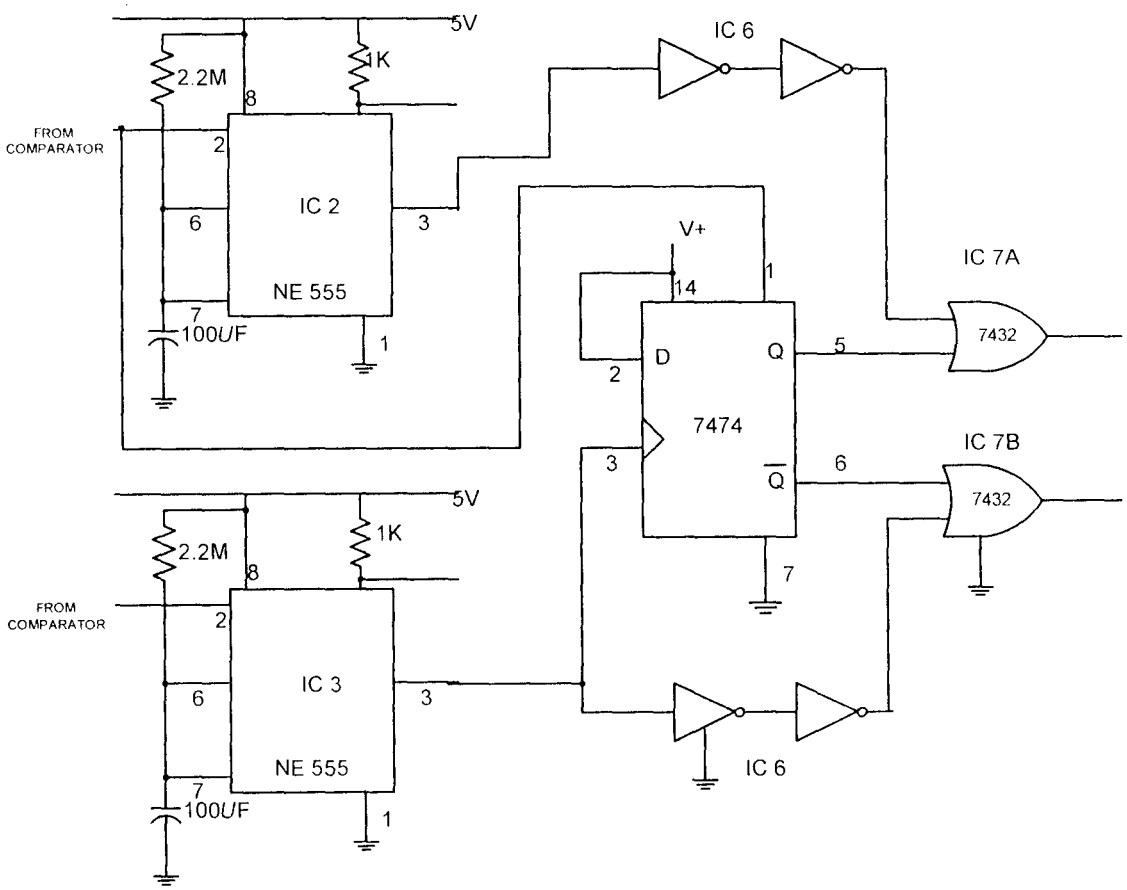

FIG 2.4 CONTROL LOGIC STAGE / FLIP-FLOP

An OR gate gives a 1 when either inputs is a 1. When the flip-flop is in set mode, the OR gate IC 7A sends a 1 to the CPD of the counter (74192) while the second OR gate (IC 7B) gets the clock pulse from the monostable (IC 3) and sends it to CPU of the counter

IC 6 is a NOT gate (40106) which establishes a delay pulse reaching the counter input to ensure that the opposite CP input of the counter gets a 1 before the other.

2.5 COUNTER STAGE

A binary counter has the following characteristics:

1. It is a sequential circuit that counts or tallies the number of input pulses it receives.
2. It is a memory device that stores the number of input pulses.
3. The number of input pulses, or the count, can be determined at any time, because the bits are those stored in the flip-flops that make up the counter.

Flip-flop generally may be used to form counters but the JK flip-flop is the most popular and most flexible to use. Counters are therefore categorized to Synchronous and Asynchronous (ripple). They are made up of flip-flops, which are triggered sequentially (as in the case of Asynchronous counters) and simultaneously as in the case of Synchronous counters.

However, in this project a 74192-up/down BCD counter was employed. Table 2 below explains the operation of the 74192. The counter has basically four operating modes from the truth table. The count up, count down and reset modes were employed.

Fig 2.5 shows the counter stage. The counters are cascaded to enable a count up to approximately 1000. To count up, CPU gets clock and CPD is activated with a HIGH. Conversely, to count down, CPD gets clock and CPU is activated with a HIGH. Cascading is done via TCU and TCD.

	INPUTS								**OUTPUTS**					
OPERATING MODE	MR	PL	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	TC_U	TC_D
	H	X	X	L	X	X	X	X	L	L	L	L	H	L
RESET (CLEAR) *	H	X	X	H	X	X	X	X	L	L	L	L	H	H
	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
PARALLEL LOAD	L	L	L	X	H	X	X	H	Qn = Dn				L	H
	L	L	H	X	H	X	X	H	Qn = Dn				H	H
COUNT UP *	L	H	↑	H	X	X	X	X	Count up				$H^{(b)}$	H
COUNT DOWN *	L	H	H	↑	X	X	X	X	Count down				H	$H^{(c)}$

TABLE 2: 74192 TRUTH TABLE

H = HIGH voltage level.

L = LOW voltage level.

X = Don't care.

↑ = LOW – to – HIGH clock transition.

b = TCU = CPU at terminal count up.

c = TCD = CPD at terminal count down.

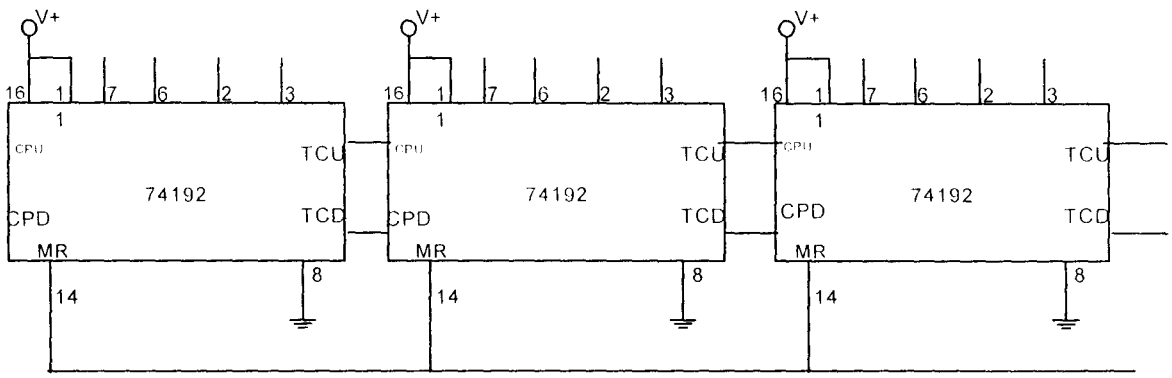

FIG 2.5 COUNTER STAGE

2.6 DECODER / DRIVER / DISPLAY

A decoder is a combinational circuit or a device that translates binary codes back into the characters they represent. The decoder/driver used in this design was 7447, a BCD-to-seven segment display driver, which decodes the output of the counter. Table 3 below shows the truth table for the 7447 driver.

Since the basic output unit of this project is a readout display, light emitting diodes (LED) were used as the display type based on its brightness, low cost, reliability and compatibility with low voltage integrated circuitry. Practically the common-anode arrangement was effected. This entails connecting the anode of the LED to V^+ while the cathode is connected to the decoder/driver.

Assuming all display bars are ON,

Current through each LED = 5mA

For 7 LED, forward current IF = 7 x 5mA = 35mA

Now, forward voltage VF = 1.7V

Thus, $$R = \frac{V+ - VF}{IF}$$

$$= (5 - 1.7) / (35mA) = 94\Omega$$

$$= 270\Omega$$ preferred value for the three displays.

DECIMAL	INPUTS				OUTPUTS						
	D	C	B	A	a	b	c	d	e	f	g
0	L	L	L	L	L	L	L	L	L	L	H
1	L	L	L	H	H	L	L	H	H	H	H
2	L	L	H	L	L	L	H	L	L	H	L
3	L	L	H	H	L	L	L	L	H	H	L
4	L	H	L	L	H	L	L	H	H	L	L
5	L	H	L	H	L	H	L	L	H	L	L
6	L	H	H	L	H	H	L	L	L	L	L
7	L	H	H	H	L	L	L	H	H	H	H
8	H	L	L	L	L	L	L	L	L	L	L
9	H	L	L	H	L	L	L	H	H	L	L

TABLE 3: TRUTH TABLE OF 7447

2.7 POWER SUPPLY UNIT

This consists of a step-down transformer, a rectifier, a filter circuit and a regulator. Basically, these components serve to provide the required dc voltage for the entire project.

The transformer steps down the ac mains supply voltage to 12V ac. The bridge rectifier converts the ac voltage from the transformer into unidirectional pulses (dc voltage). However, the shunt capacitor filter filters the imminent ripples in the voltage supplied by the rectifier while the regulator circuit provides a constant 5V dc supply required by the project. The output of the regulator remains constant irrespective of changes in the mains input voltage or changes in the load driving current. The 7806 regulator was chosen because of its size and availability. However, this gives a regulated voltage of 6V which is not suitable for TTL (that requires 5V), hence the power transistor was incorporated as the control element and thus a 5V dc is supplied to all other units of the project. Fig 2.7 shows the power supply stage.

The capacitance C1 is inversely proportional to the ripple gradient of the voltage.

Therefore,

$$dV/dt = 1/C1$$

which implies that: $C1 = dt/dv$

dV = ripple voltage

dt = time of dV

Setting ripple to be 20%

The peak voltage $V_{peak} = 12 \times \sqrt{2} = 16.9V$

Therefore 20% ripple = (20/100) x i6.9 = 3.38V (=dV)

For 50Hz, dt = 10ms

Hence C1 = dt/dV = 10ms/3.38V

= 3380μF

≈ 3300μF preferred value.

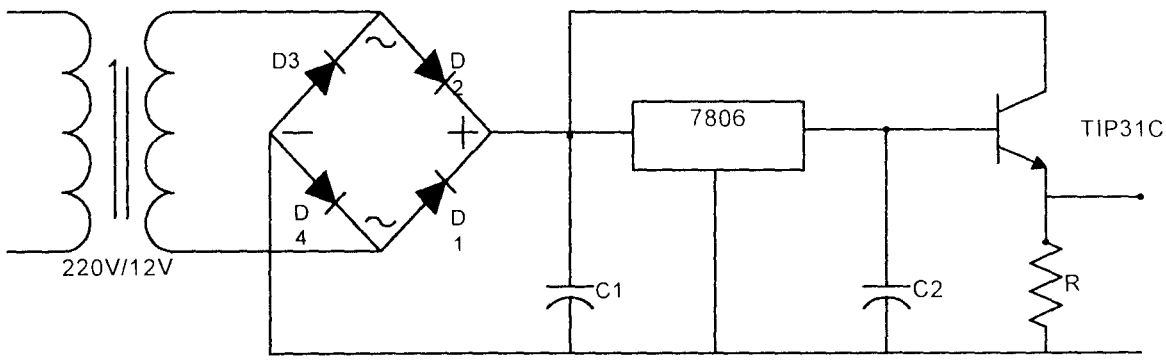

FIG 2.7 POWER SUPPLY UNIT

CHAPTER THREE

CONSTRUCTION AND TESING

3.1 INTRODUCTION

For the effective demonstration of the workability of the design for the electronic doorman, a prototype has been constructed as will be described hereunder. The prototype has been constructed in such a way that it reflects the operation capabilities and consequent implementation of the device. As such, the procedure for construction and assembly of the electronic doorman is described below in a stepwise manner that resulted in the complete system.

STEP 1: IMPLEMENTATION

The first step taken in the building of the electronic doorman was the actual designing of the circuitry necessary to carry out the required task. This design procedure has been handled extensively in chapter two. The next step was the implementation of the modules (units). This stage was carried out on a breadboard and entailed connecting and disconnecting the various components and parts until a suitable design was finally obtained.

STEP 2: CONSTRUCTION

This stage was basically done in two stages. The first stage was the actual soldering of the components onto a Vero board thereby making the connections permanent. In this stage, the Vero board was sectioned to accommodate the various units.

The second stage was the casing of the project. The Vero boards containing the soldered components were housed in a metal casing in such a way that none of the connections were bridged or short-circuited. The final outcome is as depicted in the picture below.

PICTURE OF THE PROTOTYPE OF ELECTRONIC DOORMAN

STEP 3: TESTING

During and after the construction, confirmatory tests were conducted. This ranges from component test to the final test. In the component test, all the components were tested to certify that they were in good working condition and most importantly the specified design values. Similarly, the outputs of the various units were tested basically for verification purposes.

The final test includes breaking the beams being transmitted at the entry and exit inputs of the system respectively. The system however responded accurately by counting up in the first case and down in the second case.

The equipment used in testing stage includes digital multimeter and the oscilloscope. The later was used to observe the various waveforms at different stages while the former was used to measure various electrical parameters such as voltage, current, continuity and resistance value of components.

3.2 PROBLEMS ENCOUNTERED

No doubt, many problems were encountered o the course of this project. Some emanated perhaps due to design limitations and others

due to human errors. One of such problems is the unavailability of some components. The initial concept of this project was to incorporate two LASER diodes as the optical transmitters but their unavailability in the market resulted to the use of infrared diodes which of course emit dispersed rays.

Again, during computer simulation, the exact implementation of the optical transducers gave no results and this led to the employment of opt couplers/isolators.

Other problems were those from unsuitable design. However, these problems did not defeat the goal of this project.

3.3 PRECAUTIONS.

Certain precautions were taken during project realization for optimum performance, some of which are outlined below.

1. Most of the ICs were attached via sockets to ensure that the ICs have no direct contact during soldering.
2. The Vero boards were fastened to the metal casing in such a way as to avoid contact with the casing, thus eliminating the problem of short circuit.

3. The components were firmly soldered to avoid partial contacts, which may induce heat and possibly damage the components.
4. A low power soldering iron was used to ensure that a minimal amount of heat was transferred to components during soldering.

CHAPTER FOUR

DISCUSSION OF RESULTS

The system is a dark-operated device, which energizes the output in response to a dark signal at the photo receiver (photodiode). The practical realization of the project satisfies most of the design objectives earlier stated in the report.

Thus, the **electronic doorman** provides a stable regulated dc power supply of 5V with sufficient current delivery to drive the various parts of the system. The system in the same vein, provides two beams directed at two photodiodes for entry and exit respectively which serves as the human/machine interface in such a way that an obstruction in the path of beam produces a pulse sequence which determines the direction (whether entry or exit).

The system consequently provides circuitry for decoding, counting, storage and appropriate display of the accumulated pulses. Therefore a maximum counting capacity of 1000 people (0 - 999) justifies that the system operates with respect to design specification, though it has the flexibility of being extended when necessary.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATION

5.0 CONCLUSION

This project report has given a detailed foundation and detailed analysis of the design and construction of an electronic doorman. The procedures and techniques used towards achieving the scheme have also been treated. Hence, the motive of the design was realized and this proved further that the design can be constructed from the basic principles of photo transducers, digital timing and counters.

5.1 RECOMMENDATION

Having built a prototype to demonstrate the workability of the scheme, it is thus imperative to state that this design can be improved upon in several ways. One of such ways is the implementation of the control logic with a microprocessor, which provides amore accurate and reliable result when compared with other schemes.

Finally, the system could be expanded to carter for a more practical range and as such suitable for use in public places e.g. a shopping mall most probably as a crowd monitoring system.

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COMPREHENSIVE CIRCUIT DIAGRAM OF THE ELECTRONIC DOORMAN