DESIGN AND CONSTRUCTION OF ELECTRONIC DIGITAL CLOCK

By

IDRIS ABDULRAHIM

97/6027EE

A project submitted to the Department of Electrical and Computer Engineering, School of Engineering and Engineering Technology,
Federal University of Technology, Minna.

In Partial Fulfilment of the requirement for the award of Bachelor of Engineering (B.Eng) Degree in Electrical and Computer Engineering.

AUGUST 2003

CERTIFICATION

I certify that this project was carried by **Idris Abdulrahim** under my supervision of my supervisor **Dr. Y. A. Adediran** of Electrical and Computer Engineering Department Federal, University of Technology, Minna, Niger State.

Dr. Y.A. Adediran
Supervisor

.....
Signature/Date

Engr. M. W. Nwohu
H.O.D

7/4/09
.....
Signature/Date

.....
External Examiner

.....

DECLARATION

I hereby declare that the project work is an original concept wholly carried out by me, under the Supervision of **Dr. Y.A. Adediran** of the Department of Electrical and Computer Engineering, Federal University of Technology, Minna

IDRIS ABUL
Name

21/10/2003
Date

DEDICATION

I dedicated this my project to all members of **Idris's family**. And to my two Late elder brothers, Mr. Isiaq Idris and Mr. Yusuf Idris (Mallami) may ALmighty Allah grant them ALIJANT FIRDAOUS (AMIN WA IYAKUN). And also to my parents Mallam Idris Akanbi and Madam Aminat Idris, whose love and cares got me to where I am today.

Finally to Almighty Allah for his guidance and protection during the period of my stay throughout in school.

ACKNOWLEDGMENT

My profound appreciation goes to Almighty Allah for his guidance bestowed on me and for making me part of history in the Department of Electrical and Computer Engineering.

I also express my profound gratitude to my parents Mallam Idris Akanbi and Madam Aminat Idris for their moral love and financial support given to me. I will also like to acknowledge the support of my brother Mr. Abdulfatai Abdulkareem for his financial assistance throughout my period in school.

A million appreciation also goes to my Project Superivior Dr. Y.A. Adediran for his contribution towards his guiding and conscience in brining this project successful. My thanks to the following my Project Partner Mr. Abaniwo T.E. Peter for making this a reality and my best twin friend Mr. Oyewobi Stephen Oluwaseyi for he's love and care, Mr. Adigun Oluwafemi, Mr. Yusuf B. Olanrewaju, Mr. Femi Sangodere, Mr Seun Olawale, Mrs Medinat Abdulfatai, Engr. Saka Abdulkarim, Engr. Fatai Jimo, Mr Matins Augustine Clement and Mr. Yunusa Ibrahim.

Finally all praises and glory goes to Almighty Allah for his everlasting love, guidance and protection.

IDRIS ABDULRAHIM

ABSTRACT

In this project, the design and the construction of an Electronic Digital Clock is presented. The Digital Clock is made up of Pulse Generator, the Frequency Division, the Decoder/Disiplay, the time setting and the power supply. A square oscillator generated a clock frequency of 1Hz. The frequency division section of the clock divides the clock frequency into 60 second, 60 minutes and 12 hours respectively thereby making up the seconds, minutes and hours sections respectively. A means of setting the time is provided using the clock generating circuit and exclusive OR gate. The system had been powered by regulated power supply.

TABLE OF CONTENT

CHAPTER THREE

CHAPTER FOUR.

CHAPTER ONE

1.0 INTRODUCTION

In the early days scientist had been wondering what was happening in the heavens and soon they an instrument for measuring time "The sun-dial provided them with a redding of the passage of time as accurate then as it could be expected at that time and this marked the beginning of time measurement.

As the Technology of time measurement became more advanced time keeping continued to be come and more accurate. The mechanical clock followed the sundial and the quarts clock followed the mechanical clock.

The first quartz clock appeared in 1929. It operated through the vibration of a quarts crystal through which an electrical voltage is applied. Such oscillations are accurate to within one second in ten years. The cost effective quartz crystall in now at the heart of most everyday time piece.

The atomic clock was developed in U.S.A. in 1948 it was based on the oscillation of the element caesium. It measures the frequencies of its atoms and molecules. Atomic clock are accurate to one second in I.C. million years.

The addent of the digital clock is a major break through in time mea-

surement instead of using the shadow cast by the sun like the sundial or by using mechanical spring. Like the mechanical clock digital clock was used.

Although there has been no large scale production digital clock in Nigeria many local researchers have made attempt to develop a cast effective means of time measurement using digital electronic methods. However looking at most of this attempt it is obvious that there is still the need for a more reliable and more accurate digital clock design by local engineers.

The is the motivation of this report.

This project is dimed at developing a digital clock that shall operate as follow:-

A IHz square wave clock signal is generated and feed into the second, section which is used to count dad display second from 0-59. ABCD counter advances one count per second. After 9 second the BCD counter recycles to O, which trigger a MOD-6 counter and cause it to advance one count. This continues for 59 second, after which the next pulse recycles the MOD-6 counter to Zero (The MOD-6 counter and the BCD counter make up the MOD -6 counter.

The out put of the MOD -6 counter in seconds section which counts and displays minute from O through 59. The minute section is identical

to the seconds section and operate exactly in the same manner.

The out put of the MOD - 6 Counter in the minute section has a frequency of one pulse per hour. This signal is fed into the hours section which count and diagram of the digital clock is shown in figure (a) 1.0 below.

1.1 PROJECT LAYOUT

This report contains four chapter and the chapters are arranged in the order by which the design was carried out.

Chapter one.

It deal with the introduction literature Review project objective/ Motivation and project layout

Chapter two

Deals with the system Design and other technical

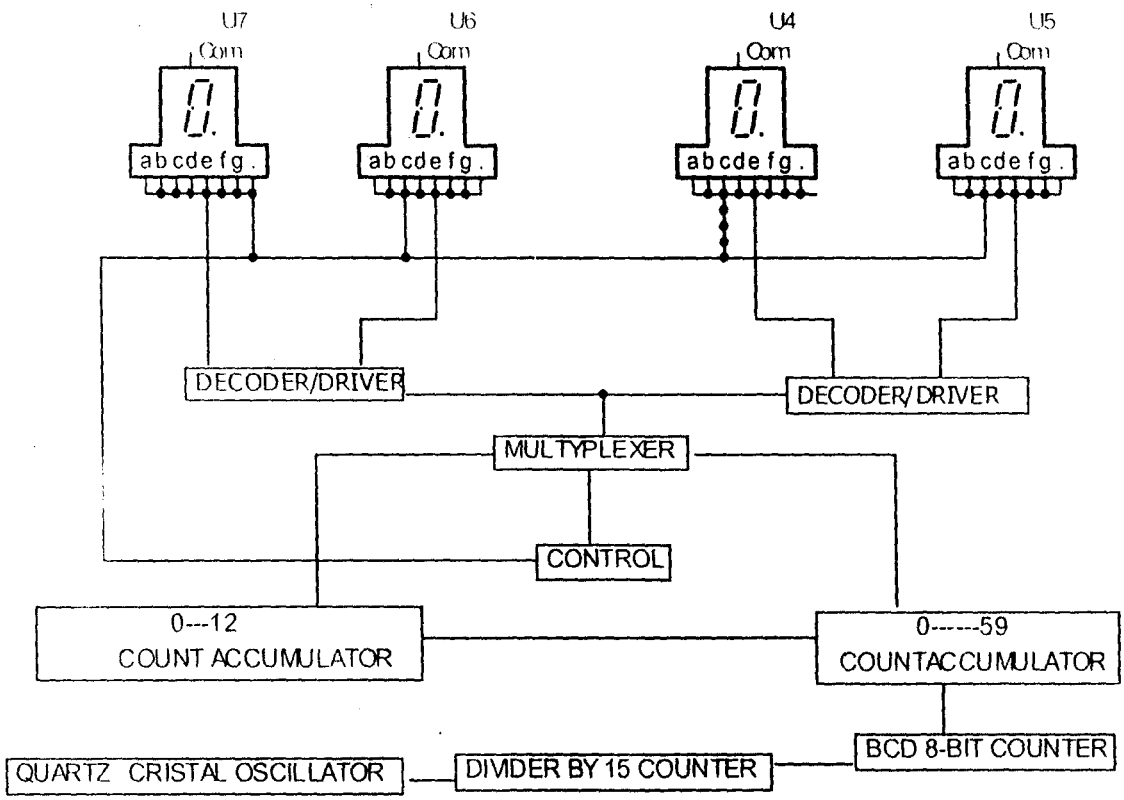
Chapter three

Deals with the construction Testing Results and discussion of Result.

chapter four

Conclusion Recommendation suggestion, Appendire and Reference.

Fig. 1.0.0 Explain the basic flow of the design of this project which are in block diagram.



In order to construct an accurate digital clock, a very closely controlled frequently is required. For battery operated digital clocks, the basic frequency is normally obtained firm a quartz crystal oscillator.

Digital clocks operated from the a.c. power line can use the 50Hz power as the basic clock frequently. But in either case the basic frequency has to be divided down to a frequency of 1Hz or 1 purse per second (1pps).

1.2 LITERATURE REVIEW.

Electronic digital clock is not a new invention over olges past there have been companies engage in construction and marketing of the digital clock their design method or technique used is usually not available for analysis. However information has it that a microprocessor design of a digital clock system is now available using this method reduces a lot of component but involves learning and using machine code program the microprocessor.

In the course of designing the digital clock system the project is analyzed. The digital clock development have the following units the pulse Generator the frequency division the decoder Display the time setting and the power supply. A few of these units have one problem or the other. But in this project design an effort is made to overcome these problem in various unit of the system.

PURSE GENERATING UNIT.

In 1988 Gong used the frequency of the A.C mains supply to generated Hz square wave clock pulse signal. This is not reliable due to the fact that the accuracy of the A.C main line frequency.

However it is a known fact that the frequency of the A.C line voltage is voltage is subjected to change due to many sectors among them over lodding generating station. GARBA (1991) on the other hand used a 555

timer connected as suitable multivibrator to generate a 1 Hz square wave clock pulse signal. This method is not reliable due to the fact that any small change in D.C. power supply to the 555 timer will result in change in the frequency of the clock pulse.

The ambient temperature can also affect the frequency of the signal. But in this project an effort is made to over come these problem mentioned above in this unit. By using a pair of CMOS (CNAND Gate connected as an inverter) inverter connected together to form an RC relazation Oscilator. Which general a 1Hz square wave signal within a b, to 18 d.c supply however it is less affected by temperature.

FREQUENCY DIVISION UNIT

The frequency division unit consist of the hours minutes and seconds section. Gong (1988) used 4018 CMOS BCD counter 1 Cs for the minutes and second section which the used 4029 COMS presentable up/ down counter I.C and 4027 CMOS J.K master slave flip plop for the hour's section.

GARBA (1991) used 4510 BCD up/Down counter IC for the various section of the units. However Gong and Garba used CMOS ICs. and CMOS ICs in general have low switching speed highly affected by electrostatic charge and CMOS inputs shows a large spread in logic threshold which can lead to the problem of clock skew. But in this project design 74129 4

bit synchronous up /down counter ICs where used for the various sections of the unit. This ICs has a high charge speed and is less affected by electrostatic charge, through it has the problem of high power consumption and low noise Immunity.

DECODER DISPLAY UNIT.

Both Gong (1988) and Garba (1991) used 4511 CMOS BCD to seven segment decoder/driver to decoder to the BCD to seven segment LEDS Displays.

In both case the seconds section decoder and display where not construct. But in this project 7447 bits BCD to seven segment decoder/ driver where used to decode the counter out put and a common cathode LEDs display were used in displays section. However the hours minutes and seconds section were all devoted and displays.

TIME SETTING UNIT

Gong (1988) used the 1Hz square wave signal for setting the hour section and five NOR Gate connected together to form an exclusive OR function with the 1Hz clock signal, were used for setting the minute section while Garba (1991) design his time setting with the 1Hz clock signal AND gate. But was not constructed. In this project the time setting unit was constructed using 7486 exclusive OR gate I.Cs for setting the

hou s and second sections.

This method reduces the complexity and number of the component in this unit.

THE POWER SUPPLY

Gong (1988) used a zener diode regulator to regulate a 12 V.D.C to 9 volts. However zener diode can be affected by the ambient temperature and cannot be handle high out put current while Garba (1991) used an unregulate power supply.

But in this project LM 7805 ICs regulate 9v to 5v Dc. This method is less affected by temperature and can tolerate wider input voltage within it limit.

CHAPTER TWO

DESIGN OF COMPONENTS

2.0 INTRODUCTION

The block representation of a digital clock is as shown in figure 1.0.0. Each block represents a stage in the whole circuit arrangement. There are six stages. The power supply, the time (pulse generator), the divider by 15 counter, the count accumulator, drivers and display state.

The states are arranged in such as way that the output of one stage serves as the input to the other stages. This chapter covers all the design specification of each stage.

2.1 THE TIMER (PULSE GENERATOR)

The function of the timer is to generate timed pulses that are counted by the counter there are several types of astable muitilubrators that are in common but a quartz crystal oscillator was chosen for this project.

QUATZ CRYSTAL OSCILLATOR.

A quartz crystal controls the oscillation of an electric current the frequency of which is reduced to compute time.. The maximum error of the must accurate quarts crystal clocks is plus or minus one second in ten years. how our they are made from CMOS.

CMOS in computer science, acronym for complementary metal oxid semi conductor.A Semiconductor device that consist of two metal oxid, semi conductor field effect transistors (MOS FET One N- Type and one type integrated on a single silicon chip. Generally used for switching applications there device deuie have extremely low power consumption at some cost in speed. They are how ever easily damaged by static electricity.

A Phenomenon there by a potential Difference is developed across the opposite phases of a quarts crystal when a mechanical stresses are applied to it is called piezoelectric effects.

The extremely high quality factor or quarts crystals applied to osicllators Led to very stable frequency values such as used in timing circuits and clock signal generator. When a crystal is not vibrating it is equivalent to a capacitor knownlannion as mounting capacitor (cmy and oscillator quartz crystal because like a tuned circuit as shown in figure below

Fig 2.1

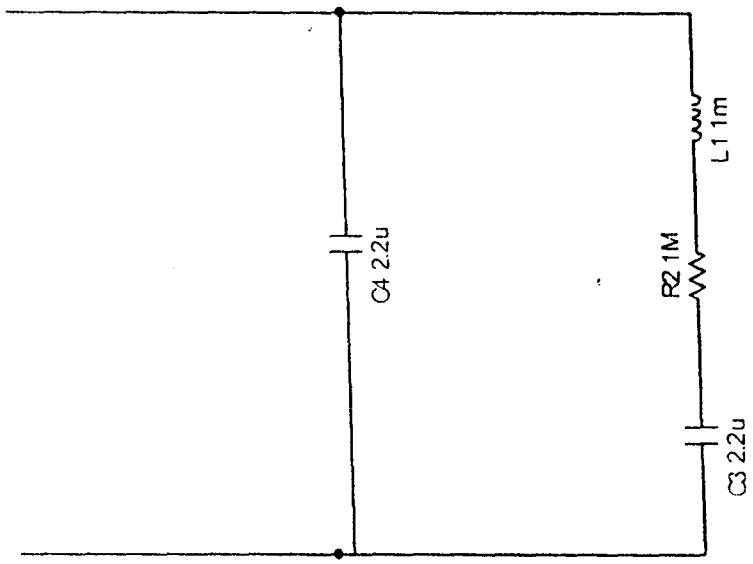
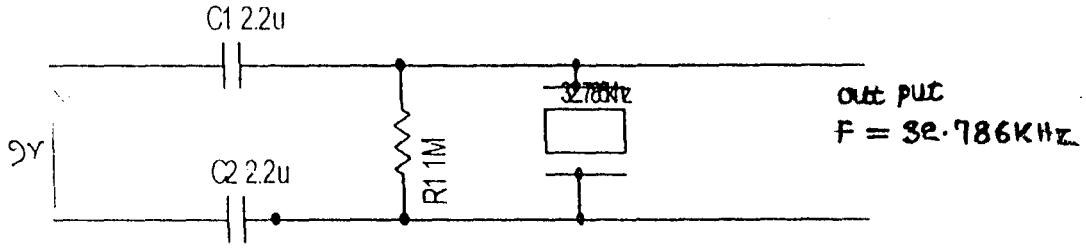

L1 1m
R2 1M
C4 2.2u
C3 2.2u

Fig 2.2


C1 2.2u
C2 2.2u
R1 1M
32.768KHz
out put
F = 32.786KHz

2.2 THE COUNTER SEQUENTIAL CIRCUIT

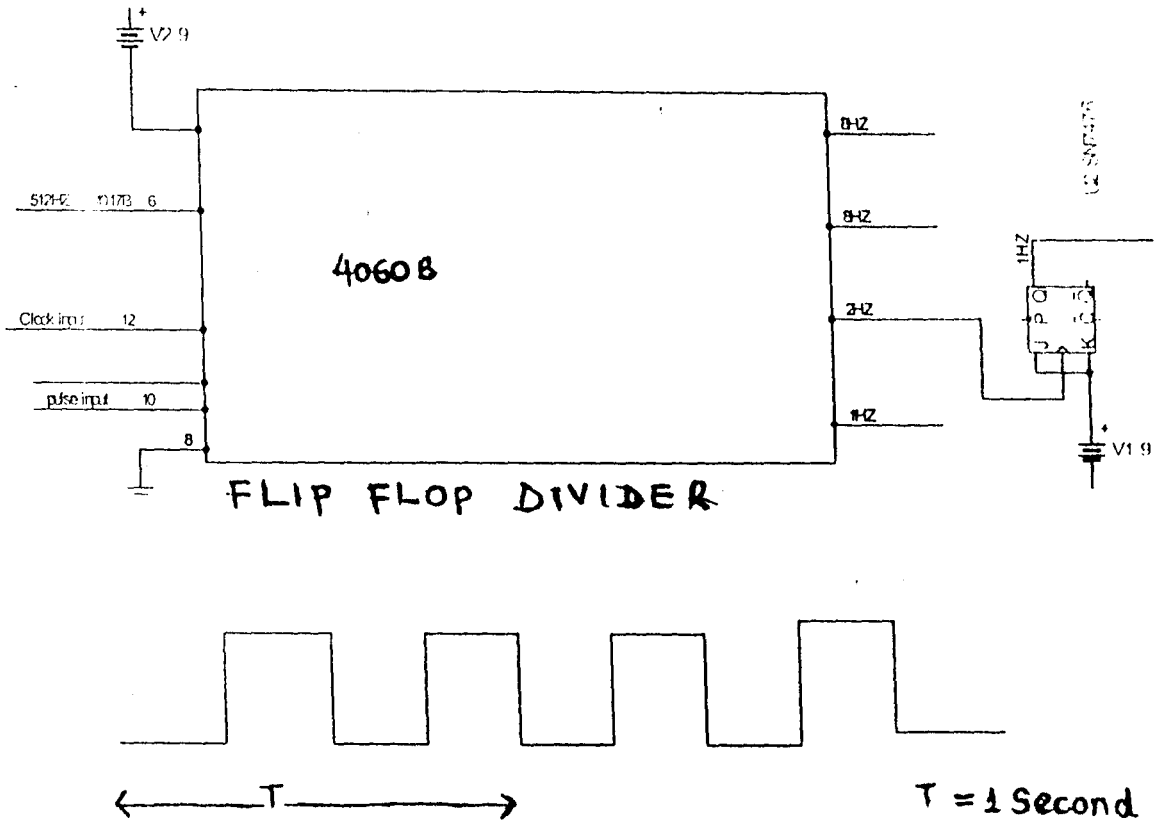
Counters are divided into 2 - main groups: asynehronous or ripple counter and synehronous counter despite the problem encountered with the ripple counters the simplicity of syrehronous counter makes them useful for application where their frequency limitation is not critical an there for synchronous counter has been chosen for this project.

DIVIDER BY 15- COUNTER

Many application of counter as frequency dividers digital clock fro example) require some other modulo but for this project me decided to use (CD 4060 B) Which is an oscillator divider. It has 14 fhip flops in side as component which divides are input frequently which is 32.7 86 by time.

However is flip flop is needed for the division to have second pulse period) but 40060B can only divide times to have a frequently of 243 which MOTT =seconds then an external J.K flip flop at toggle state is required which has 2Jla Fhip Flop inside one of them is used after the addition the frequently out put is I second. how ever the 2Jla flip flop IC used is 4027B.

The circuit disgram of the divider by is counter is shown below in figure 2.20.



the first state of the design Process is to set down the desire sequence and to examine it to see which state must change state at each step and what signal are available to initiate these changes. But J.la change state when its clóck input goes from to o for any given present state of the output the flip flop may be required to keep up any particular next state and the table sets out the necessary inputs at J and la for each of the four possibilities shown in the table below.

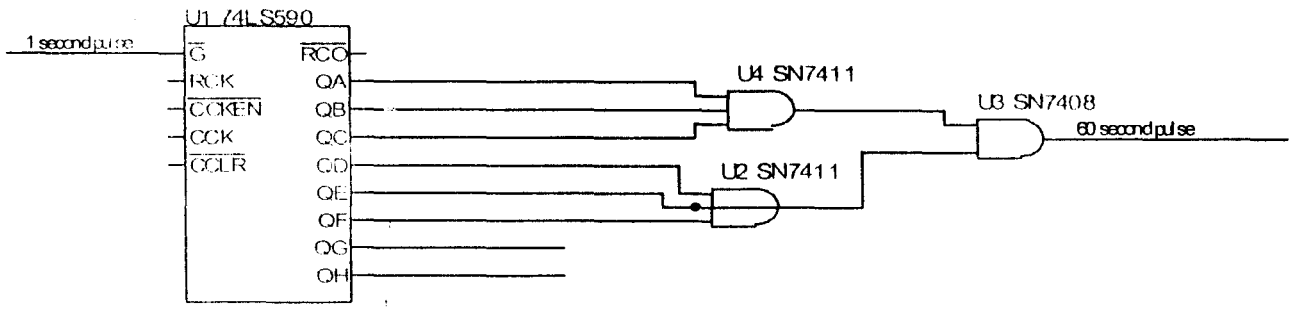
Present out put	Desired next out put	Required input	
Q	Q	J	K
0	0	0	x
0	1	1	x
1	0	X	1
1	1	X	o

Transition table for J - k flip flops

FOR MINUTE DIVISION.

Component CP4520 13 is used it is an 8- bit counter the counter starts counting from using the one below pulse the Jla counter resets itself back to OOOOOO(O) however an AmD gate decodes the binary (80) before reset so as o have a pulse during the period of the binary codes. The pulse share is give below in figure 2.31.

60 seconds



THE TRUTH TABLE FOR THE 8-BIT COUNTER

NPUTS	A	B	C	D	E	F	G	H	OUTPUTS
0	0	0	0	0	0	0	x	x	0
1	0	0	0	0	0	1	x	x	0
2	0	0	0	0	1	0	x	x	0
3	0	0	0	0	1	1	x	x	0
4	0	0	0	1	0	0	x	x	0
5	0	0	0	1	0	1	x	x	0
6	0	0	0	1	1	0	x	x	
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
59	0	0	0	1	1	1	x	x	1

We can deduce from the diagram that only 6 bits out of the 8- bit that are only function due to the fact that only 11110 (60) is required.

2.3 THE COUNT ACCUMULATORS.

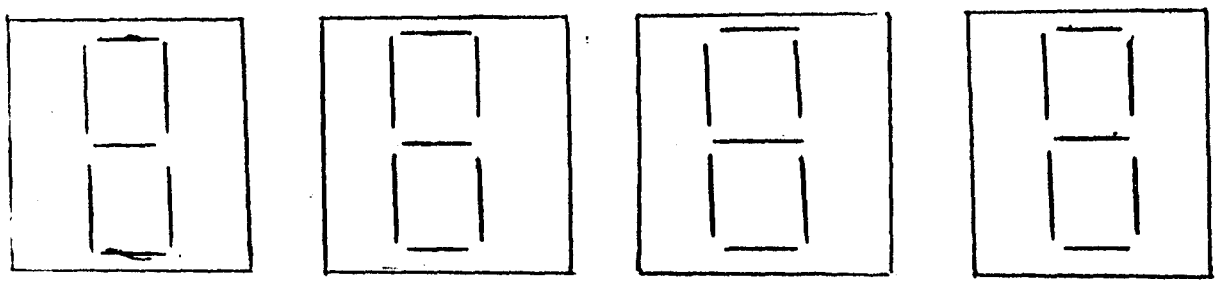
The count accumulation job is to count the input pulses and to serve as a temporary among while passing the current time through the deode into the time displays.

The clock has four naira counter which are grouped into 2 group two minute and the other two for reading hours

OUNT 1

Counter number 1 serves digit one (1) and counter 2 serves for digit 2

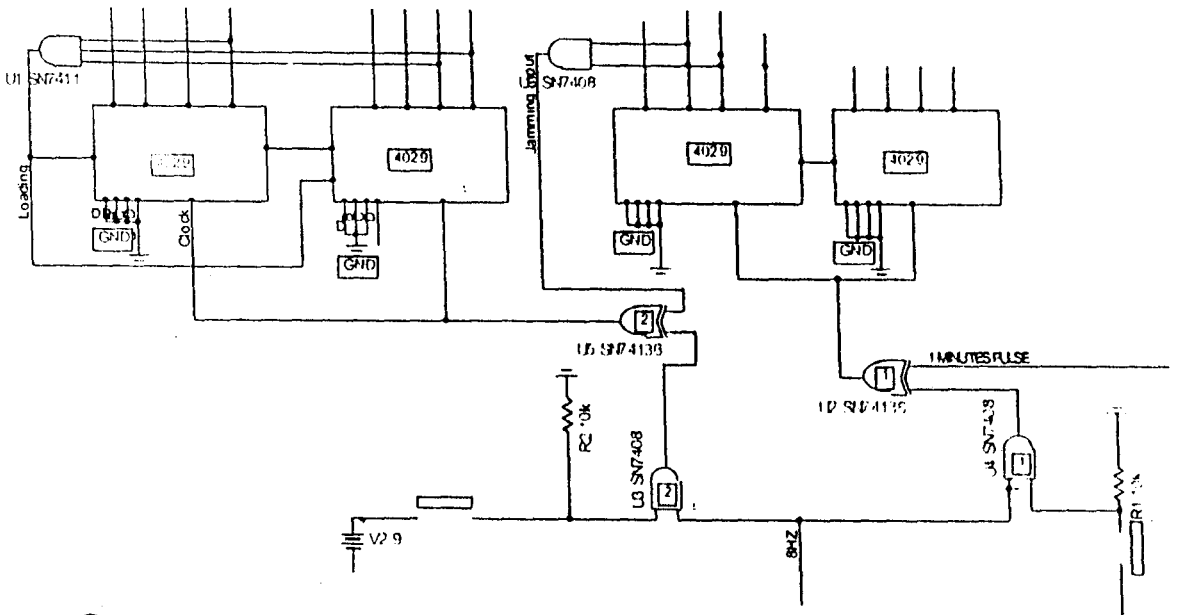
e digits are shown below:



Counter 1 counts from 0 9, but counter 2 counts fro 0 - 5 so that on ombining the counts, number 59 will be formed, Remembering that 60 econds is feed into the next group that is for hours.

However, it is important to note that as counter 2 start from 0 - 5, at hat moment that we have 59 going to 60, And gate 1 decodes 6.030 as o reset the jump back to 00: We have a count from 00 - 59, at 60 the whole counter starts from 00, the and gate out put now a cent every 60 minutes and operates the hour counter, the output passes through Or gate 2 before it can be used as a clock for the hour counter.

Its schematic diagram is shown in figure 2.40



CONTROL CIRCUIT FOR COUNTER 1 AND 2

HOURS GROUP

Hour counters consist of two (2) counters counting from 01 - 12. The counter 3 is a decade type counting from 0 - 9 9, but counter 4 is very different, it counts from 0 - 1. When the combine counter starts from 01 ---------- of ---------- 09 ----------10 ---------- 11----------12 13 the and gate 2 decoder decodes binary code 12 which in turn sets the whole count to 01 the output of the AND gate is connected to the preset input of the two counters involved. When the preset is high counter 3 loades 0001 (which is already at its heading input) and counter 40000 (which is already at its loading input).

However, "3" won't show because it turns to 01 at micro seconds so fast that it will not be noticeable, this effects gives a count of 01 - 12 periodically.

Furthermore, or gate and 2 are used to set hours and minutes respectively. Whenever set botton 1 or 2 are pressed logic 1 enters through the selected or gate and behaves as it the required check to counter advance the counter.

Or gates jump up input logic towards its inputs the truth table of an AND gate is show below:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Note: The output of the counters are connected to a group of butters (4 in number) one fore each counters.

2.4 MULTIPLEXERS (4503)

BUFFER

The buffers (4503) is a non investing buffer, it's enabling input is used to enable or cut off the incoming input toward the output.

When the enabling input is 0 (low), the code or logic flows, but when the enabling input is 1 high (high) the input codes do not flow (the code is cut off).

However, this mechanism of the butter is used to multiplex the outputs of the counter towards the only decoder (4511) which displays the digital on the display panel.

NOTE: Multiplexing is a technique used in communications and input/output operations for transmitting a number of separate signals simultaneously over a single channel or line. To maintain the integrity of each signal on the channel, multiplexing can separate the signals is a multiplexer.

The internal structure of the buffer is shown below in figure 2.5.0 for better understanding.

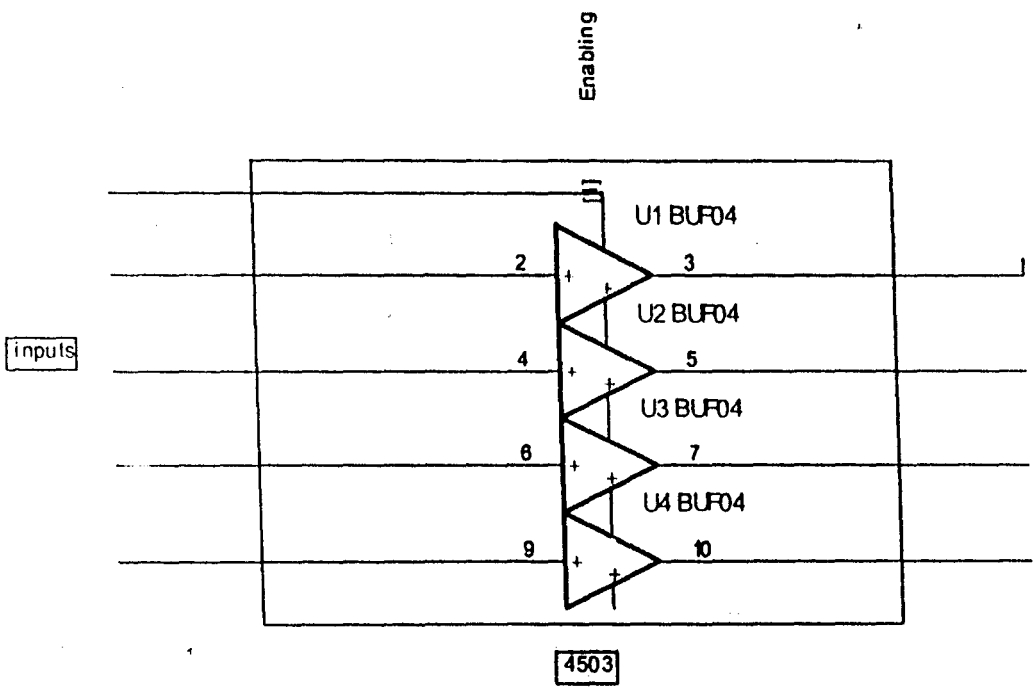


Fig 2.50

However, to check the functionality of the buffers a scanner will be required to be able to enable a buffer at a time to avoid conflictions, then a stepper is used (401703) to scan the buffers.

The truth table for the scanner is shown in below 2.5.0

		OUTPUT		
Clock	1	2	3	4
0	1	0	0	0
1	0	1	0	0
2	0	1	0	0
3	0	0	0	1
Back Again				
4	1	0	0	0
5				
6				

A truth table 2.50 for the stepper (4017B)

The 4017B operates in a mode that only one of the buffer will be enabled that is it is only one of the buffers that will be connected to the 7 - segment decodes (45113) the rate of the scanning connects each of the buffer with their output from the respective counter to the decoder.

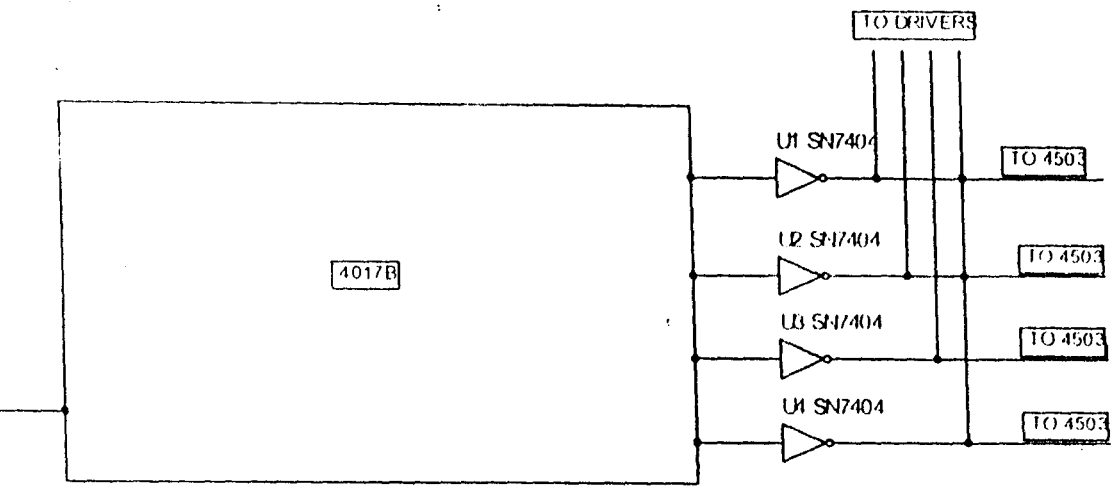


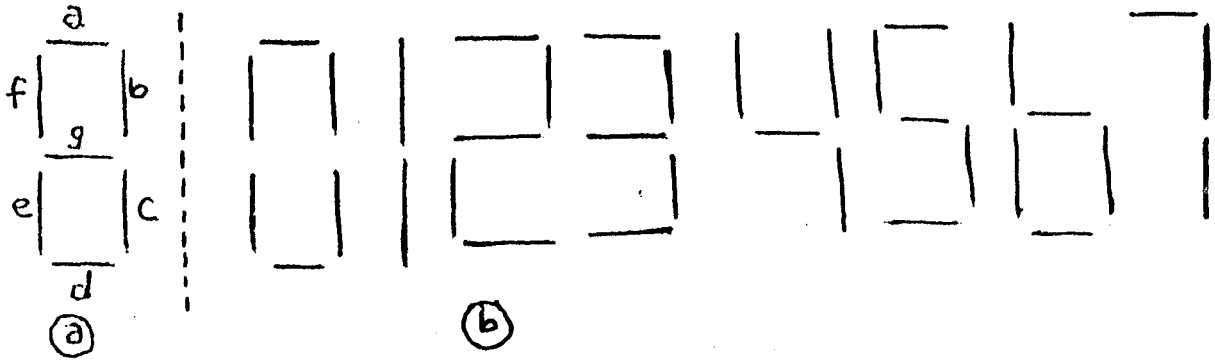
DIAGRAM OF INVERTER AND DRIVER.

DECODER/DRIVERS

any numerical displays use a 7 - segment configuration to produce decimental characters 0 - 9, 7 segments displays are used to convert - bit BCD number into a visible read out, each segment is made up of material that emits light when current is passed throughout. Modern id calculators, digital clocks, uses 7 - segment displays for their read - 7 - segments may be of L.E.D. types, LED which is commonly used hosen because of its brightness, low cost, reliability and compatibility h low voltage integrated circuit the figure below shows the 7 - segment angement.

(a) 7 Segment arrangement

(b) Active Segment for each digits.



The segments of the 7 - segment display turn on that which most closely approximate the shape of the decimal digital equivalent to the binary values of the input, figure (b) shows the patterns of segments which re used to display the various digits. Since the numbers to be presented must be between on and 9. Numbers greater than 9 should not appear on the inputs and the outputs corresponding to these prohibited inputs are written as don't cares. In the typical 7 - segment display shown in figure each segment appears at a terminal and all segments are connected in common to a supply terminal and all segments are connected as a command anode display. In which the positive side of the power supply is connected to the anode of each segment and a voltage (0) at the segment cathode lights the segment, or they may be connected as a common cathode display in which the negative side of the power supply is connected to the cathode of each segment, but for this project a common anode 7 - segment LED display is used the truth table for a common anode 7 - segment display is shown below in table 2.61

Truth table 2.61 for common anode connection display

Decimal Display	Input D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

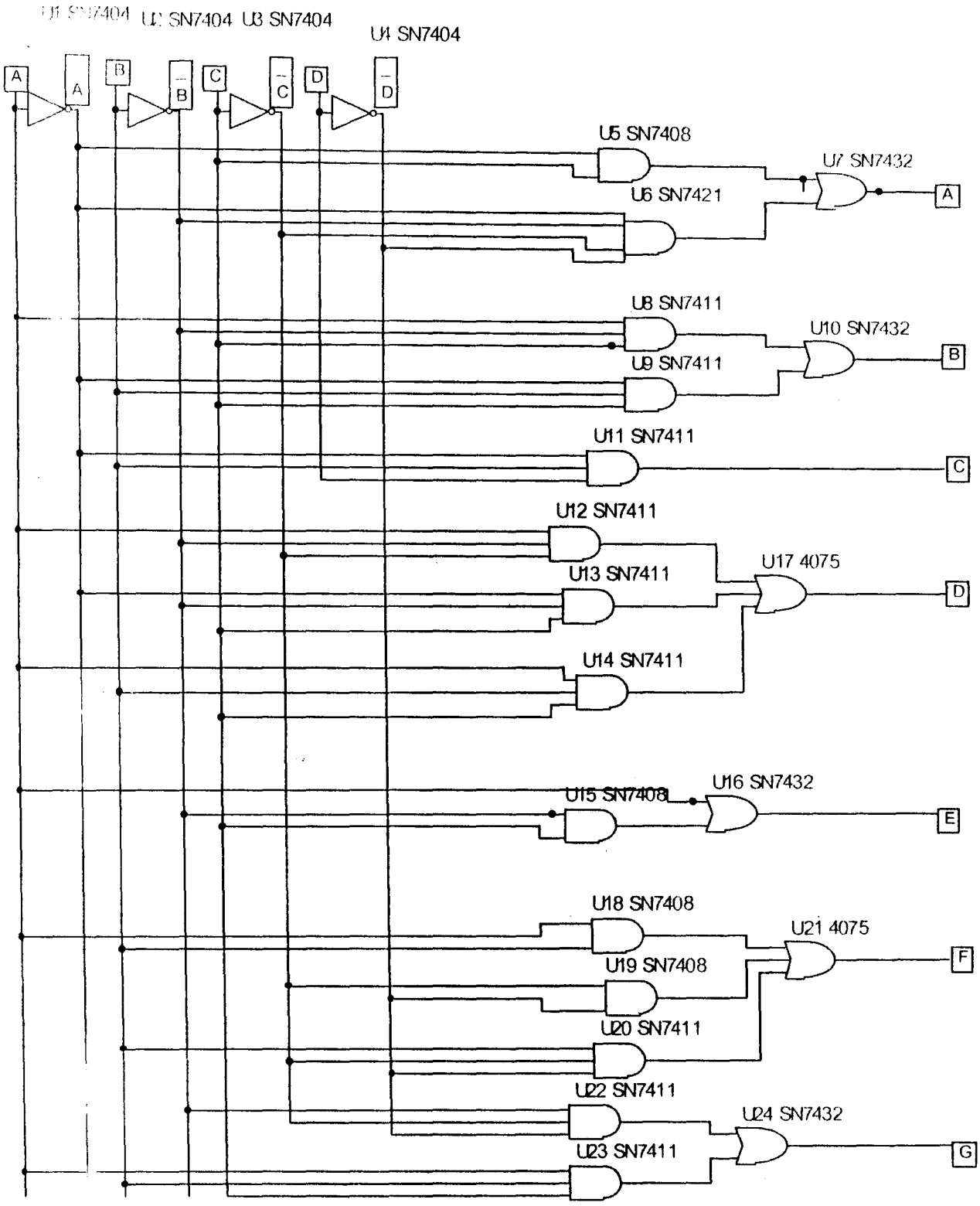


Figure shows a BCD for a 7-segment decoder driver

figure shows a BCD to 7-segment decoder/driverbeing used to drive a 7-segment LED READ-OUT.

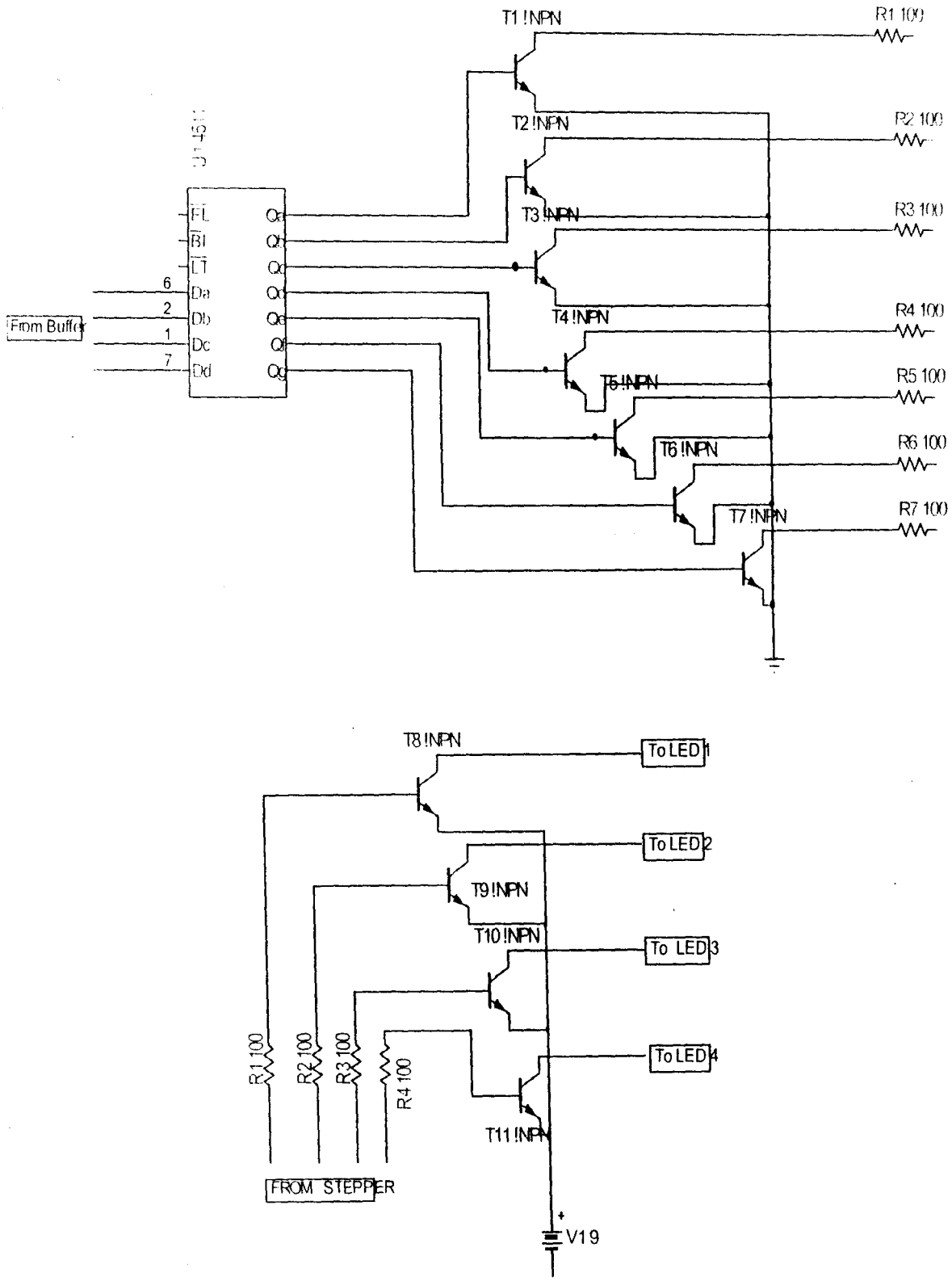


FIGURE bcd to 7-segment decoder/driver driving a common anode 7-segment LED display

which have different handling

When handling CMOS devices great care must be taken since they are very susceptible to damage from excessive voltage caused by static electricity and equipment which is not correctly earthed.

POINTS TO REMEMBER WORK WITH CMOS GATES

(a) Ti e unsed inputs to licc with a 1kz resistor or directly to ground.

(b) The outputs of CMOS gates should not be connected together

(c) The Maximum signal is 7V

(d) The Maximum Signal is 1-5 to 5-5v

(e) There is maximum fan out of 10 gates within each CMOS family.

(f) Install a 0.2-or0.02 Nu by pass capacitor is feasible

(g) Connecting head should not be more there 12to 124 inches (30-5 to 35 6(n) for standard CMOS.

3.2 THE COUNTER AND COMBINATIONAL CIRCUITS.

In the counter construction the divide by 15 counter was constructed with a divide by +4 counter feeding a ship flop 2Jia counter the count accumulator was also constructed using an 8-bit counter with only 6-bits functional.

The light emitting diodes (LEDS) were used as the 5 second indicator

they emit light when they are forward biased and should be counted with a service registor to limit the counrent flowing through it.the diagram of the LED is shoun in figure 3.1 and the coloure type used for this project is blue and green.

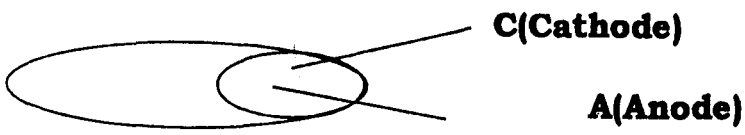


FIGURE 3.2

3.3 CONSTRUCTION

The power supply is a D.C. Energy VIa the use at a butterly cell.

The pulse generator was constructed using a quartz crustal oscillator as an Astable multivibrator with R-A I mr and a capacitor of 22 PF guing 32.7 st kt3.

The count accumulator section was constructed by using an 8 bit counter feeding decade counters.

The decoder/Driver display was constructed using the output of the count accumulator as its own inputs and a resistor of (1002) 200 of each was used to limit the current from the output at the deode the segment dispel.

The stages are arranged is such a way that the out put at one stage serves as the input to the other stages.

Which count and display hours from o through 23. This hours section

is different from the second and minutes section the circulatory in this section is sufficiently unusual to warant a closer investigation. Fig 1.01 shows the detailed circutory in the hours section it includes a BCD counter to count unit of the hours section and a MOD counter to count tens of hours the BCD counter counts only between OOO and 1001 and count up in response to the I pulse per hour signal coming from the minutes section.

The Inveter on the CPu input is needed because the BCD counter responds to pGTs and we want it to respond to NGTs that occurs when the Minutes section recycles back to ZERo hour for example at 7 cloua this counter will be at 0111 and its decoder/ display ciruitory will display the numeral 7 at the same time Q2 od mode counter will be low and its display will show a Zero this two displays will show 07 when the BCD counter is in 1001 (9) state and next toggle MOD 3 counter Q2Q from))to)1 this produces a mumeral 1 on the MOD 3 counter display and a numeral O" on the BCD display so that the combined display show 10 for10 O' clock.

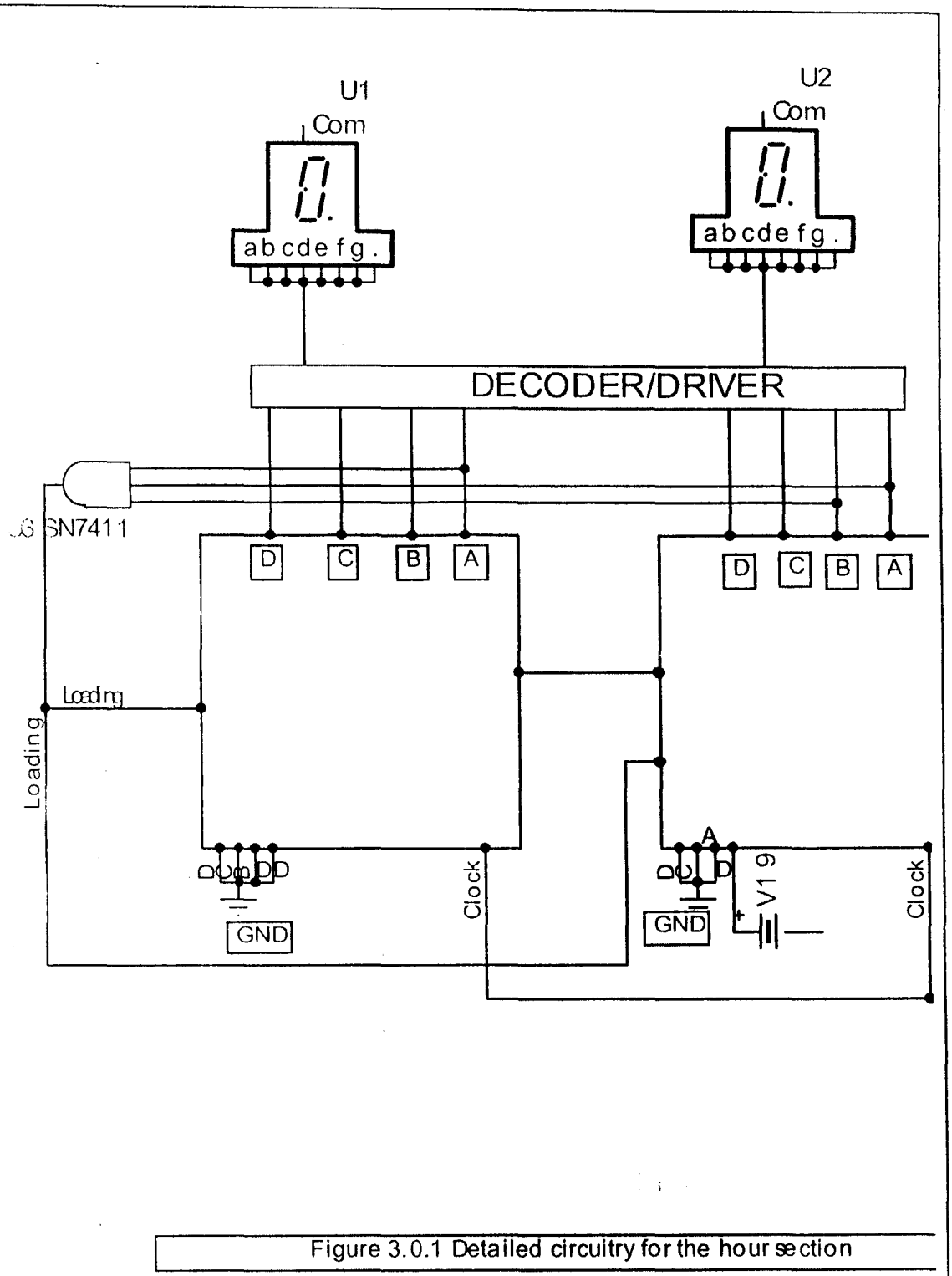


Figure 3.0.1 Detailed circuitry for the hour section

activates the MOD 3 counter and PT Input of the BCD counter. This cleas MOD counter to a and presets The BOD Counter to 000 the resuts is a display of"O" for 120 clock in the eary morning and night.

This report assumes that the reder has a basic lanowledge of both digital and power. A basic lanowledge of combinationaland sequential circuts helps us understand the time conuter and conbinational circult sections of the project. Also Litle hnowledge of power will help him understand the power section.

In order to understand the report more the first chapter thows some light on some necessary basic topics. The second chapter deals with thge desig component. the third chapter state how the design obective of the secon l chapter is achieved in the constructive faces. Chapter four goes to present. the falrication and the tests carried out.

REFERENCES.

1 Analysis and Design of Digital integrated circuits-second edition by David A. Hodges, Horale G. Jackson.

ii Digital Principles - second edition by reoger I. Tokheim .

iii Digital system principle and Applications -fourth edition Ronald J., Tocci.

iv Electronics II by D.C. Green.

v Electronic Cirucit - Digital and Analog by Charles A. Holt.

vi Knowledge in depth - Encyclopedia.

vii Micro processor and digital system -second edition by Douglas V. Hall.

viii Encarta -Encyclopedia.