COMPARATIVE EVALUATION OF TRAFFIC LIGHT REALIZATION USING COMBINATION AND MONOSTABLE MULTIVIBRATOR METHODS OF DESIGN.

BY

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"A PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF BACHELOR OF ENGINEERING TECHNOLOGY IN DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGER-STATE."

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CERTIFICATION

The undersigned certify that this project has been carried out by **Abdulsalam** Shakiru Shayo and has been read and approved as meeting the requirements of the Department of Electrical and Computer Engineering Technology, Minna, for a project report in partial fulfillment of the requirements for the award of the degree of Bachelor of Engineering Technology.

PROF. S.O. AJOSE
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DR. E.B. OYETOLA
(Ag. DEAN OF ENGINEERING SCHOOL) — DATE

EXTERNAL EXAMINER — DATE

DECLARATION

I hereby declare that this project work is a genuine one which was wholly and solely constructed by me under the supervision of Prof. S.O. Ajose, Chairman department of Electrical and computer Engineering, federal University of technology, Minna.

Information derived from published and un published work of others has been acknowledged in the text.

S.S.S

DEDICATION

This project work is dedicated to :

- Glory of almighty Allah.
- My late grand mum- Hajiya Wuraola A. Garba.
- My blood; Bayo, Dola, Joke, Sina, Tunde and Wole.

ACKNOWLEDGEMENT

Praise be to allah, the cherisher, the most gracious, the most merciful, sustainer of the world and peace and blessings of Allah be unto his messenger, Muhammad, the seal of all prophets. Praise be to Allah the lord of universe.

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I am grateful to all my lecturers in the school of Engineering who taught me and helped me in one way or the other during the course of my studies; especially: late engineer L.A Moses who started the supervision of this project work but due to Allah's will, was unable to end it. May his soul rest in perfect peace.

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I am indebted to authors and publishers of the enlightening works listed in the reference which has been consulted and quoted literally. My debt to these Writers will be sufficiently clean from the references made to them and if any remain unacknowledge, the oversight is unintentional.

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Oh, Allah; I am grateful to you.

- Shayo Salam

ABSTRACT

The project dealt with comparative analysis and evaluation of traffic light realization using combinational logic circuit and MONOSTABLE MULTIVIBRATOR methods of design.

The basic factors used in comparative analysis and evaluation are cost of production, space occupation, speed and reliability to know which of the design method is more considerable and economical for future environmental development.

In proceeding chapters, like in chapter one, introduction and literature review was dealt with, review the implication of traffic jam, also compared different methods of traffic light realization design and their mode of operation.

Problems statement and methodology was discussed in chapter two, stating various type of problems that has been encountered in traffic light implementation.

Chapter three deals with selection and design of components. Components selection and design was done in such a way that there will be a room for comparison between the two design methods.

In chapter four, Comparative evaluation of the design methods (combinational and monostable multvibrator) was carried out using the above stated factors. Most of the project work was performed

in this chapter because the design and its pin connection was done here too.

Finally, chapter five talks about the conclusion and recommendation where the appropriate design was recommended for future design.

TABLE OF CONTENTS

CHAPTER ONE

INTRODUCTION

"Traffic" means, the movement of people or vehicles along roads or streets, of ships in the sea, planes in the air space, movement of products on conveyor belts e.t.c.

Due to development and everyday increase in human population and vehicles, traffics leads to "Traffic jam or congestion", and this traffic congestion has being one of the utmost problem in our cities and towns in all corners of the world. Various accidents have resulted as a result of traffic congestion which leads to loss of lives and properties.

Attempt have been made in all ways to avoid if possible or reduced the problem of traffic congestion. Like in those days and up till today in most cities and towns in developing countries, traffic warders are being employed, making use of hand to control traffic. There are lot of imperfection in this method of traffic control due to fatigue during the period of working, poor conditions of service, risk taking, scaring and human feelings during and after fatal accidents, and mis-interpretation of sign given by warder in conjunction with rule - activities of some drivers.

For more efficiency and perfection in traffic control, different automatic traffic control methods have been adopted. They are:

Combination Logic Circuit type, Micro-processor type, Micro-computer type, Programmable logic Array (PLA) type e.t.c. These automatic traffic light control systems employ different types of lighting colours and the most commonly used lighting colours in traffic are: Red, Amber and Green. The meaning of these colours are;

i. Red - Stop.
ii. Red/Amber - Get ready to start moving.
iii. Green - Go.
iv. Amber - Get ready to stop.

The lighting of each bulb has duration which can be vary by using couples of capacitors and resistors, though in this project work we are not really concerned with the time duration but the evaluation of different design methods.

Automatic traffic light control are categorized into four (4) places:

A. Fixed time signal; the lighting duration of all the lights (Red, Amber and Green) are fixed or remain unchanged until they are reset.

B. Time variable signal: this works in such a way that the lighting periods change at specify time of the day for Red, Amber and Green lights.

C. Vehicle actuated signal: it works with the vehicle movement over a detector to an automatic controller gives signal or

controls the lights.

D. Computer control traffic: Area computer control traffic uses computer for the storage of a number of traffic plans designed to match all the various traffic conditions likely to be encountered. The computer sends instructions to all the various controllers in the area according to the particular plan selected. The computer also monitors the system to check for controller or detector faults and thus considerably speeds maintenance and avoid lengthy delays.

In this project, a comparative analysis and evaluation of the methods of designing traffic light is to be carried out, but before then a literature survey on the topic was carried out.

1.1 LITERATURE REVIEW

Due to the problems encountered with manually controlled traffic, many methods of controlling traffic automatically have been developed and some of the methods are as follows:

A. Combinational Logic Circuit method.

B. Monostable Multivibrator method.

C. Programmable Logic Array (PLA) method.

D. Microprocessor method.

E. Microcomputer method.

Here in Electrical and computer engineering department, F.U.T, Minna;

- In the work carried out by Austin A. in 1992, he made use of combinational logic method of designing.

- In Ogunkayode A. Olufemi's work of 1994, he made use of monostable multivibrator method to carry out the design of traffic light, and in the project work carried out by Ogungbesan A. Adeniyi in 1994, he made use of Programmable Logic Array (PLA) method of designing.

- In most advanced countries like America, Russian, France, they make use of Microprocessor and Microcomputers in implementing their traffic light control systems.

This project is concerned with comparative analysis and evaluation of two of the different methods of design (combinational logic circuit and Monostable multivibrator methods of design) using the following criteria:

- Production cost
- Reliability.
- Space.
- Speeds, and to therefore propose which is more suitable for implementation in our environment.

In chapter two, the problem statement and methodology of evaluation is presented.

In chapter three selection and designs of various components and modules are presented.

Chapter four talks about comparative evaluation of the design methods.

While in chapter five, conclusion and recommendation of the project topic was carried out. Where the suitable method of design for our environment was recommended for future execution.

CHAPTER TWO

PROBLEM STATEMENT AND METHODOLOGY

2.1 PROBLEM STATEMENT:

It is discovered that the traffic light controller implemented using combinational logic circuit has low reliability value due to too many connections of wires, too many components like capacitors, transistors, ICs, Diodes, e.t.c. The moment one of these components fails, the system as a whole fails or when there is disconnection of one of the connected wires, the system also fails.

Therefore, for economical and durability purposes it is required to carry out a comparative evaluation of combinational method of traffic light design and monostable multivibrator method of design using the following criteria and then give a recommendation for the traffic light which is more suitable and durable for implementation in our environment - Minna metropolis.

The criteria to be used for evaluations are;

i. Production cost.

ii. Reliability of the system.

iii. Speed and

iv. Space on printed circuit board (Vero board).

2.2 METHODOLOGY:

The methodologies employed for the comparative evaluation involves (consists) of the following steps:

i. The design of traffic light controller is carried out using combinational Logic Circuit method and Monostable Multivibrator method.

ii. The pin connections of the ICs and the wire connections of the analog electronic components involved are carried out and from here the evaluation of the two methods of designs proceeds.

iii. The evaluation is being carried out using the criteria: Production cost, reliability, space and speed, as follows:

- Production cost:

The bill of quantity, labor cost, and overhead cost prices of producing electronic systems in Minna town for each design is computed and compared to determine which is more cheaper. See the table 1 for the format of the bill of quantity:

TABLE 1 BILL OF QUANTITY TABLE

S/N	NAME OF ITEMS	QUANTITY	COST/ITEM	TOTAL COST
	TOTAL			

- Labor cost is also calculated. The labor cost is taken as 20% of the material cost, if direct labor used.

$$\text{Labor Cost (LC)} = \frac{\text{Material Cost(MC)} \times 20}{100} \quad ₦$$

- Overhead Cost:

The overhead cost includes all expenses incurred, different from material and labor costs and is taken as 10% of the cost material.

$$\text{Overhead Cost (OC)} = \frac{\text{Material Cost(MC) x 10}}{100} \quad ₦$$

Total production cost = MC + LC + OC

- Reliability:

The reliability of each of the design work would be calculated and compared to determine which one has higher reliability. The following formula is used for the calculation of the reliability ($R=e^{-\lambda t}$):

$$R = R_{IC} + R_T + R_D + R_C$$

R = Total reliability

R_{IC} = Reliability of Integrated Circuit (IC)

R_T = Reliability of Transistor

R_D = Reliability of Diodes

R_C = Reliability of Capacitors

- Space:

The number of ICs, Diodes, Resistors, Transistors, and Capacitors wold be controlled for each of the design and compared to determine which of the design occupied more spaces.

- Speed:

The speed of each of the design circuit diagram for the light would be determined. This is determined by using the following formula:

$Y = Y_{IC1} + Y_{IC2} + \ldots\ldots + Y_{ICn}$

Y = delay time

Y_{IC1} = delay time for IC1

Y_{ICn} = delay time for n IC

Y is determined through the longest wire connection on veroboard.

A comparative table of evaluation is drawn as shown in Table2 for clear comparison and analysis.

Table 2

	PRODUCT COST (₦)	RELIABILITY (NO UNIT)	SPACE (No IC)	SPEED (secs)
COMBINATIONAL LOGIC DESIGN METHOD				
MONOSTABLE MULTIVIBRATOR DESIGN METHOD				

CHAPTER THREE

COMPONENTS AND DESIGN OF TRAFFIC LIGHT CONTROLLERS

This section of the project consists of two design of traffic controller and Monostable multivibrator design of traffic light controller.

3.1 COMBINATIONAL LOGIC CIRCUIT DESIGN

The model of the traffic light controller system is illustrated pictorially as shown in Figure 3.1 below:

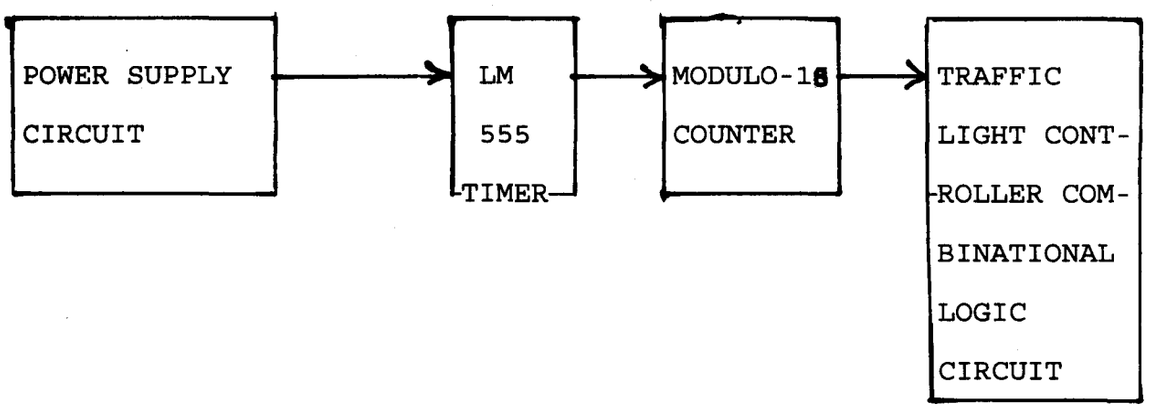


Fig. 3.10: pictorial model of the combinational traffic light controller.

Traffic light controller system was designed basically on electronic components like capacitors, diodes, IC's, resistors and transistors. The system is simply based on the sequential counting of a clock (synchorous) Mod-16-counter and the decoding output of Mod-16-counter using logic gates gives the sequential changes of the light. These decoded outputs are fed into

transistors which consequently switch "ON" the different bulb at different intervals. Stabilized 5V d.c supply was used for the integrated circuits while 12v d.c supply was used for the bulbs.

Traffic controller system is analyzed as follows:

- 240/9V and 240/12V step-down transformer was used as a source of power which the output from the secondary was rectified, filtered and regulated properly so that stabilized 5V and 12V d.c. supply was obtained to power the system.
- The timing pulses needed by the logic counter is generated using LM 555 timer, in an astable mode.
- Two dual JK flip-flop ICs (SN74107) counter was connected across the timer output.
- The counter output was combined together and decoded using combinational logic circuits which thus make the bulbs glow when necessary by switching the transistors respectively.

3.2 DESIGN OF REGULATED POWER SUPPLY

The most vital part of any electronic circuit is the source of power. Apart from the 240/9V and 240/12V a.c step down and the rectifiers, there is the need for a smoothing circuit and a stabilizing circuit. For this project, two power supply units are used, the first is the regulated 5V d.c which is used to fed the Ics and the second 12V d.c that supplies the bulbs. The circuit diagram for +5V and +12V were shown in Figures 3.20 and 3.21 respectively.

Fig 3.20: 5V d.c. regulated power supply circuit

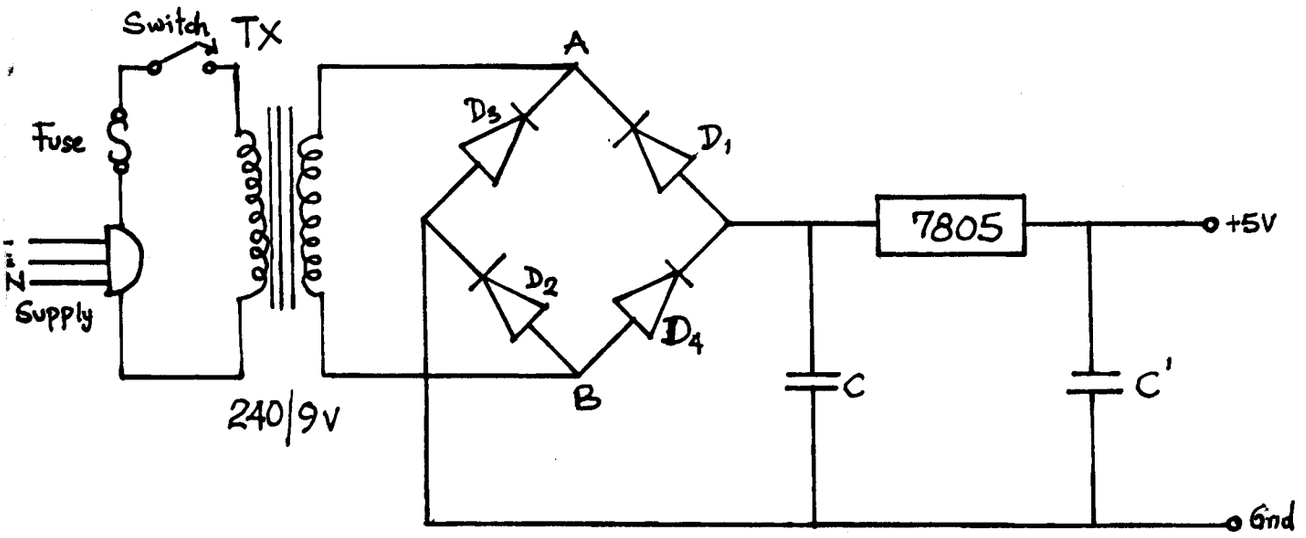
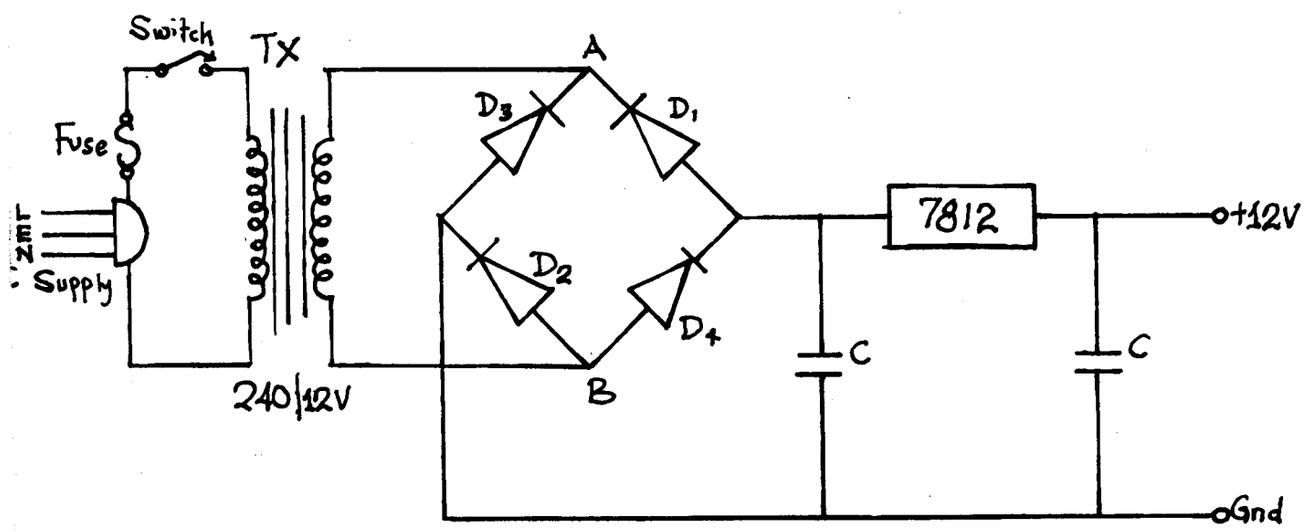


Fig. 3,21: 12 d.c Regulated Power Supply Circuit



When 240V a.c is fed into the input of the transformer, the transformer steps 240V down to its rating. Like in 240/9V, the transformer steps 240V down to 9V a.c. This 9V is then passed through a Bridge rectifier. This bridge rectifier circuit has four diodes, diagonally opposite pairs of which conduct simultaneously so that when point A is positive with respect to B, diodes D1 and D2 conduct, D3 and D4 being reverse biased. When point B is positive with respect to point A, diodes D3 and D4 conduct, while D1 and D2 are reverse biased as shown in Figures 3.20 and 3.21.

A undirectional currents and voltages were obtained from the rectifying th ough still contains some degree of alternating currents and voltages along its d.c counterpart.

3.2.1 SMOOTHING THE RECTIFIED A.C SUPPLY

Capacitors play an important role in this section of the circuitry shown in figures 3.20 and 3.21 especially for the smoothening activities in the power supply circuits and also to determine the frequencies of the timing pulses in the timer circuit. Though using Bridge rectifier, as used in the design would have reduced the a.c component to the minimum level but there is still a need to smoothing the rectifier's output. The capacitors (C) in Figures 3.20 and 3.21 was used as a filter, thus giving an output that is steady and devoid of the remaining a.c components. This capacitor is called "reservoir Capacitor"

and the other capacitor C' is improving the quality of the output of the regulators.

3.2.2 STABILIZING THE SUPPLY

As the load current increases from zero to infinity, the d.c output voltage from an ordinary power supply units decreases from maximum level to zero i.e load current is inversely proportional to the output voltage (V=IR). So, due to dropping in output voltage as a result of increase in load current, there is need to stabilize the voltage supply and this explains the reason for the use of the AN7805 voltage regulation as shown in Figure 3.20 and this AN7805 regulator provides protection against overloading and overheating of the circuit components.

Figure 3.20 is the circuit diagram of the regulated 5V that supplies ICs while Figure 3.21 is also the circuit diagram of regulated 12V which supply power to the bulbs.

3.2.3 USED COMPONENTS AND VALUES

AN7805 5V voltage regulator.

KIA7812 12V voltage regulator.

0.022 micro Farad ceramic capacitor (x2)

IN 4001 diode (x8)

2200 micro Farad/25V d.c Electrolytic capacitor

6800 micro Farad/25V d.c Electrolytic capacitor=r

240/9V a.c Transformer.

240/12V a.c Transformer.

switch (x2)

100 mA Fuse.

3.3 THE PULSE GENERATOR:

LM 555 Timer IC was used in an astable mode to generate the timing pulses needed by the logic counter. Basically, it consist of an SR flip-flop which set and reset are each controlled by an operational Amplifiers (used as voltage comparators). An eight pin DIL IC operates from supply rail voltages of (3-15)V and since Transistor-Transistor Logic (TTL) logic family was used in this project design, the timer IC in this case was operated from a d.c supply of 5V. The interval block diagram of LM 555 Timer is shown in Figure 3.30

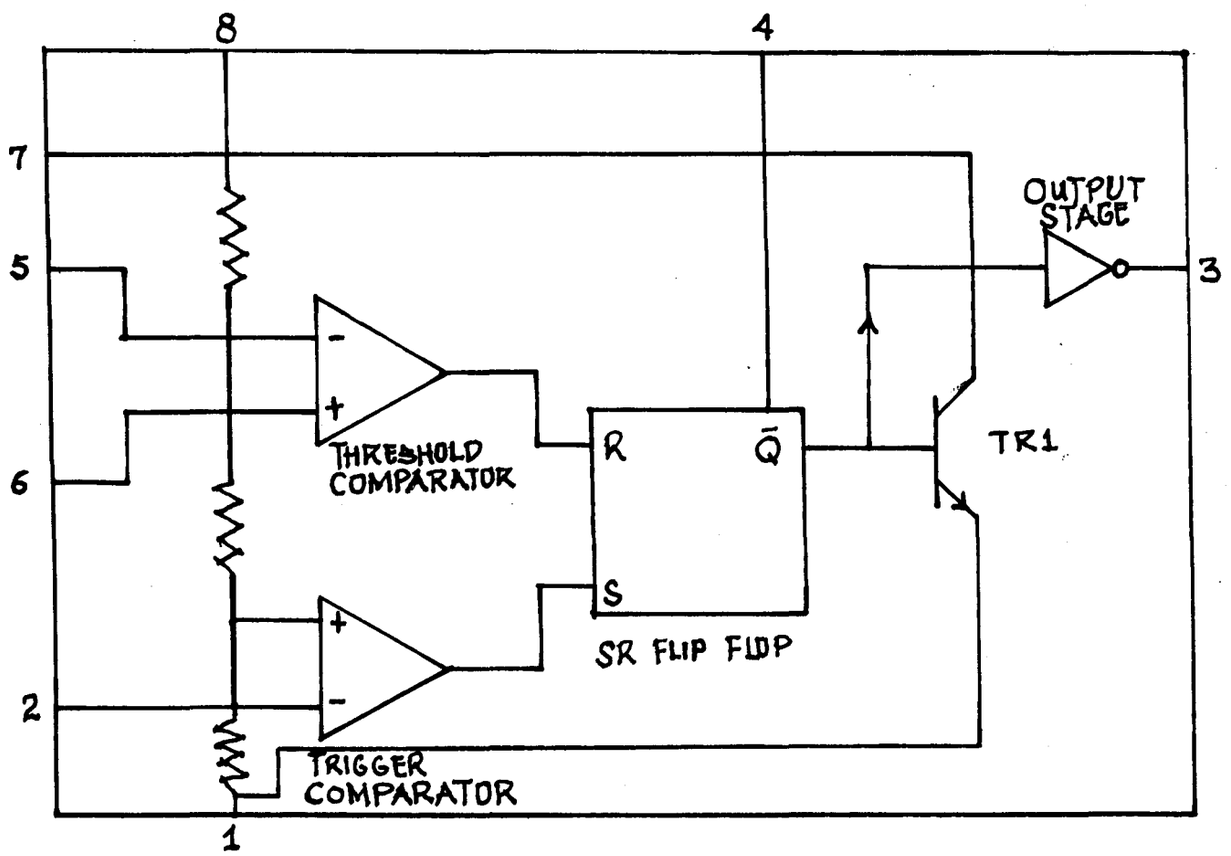


Fig. 3.3.1 ASTABLE OPERATION OF LM 555 TIMER

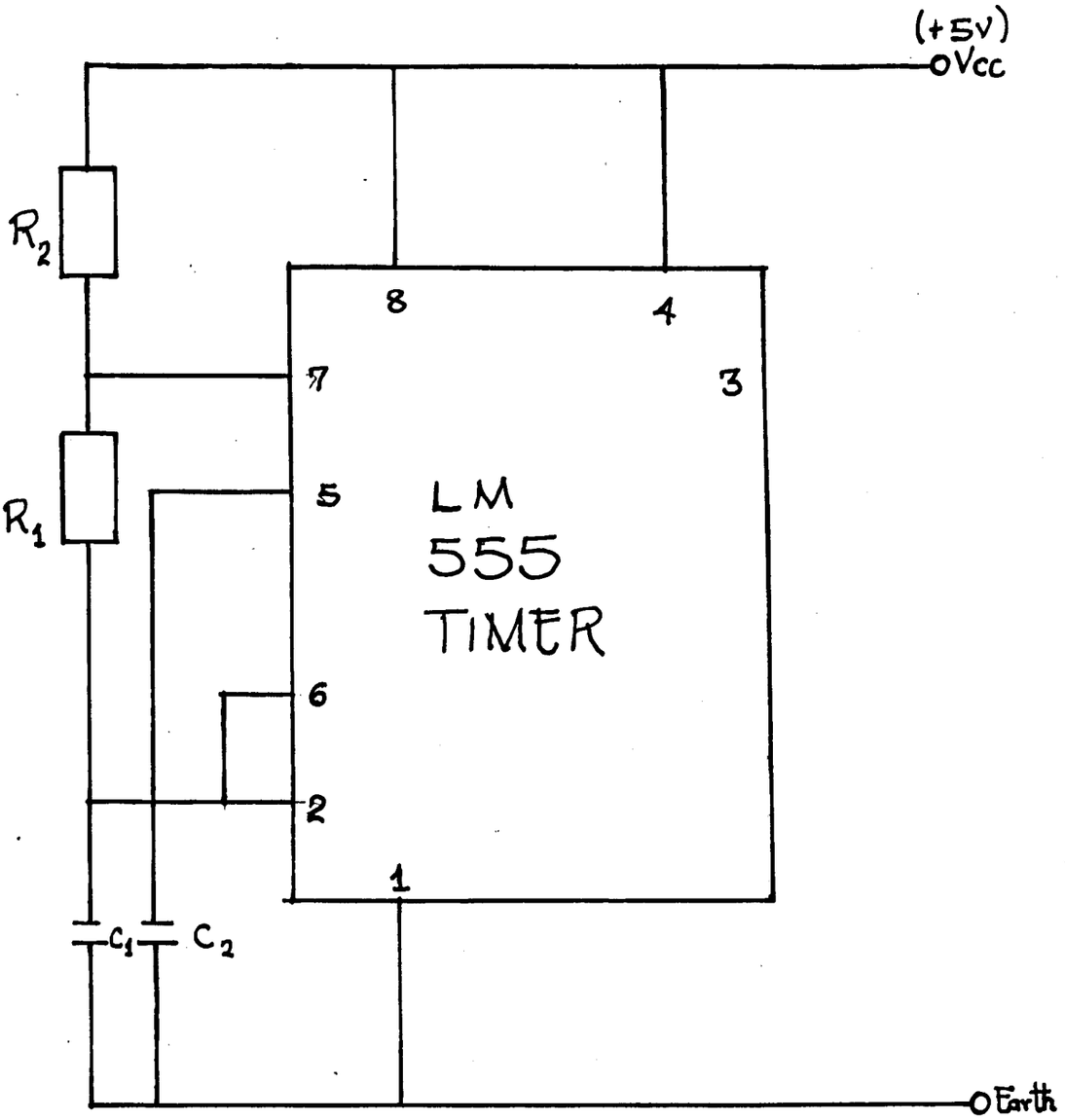


Fig. 3.31: Block diagram of pin Connection of LM 555 Timer

Pin 1: Ground	Pin 5: Control Voltage
Pin 2: Trigger Input	Pin 6: Threshold
Pin 3: Output	Pin 7: Discharge
Pin 4: Reset	Pin 8: Power Supply

The figure 3.31 shows block diagram of the pin connection of LM 555 Timer when connected in an astable mode.

Trigger (Pin 2) was connected to the Threshold (Pin 6) as shown in Figure 3.31. R1, R2, C1 and C2 are external components. Initially C1 charges up through R1 and R2 and when the voltage across it just more than 2/3 Vcc, the output from the Threshold comparator goes "high", and resets the flip-flop. When Q goes "high", there is existence of two outputs, firstly the output from the IC pin 3 goes low (since inverting output buffer is incorporated so that a considerable current can be source to, or sunk from, a load). Second, transistor (Tr1) switches ON (since its base is now +ve) allowing to discharge through it and R1.

Now when the voltage across C1 is below 1/3 Vcc, the output from the Trigger comparator goes "high" and sets the flip-flop. Q will thus go "low", also with two outputs. First, the output from the IC goes "high" and second, the transistor (Tr1) turns OFF (since its base is no longer +ve) so letting C1 charge up to 2/3 Vcc again through R1 and R2, as it did at the beginning. And this cycle is then repeated continuously giving an oscillatory, output with a rectangular wave from which is "high" while C1 is charging and "low" while it discharge.

Generally, the output is 'high' for longer period than it is 'low', since C1 charges through two resistors R1 and R2, but

discharges only through R1. LM 555 Timer using in an astable mode has one important factor which is the connection of reset (Pin 4) which is the "direct reset" for the flip-flop to +Vcc (+5V). If the voltage falls below approximately 0.7V, the astable will stop. Also, since the 555 Timer is used as an astable, the control voltage (Pin 5) was connected via 0.01 micro Farad capacitor to the neutral (0V).

LM 555 Timer wave form is shown in Figure 3.32.

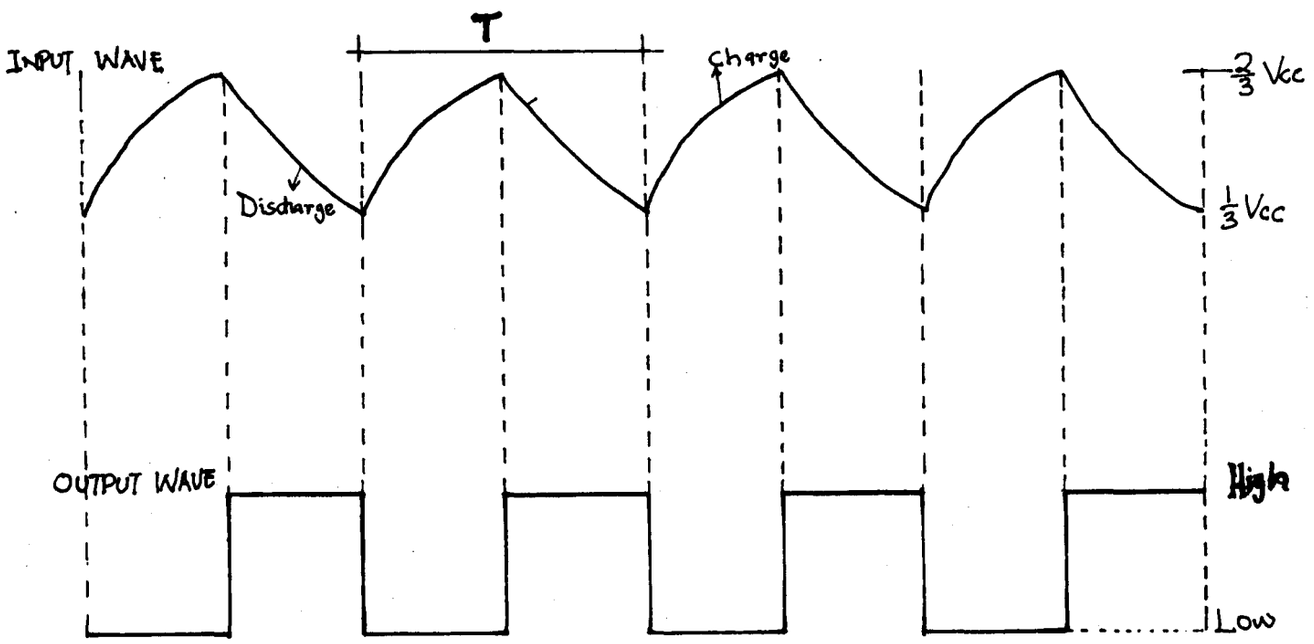


Fig. 3.32: Waveforms of the LM 555 Timer

The voltage across the capacitor when charging and discharging was given as calculated below:

i. When charging, the charging period is t, and calculated as follows;

$$2/3Vcc = Vcc - [Vcc - Vcc/3] \exp [-t/C1(R1 + R2)] \text{ ----(a)}$$

$$2/3Vcc = Vcc - 2/3Vcc \exp [-t/C1(R1+R2)] \text{ ----------(b)}$$

dividing through by Vcc,

$$2/3 = 1 - 2/3 \exp [-t/C1(R1+R2)]$$

$$2/3 \exp [-t/C1 (R1+ R2)] = 1 - 2/3 = 1/3$$

multiplying through by 3/2,

$$\exp [-t/C1(R1 + R2)] = 1/2$$

$$2 = \frac{1}{\exp [-t/C1(R1 + R)}$$

$$\log 2 = t/C1(R1 + R2)$$

$$t = c!(R1 + R2) \log 2$$

$$t = 0.693\ C1(R1 + R2) \text{ ---------- (b)}$$

ii. When discharging, the discharge period is td, and calculated as follows;

$$2/3Vcc = Vcc - [Vcc - Vcc/3]\exp[-td/C1R1]$$

$$2/3Vcc = Vcc - [2/3Vcc]\exp[-td/C1R1]$$

$$1/3Vcc = 2/3Vcc \exp[-td/C1R1]$$

dividing through by Vcc,

$$1/3 = 2/3 \exp[-td/C1R1]$$

$$1/2 = \exp [-td/C1R1]$$

$$2 = \exp [td/C1R1]$$

$$td = C1R1 \log 2$$

$$td = 0.6933C1R1 \text{ ---------- (c)}$$

The period time 'T' of the output wave form is thus given by,

$$T = t + td$$

$$T = 0.693C1[R1 + R2] + 0.693C1R1$$

$$T = 0.693C1R1 + 0.693C1R1 + 0.693C1R2$$

$$T = 0.693C1[2R1 + R2] \text{ ---------- (d)}$$

The operating frequency of the output waveform is,

$$F = \frac{1}{T} = \frac{1}{0.693C1(2R1 + R2)}$$

$$= \frac{1.44}{C1(2R1 + R2)} \text{ Hz ---------- (e)}$$

In this traffic light controller design, the period of each pulse was chosen to be 2 seconds, the capacitor's value was chosen to be 330 micro Farad and R2 was chosen to be 1K ohm.

From equation (d),

$$T = 0.693C1(2R1 + R2)$$

where T = 2 secs, C = 330 micro Farad and R2 = 1 K ohm.

$$2 = 0.693 \times 330x10^{-6}(2R1 + R2)$$

$$2 = 0228.69x10^{-6}(2R1 + 10^{3})$$

$$2 = 0.22869 + 457.38x10^{-6}R1$$

$$1.77131 = 457.38x10^{-6}R1$$

$$R1 = \frac{1.77131}{457.38 \times 10^{-6}} = \frac{1.77131}{457.38} \times 10^{6}$$

Therefore,

$$R1 = \frac{1.77131}{457.38} \times 10^{6}\,\text{ohm} = 3873 \text{ ohm.}$$

Which implies that,

R1 is approximated to 4K ohm.

Since R1 = 4K ohm, this gives the opportunity of using 10K ohm variable resistor in the design.

3.4 MODULOS -16- COUNTER DESIGN USING JK FLIP-FLOP

Electric counters are digital instrument that can be used to perform many functions like in data handling and control, counting the number of pulses in a controlled time interval, or alternatively the time interval between the pulses.

Synchronous (clock) counter and Asynchronous (ripple) counter are two types of digital counters.

A. ASYNCHRONOUS COUNTER

In Asychronous counter, the output of the last flip-flop, in a four binary counter will not change until four flip-flop propagation delays after a positive edge of the input clock (i.e the effect of a clock pulse ripples down through the chain of the

flip-flops and the outputs are not directly in synchronization with the clock).

There are some advantages and disadvantages in this type of counter;

i. Advantage;

- Inexpensive.

ii. Disadvantage;

- Generation of unwanted spikes during the transition from the first stage through the time at which the first flip-flop in a chain changes its output stage.

B. SYNCHRONOUS COUNTER

In this type of counter, all the flip-flops are directly clocked at the same time by the input clock thereby changing their output simultaneously. and this is the only advantage that clock counter is having over its ripple counterparts.

Modulo -16- counter is a counter that returns to its initial stage after 16 cycles of the input waveform.

The first step taken in Mod -16- Synchronous counter design is the construction of the basic transition table for flip-flop use in the design as shown in Figure 3.40.

J	K	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	Q^n

Fig. 3.40: Next state table for JK flip-flop.

where Q^{n+1} = The Q output after the clock transition.

Q^n = The Q output before the clock pulse occurred.

JK flip-flop is used because it is a universal one that can be connected as D or T - types.

In this particular Mod -16- counter design using synchronous JK flip-flop, if J=1 and K=0, the Q output becomes 1 at the next clock transition. If J=0 and K=1, the Q outputs are 0 (i.e J=K=0) when a clock transition occurs, the Q output remains the same, $Q^{n+1} = Q^n$ and finally, if J = 1 and K = 1 (i.e J=K=1), the Q output assumes the opposite state at the clock transition, $Q^{n+1}=\overline{Q}n$ and this opposite state at the clock transition is refereed to as "Toggling".

Basic transition table for the JK flip-flop and counter state table were shown in Figures 3.41 and 3.42 respectively.

ORIGINAL STATE (Q^n)	NEXT STATE Q^{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	0	1
1	1	1	0

X = "dont care"

Fig. 3.41 Transition table for JK flip-flop

DECIMAL	PRESENT STATE Q^n W X Y Z	NEXT STATE Q^{n+1} W X Y Z	Jw	Kw	Jx	Kx	Jy	Ky	Jz	Kz
0	0 0 0 0	0 0 0 1	0	X	0	X	0	X	1	X
1	0 0 0 1	0 0 1 0	0	X	0	X	1	X	X	1
2	0 0 1 0	0 0 1 1	0	X	0	X	X	0	1	X
3	0 0 1 1	0 1 0 0	0	X	1	X	X	1	X	1
4	0 1 0 0	0 1 0 1	0	X	X	0	0	X	1	X
5	0 1 0 1	0 1 1 0	0	X	X	0	1	X	X	1
6	0 1 1 0	0 1 1 1	0	X	X	0	X	0	1	X
7	0 1 1 1	1 0 0 0	1	X	X	1	X	1	X	1
8	1 0 0 0	1 0 0 1	X	0	0	X	0	X	1	X
9	1 0 0 1	1 0 1 0	X	0	0	X	1	X	X	1
10	1 0 1 0	1 0 1 1	X	0	0	X	X	0	1	X
11	1 0 1 1	1 1 0 0	X	0	1	X	X	1	X	1
12	1 1 0 0	1 1 0 1	X	0	X	0	0	X	1	X
13	1 1 0 1	1 1 1 0	X	0	X	0	1	X	X	1
14	1 1 1 0	1 1 1 1	X	0	X	0	X	0	1	X
15	1 1 1 1	0 0 0 0	X	1	X	1	X	1	X	1

Fig. 3.42: Modulo -16- counter state table

Further simplification of the design is being carried out use Karnaugh Map as shown in Figure 3.43.

I. FOR Jw:

WX / YZ	00	01	10	11
00	0	0	X	X
01	0	0	X	X
10	0	1	X	X
11	0	0	X	X

J_w = BCD

II. FOR Jx:

WX / YZ	00	01	11	10
00	0	X	X	0
01	0	X	X	0
10	1	X	X	1
11	0	X	X	0

J_x = CD

III. FOR Jy:

WX YZ	00	01	11	10
00	0	0	0	0
01	1	1	1	1
10	X	X	X	X
11	X	X	X	X

$J_y = D$

IV. FOR Jz:

WX YZ	00	01	11	10
00	1	1	1	1
01	X	X	X	X
10	X	X	X	X
11	1	1	1	1

$J_z = 1$

FOR Kw:

WX YZ	00	01	11	10
00	X	X	0	0
01	X	X	0	0
10	X	X	1	0
11	X	X	0	0

K_W = BCD

FOR Kx:

WX YZ	00	01	11	10
00	X	0	0	X
01	X	0	0	X
10	X	1	1	X
11	X	0	0	X

K_x = CD

FOR KY:

WX / YZ	00	01	11	10
00	X	X	X	X
01	X	X	X	X
10	1	1	1	1
11	0	0	0	0

$K_y = D$

FOR Kz:

WX / YZ	00	01	11	10
00	X	X	X	X
01	1	1	1	1
10	1	1	1	1
11	X	X	X	X

$K_z = 1$

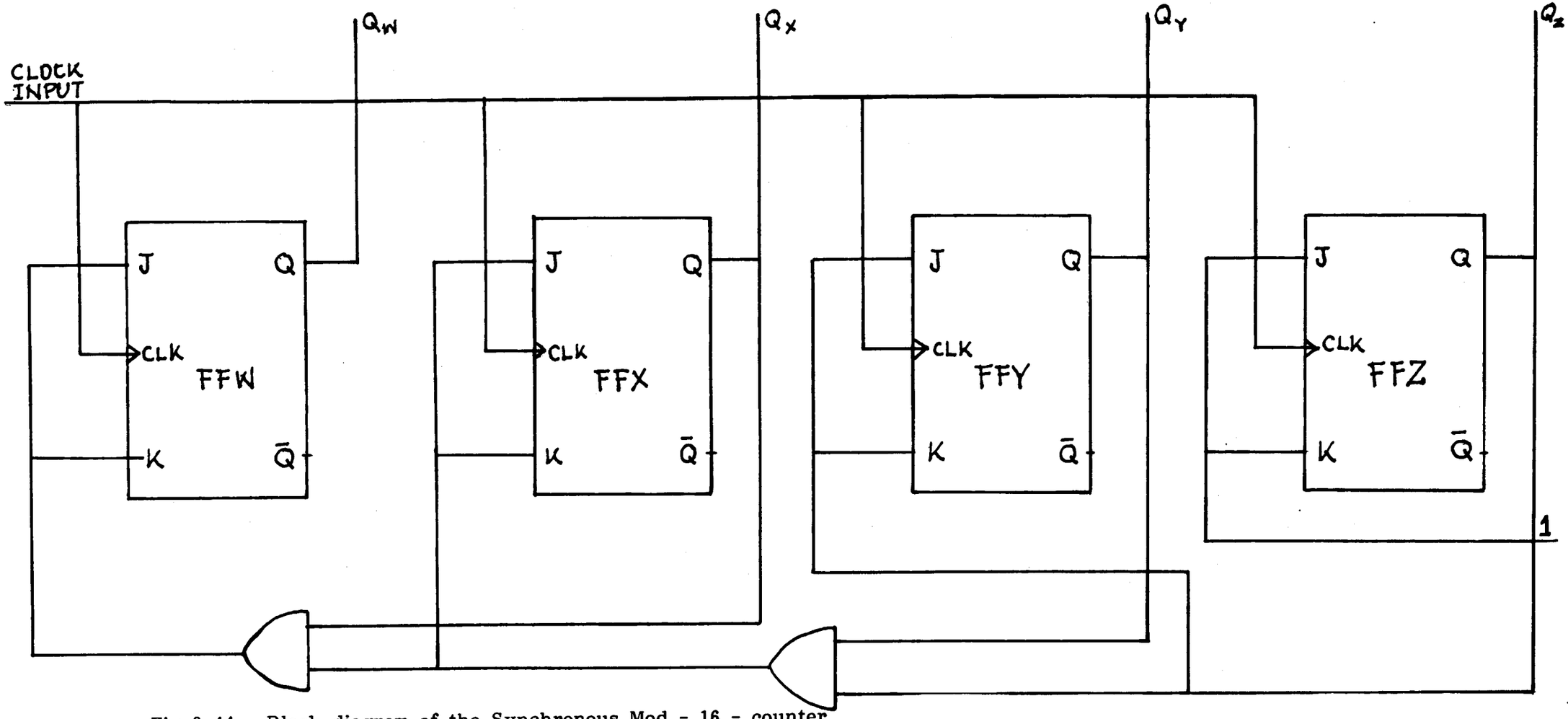


Fig 3.44: Block diagram of the Synchronous Mod - 16 - counter

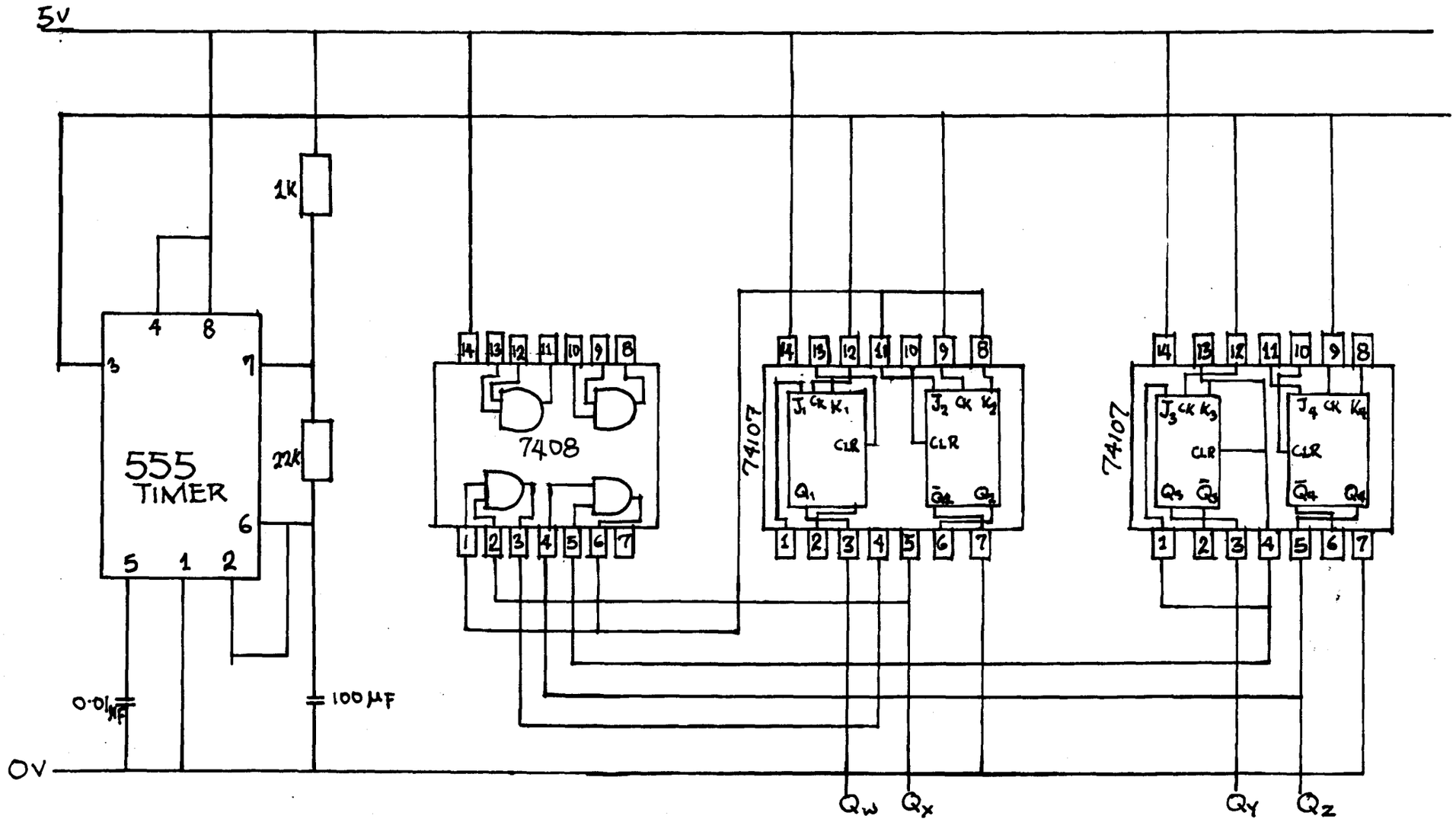


Fig 3·45. Circuit diagram of mod-16-Counter showing ICs and 555 timer connections

3.5 COMBINATIONAL LOGIC CIRCUIT TRAFFIC LIGHT CONTROLLER

The operational of the traffic light controller is shown in the Table 3.50 using M0d -16- counter as a counting element.

DECIMAL	W	X	Y	Z	R	A	G	PULSES (SECS)
0	0	0	0	0	1	0	0	2
1	0	0	0	1	1	0	0	2
2	0	0	1	0	1	0	0	2
3	0	0	1	1	1	0	0	2
4	0	1	0	0	1	0	0	2
5	0	1	0	1	1	0	0	2
6	0	1	1	0	1	0	0	2
7	0	1	1	1	1	0	0	2
8	1	0	0	0	0	0	1	2
9	1	0	0	1	0	0	1	2
10	1	0	1	0	0	0	1	2
11	1	0	1	1	0	0	1	2
12	1	1	0	0	0	0	1	2
13	1	1	0	1	0	0	1	2
14	1	1	1	0	0	1	0	2
15	1	1	1	1	0	1	0	2

Table 3.50: Truth table of counting order.

Some boolean algebra had to be performed in order to determine which output will be decoded by the logic gate (i.e W,X,Y,Z).

i. FOR RED:

$\bar{W}\bar{X}\bar{Y}Z + \bar{W}\bar{X}\bar{Y}Z + \bar{W}\bar{X}YZ + \bar{W}\bar{X}YZ + \bar{W}X\bar{Y}\bar{Z} + \bar{W}X\bar{Y}Z + \bar{W}XY\bar{Z} + \bar{W}XYZ$

$= \bar{W}\bar{X}\bar{Y} + \bar{W}\bar{X}Y + \bar{W}X\bar{Y} + \bar{W}XY$

$= \bar{W}\bar{X} + \bar{W}X$

$= \bar{W}(\bar{X}+X)$

$=\bar{W}.$

ii. FOR AMBER:

$WXY\bar{Z} + WXYZ$

$= WXY(\bar{Z}+Z)$

$= WXY.$

iii. FOR GREEN:

$W\bar{X}\bar{Y}\bar{Z} + W\bar{X}\bar{Y}Z + W\bar{X}Y\bar{Z} + W\bar{X}YZ + WX\bar{Y}\bar{Z} + WX\bar{Y}Z$

$= W\bar{X}\bar{Y}\bar{Z} + WX\bar{Y}\bar{Z} + W\bar{X}\bar{Y}Z + WX\bar{Y}Z + W\bar{X}Y\bar{Z} + W\bar{X}YZ$

$= W\bar{Y}\bar{Z}(\bar{X}+X) + W\bar{Y}Z(\bar{X}+X) + W\bar{X}Y(\bar{Z}+Z)$

$= W\bar{Y}\bar{Z} + W\bar{Y}Z + W\bar{X}Y$

$= W\bar{Y}(\bar{Z}+Z) + W\bar{X}Y$

$= W\bar{Y} + W\bar{X}Y$

$= W(\bar{Y}+\bar{X}Y)$

$= W(\bar{Y}+\bar{X})$

$= W(\bar{Y}+\bar{X})$

The output of the binary counter is then decoded with the

designed combinational logic circuit.

Karnangh Map (a system of reducing Boolean expressions using a matrix of 1's and 0's) can be used to simplify Boolean algebra as shown in Tables 3.51.

I. FOR RED:

ZY / XW	00	01	10	11
00	1	1	1	1
01	0	0	0	0
11	0	1	1	0
10	1	1	1	1

==> RED = W

TABLE 3.51(a)

II. FOR AMBER:

ZY / XW	00	01	10	11
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0

10	0	0	0	0

==> AMBER = WXY

TABLE 3.51(b)

III. FOR GREEN:

ZY / XW	00	01	10	11
00				
01	1	1	1	1
11	1	0	0	1
10	0	0	0	0

TABLE 3.51(c)

$= W\bar{X} + W\bar{Y}\bar{Z} + W\bar{Y}Z$

$= W\bar{X} + W\bar{Y}(\bar{Z}+Z)$

$= W\bar{X} + W\bar{Y}$

$= W(\bar{X}+\bar{Y})$.

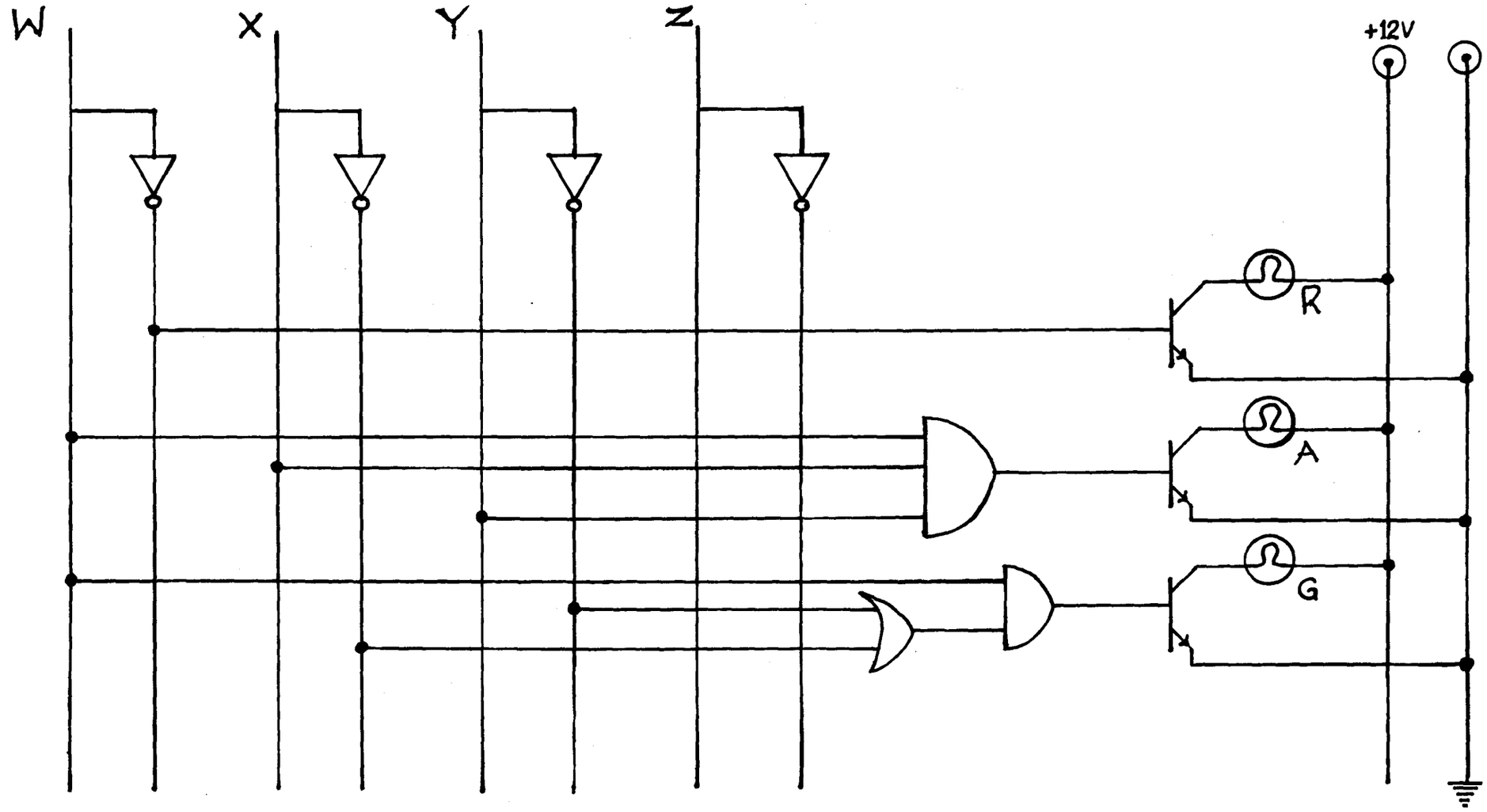


Fig. 3.52: COMBINATIONAL LOGIC CIRCUIT

3.6 THE OUTPUT STAGE

Combinational Logic gates is use to combined different output of the Mod -16- counter, and the output of the gates are then connected to different transistors each. A particular final output is connected to the base of a transistor, while the ammeter of the transistor is connected to neutral line (OV) the output of the transistor is connected to bulb. The collector is then connected to one of the bulb pin, while the other bulb pin is connected to the 12 volts d.c regulated supply. Once the logic is 'high' the transistor automatically switch ON the bulb attached to it and this remains for the duration of which the logic is 'high'. Once the logic goes 'low', the bulb goes OFF.

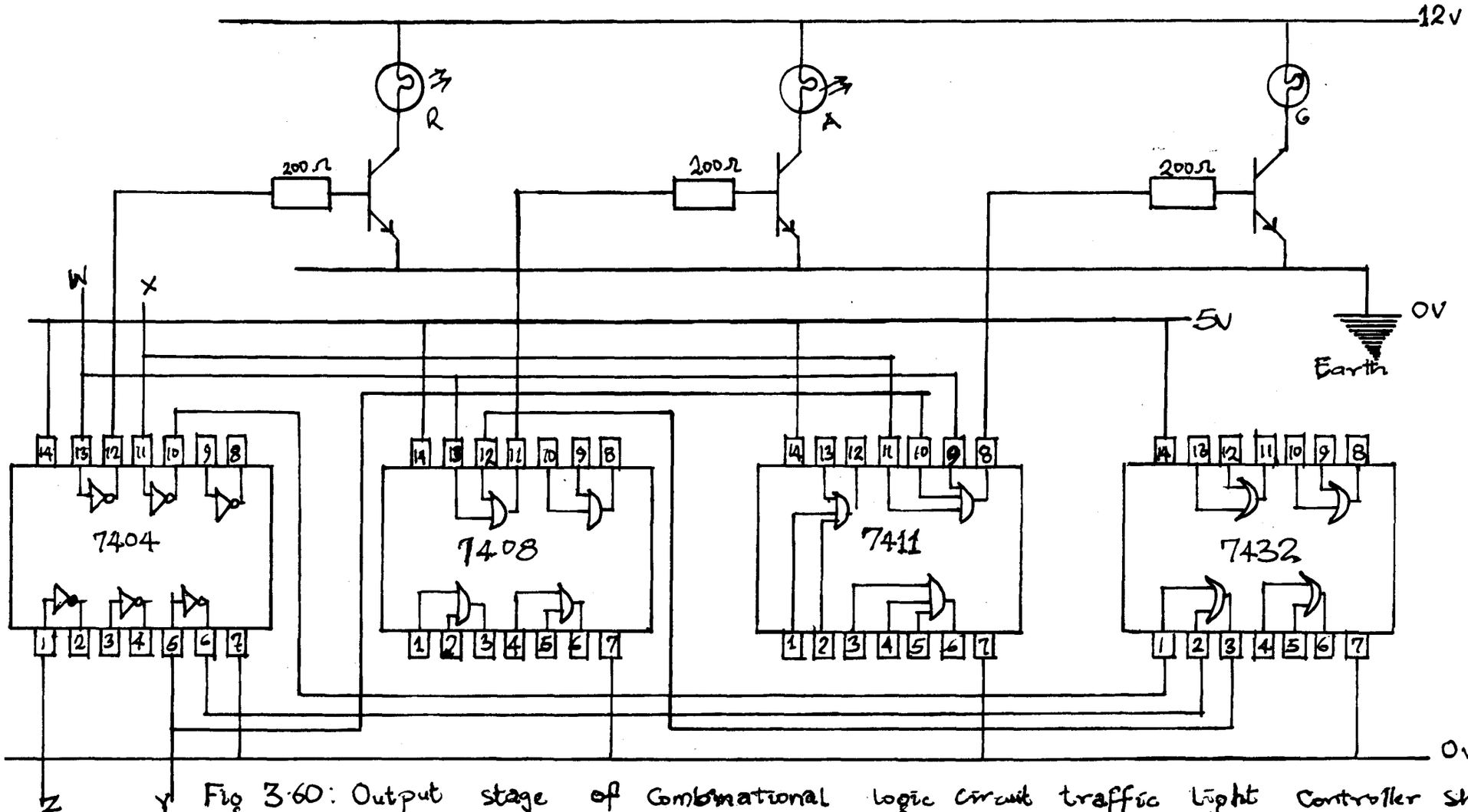


Fig 3·60: Output stage of Combinational logic circuit traffic light Controller Showing logic gate connection

3.7: COMPONENTS AND VALUES

SN 7411 (x1) Quad 3-input AND gate.

SN 7432 (x1) Quad 2-input OR gate.

SN 7404 (x1) Hex Inverter.

SN 7408 (x2) Quad 2-input AND gate.

SN 74107 (x2) Dual JK flip-flop.

LM 555 Timer.

Capacitor C=330 micro Farad/25V

Capacitor C=0.01 micro Farad

BFY52 (x3) Transistor.

12V, 5W(x3) Bulb.

Resistor R1 = 4K ohm.

Resistor R2 = 1K ohm.

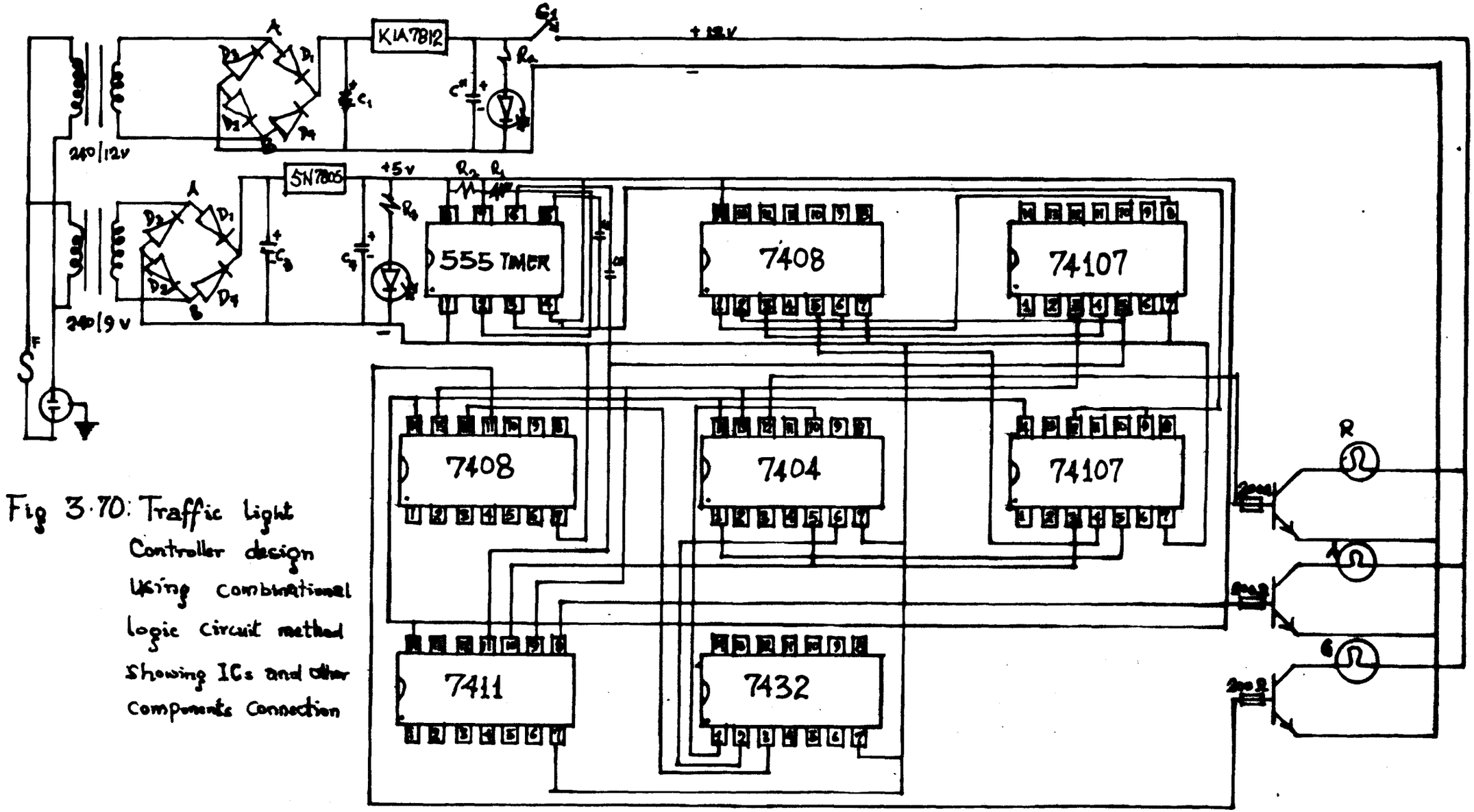


Fig 3·70: Traffic light Controller design using combinational logic circuit method showing ICs and other components connection

3.8 TRAFFIC LIGHT CONTROLLER DESIGN USING MONOSTABLE MULTIVIBRATOR.

The block diagram of the light controller using Monostable multivibrator is shown in Fig. 3.80.

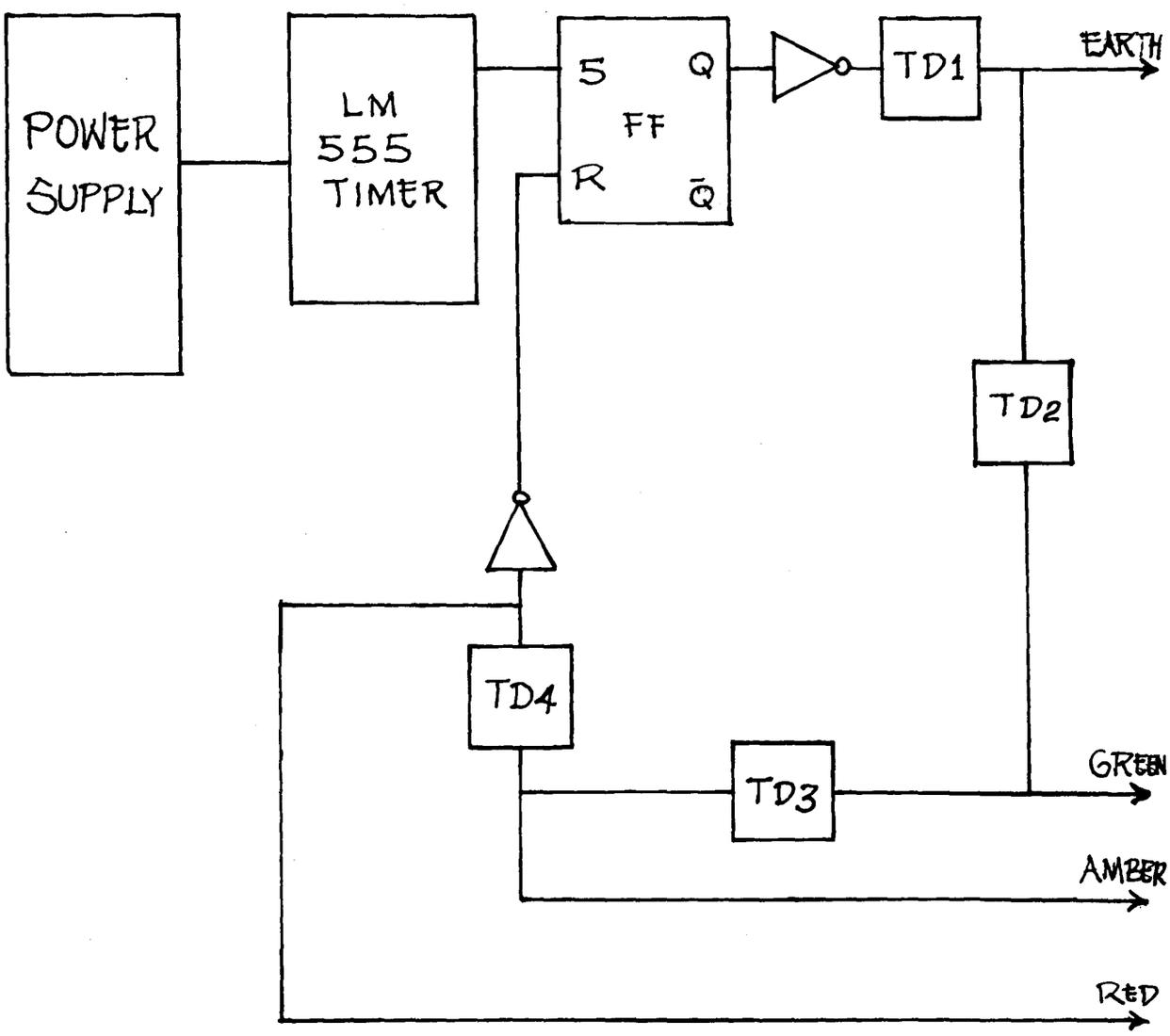


Fig. 3.80: Block diagram of traffic light controller using mono stable multivibrator.

The design for the power supply and the 555 Timer has been done in sections 3.2 and 3.3.

The next thing is to compute the time delay for the four multivibrators. The 555 timer here generates a signal of 1 pulse per sum of the delay times 30.3 secs.

3.8.1 CALCULATION OF THE TIME DELAY

In any circuit where time delay is required, Multivibrator are mostly used. These Multivibrators are categorized into three:-

- Astable or free-running Multivibrator: which has no stable states. It switches at a rate determined by the circuit components from a state to another. It generates a continuous stream of almost square wave pulses which is used to produce timing pulses for keeping the different part of a digital system, and this is one of the importance.

- Bistable Multivibrator: this has two stable states. External trigger or clock pulses makes it to switch from one stage to another.

They are normally refereed to as memory type circuits because in any digital systems, it is used to store the binary digits of '0' (low) and '1' (high) output.

- Monostable Multivibrator: is a device that causes delay by converting a pulse of unpredicted length of time into a square pulse of predicted length (voltage). Monostable Multivibrator is

also refereed to as one shot multivibrator.

This project work, for the time delay, Monostable (one shot) Multivibrator is use. And SN74121 type is used because it is a non-triggable one, which when stimulated, releases its pulse, but however locks any further incoming information until the full pulse duration and can be express mathematically as follows:

$$T = 0.7RC$$

where C = Capacitor value.

R = Resistor value.

T = Time duration of the pulse.

Various calculations carried out are as follows:

(a) FOR RED:

The first signal means "wait don't cross" and the time delay (TD1) is calculated as shown below:

When R = 15K ohm and C = 470 micro Farad

$T = 0.7\ RC$

$T = 0.7 \times 15\times10^{3} \times 470\times10^{-6}$

$= 4.9$ secs

==> TD1 = 4.9 secs

(b) FOR GREEN:

Green signals means "Cross" and the delay time (TD2) is calculated as follows:

when R = 30K ohm and C = 470 micro Farad.

T = 0.7RC

T = 0.7 x $30x10^3$ x $470x10^{-6}$

= 9.9 secs.

==> TD2 = <u>9.9 secs</u>

(c) <u>FOR AMBER</u>:

Amber signal means "Get ready to stop crossing" and the delay time (TD3) is calculated as shown:

when R = 9K ohm and C = 470 micro Farad.

T = 0.7RC

T = 0.7 x $9x10^3$ x $470x10^{-6}$

= 3.0 secs.

==> TD3 = <u>3.0 secs</u>

(d) <u>FOR RED</u>:

The second red signal means "Stop crossing" and the delay time is calculated as:

T = 0.7RC

T = 0.7 x $38x10^3$ x $470x10^{-6}$

= 12.5 secs.

==> TD4 = <u>12.5 secs</u>

Total delay time = T_{td} = TD1 + TD2 + TD3 + TD4

= 4.9 + 9.9 + 3.0 + 12.5

= <u>30.3 secs</u>

Choosing a particular 470 micro Farad for the total delay time (T_{td}), the average resistor value is:

$= T_{td} = 0.7RC$

$30.3 = 0.7R \times 470 \times 10^{-6}$

$R = 92.1K$ ohm

$R = \underline{92K \text{ ohm}}$

The connection mode of the resistor and capacitor on SN74121 monostable multivibrator with SN74121 internal block diagram is shown in Figure 3.81.

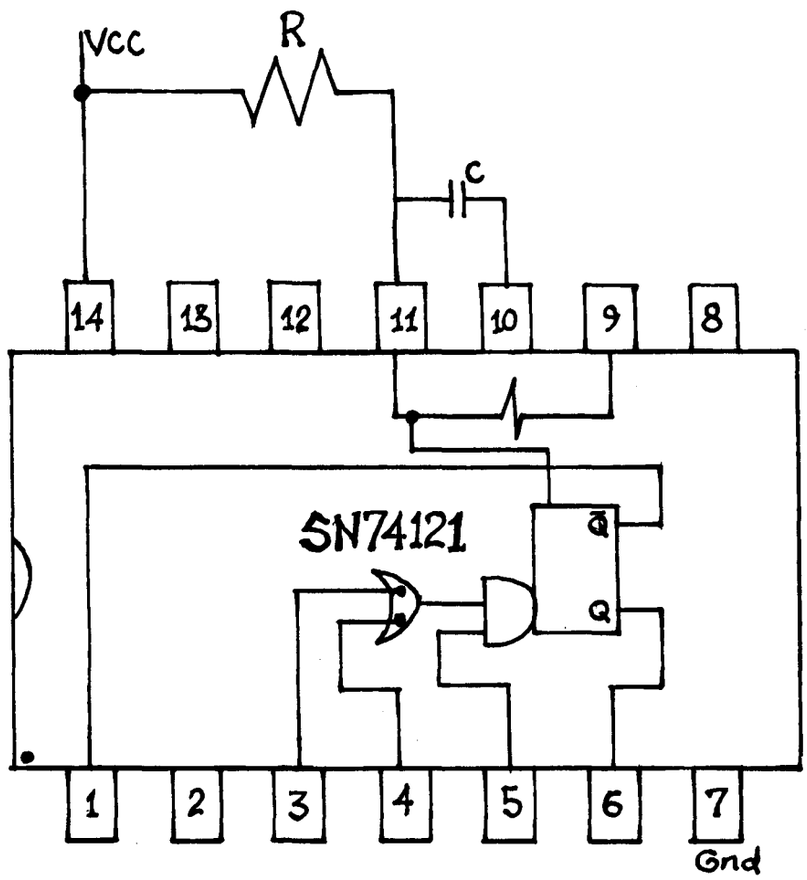


Fig. 3.81: Connection Mode and Internal Block Diagram of SN 74121 Monostable Multivibrator.

Fig. 3.81 Connection mode and interval block diagram of SN74121 monostable Multivibrator.

In this project work, the other Transistor Logic family used are:-

- SN7408 AND gate.
- SN7404 NOT gate.

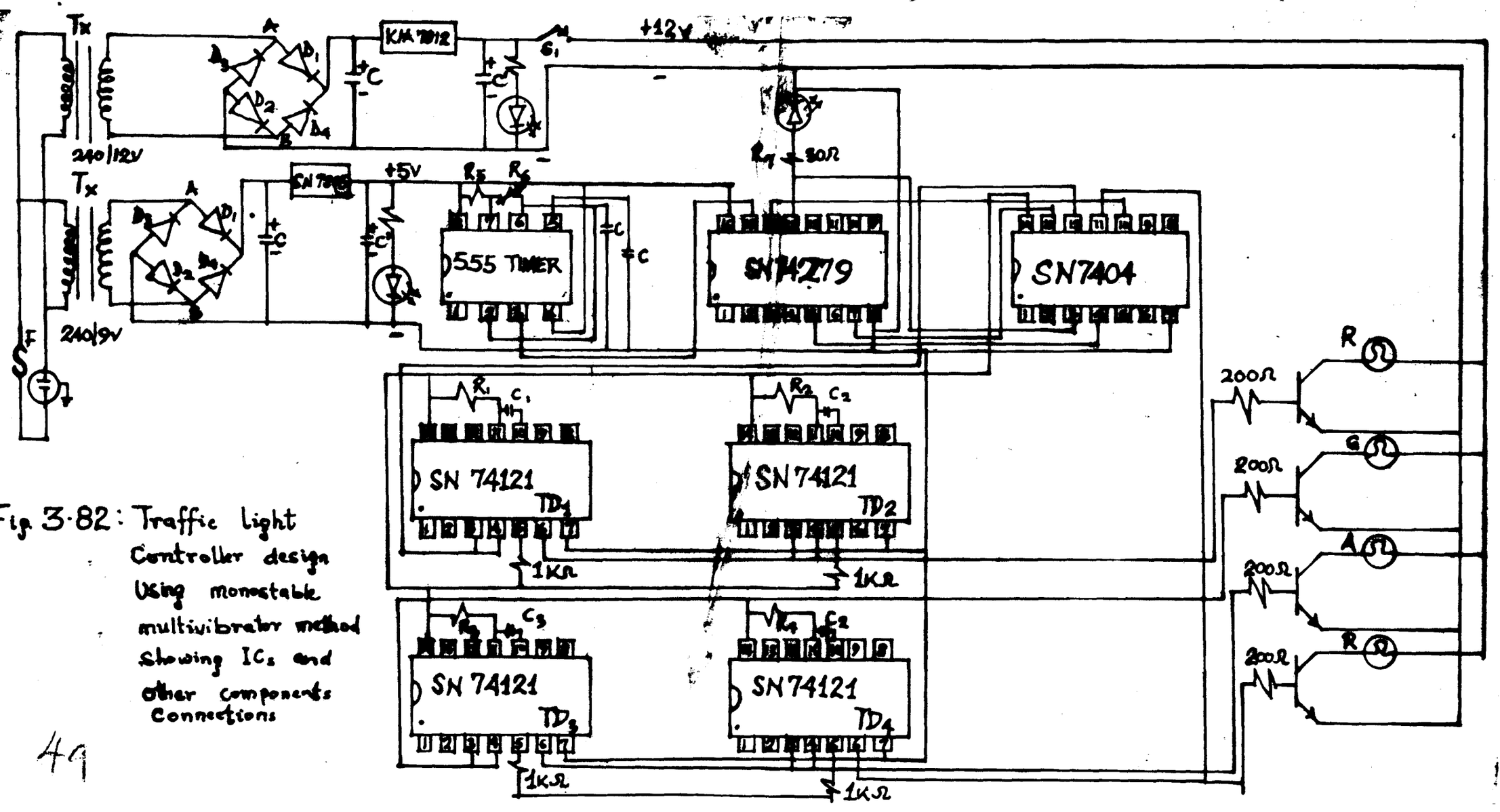


Fig 3·82: Traffic light Controller design Using monostable multivibrator method showing ICs and other components Connections

CHAPTER FOUR

COMPARATIVE EVALUATION OF THE DESIGNS

As we have earlier stated in chapter two, the comparative evaluation of the two designs (i.e using combinational Logic method and Monostable Multivibrator method) shall now be carried out using the following criteria;

i. Production cost.

ii. Reliability

iii. Space

iv. Speed.

4.1 PRODUCTION COST

Production cost or bill of quantity for combinational Logic Circuit method of design and Monostable Multivibrator method design are shown in Tables 4.10 and 4.11 respectively.

COST ESTIMATE TABLES

S/N	ITEM	ITEM LABEL	UNIT COST ₦	QUANTITY	AMOUNT ₦
1.	TIMER (PULSE GENERATOR)	LM555CN	40	1	40
2.	JK FLIP-FLOP	SN74107	120	2	240
3.	2-INPUT AND GATE	SN7408	110	2	220
4.	NOT GATE	SN7404	80	1	80
5.	3-INPUT AND GATE	SN7411	110	1	110
6.	2-INPUT OR GATE	SN7432	110	1	110
7.	DIODES	IN4001	5	8	40
8.	LIGHT EMITTING DIODES	-	10	2	20
9.	TRANSISTOR	BFY52	20	3	60
10	VERO BOARD	-	100	1	100
11	SOLDERING IRON	-	1.5M	-	50
12	CONNECTION WIRE	-	30M	-	150
13	VOLTAGE REGULATOR	SN7805	50	1	50
14	VOLTAGE REGULATOR	KIA7812	50	1	50
.					
.					
.					

S/N	ITEM	RATING	UNIT COST(₦)	QTY	AMOUNT
15	TRANSFORMER	240/9V	150	1	150
.16	TRANSFORMER	240/12V	150	1	150
17	CAPACITORS				
.i	C1	6800UF	10	1	10
1i	C1 AND C4	0.02UF	10	2	20
iii	C3	2200UF	10	1	10
iv	C5	330UF	10	1	10
v	C6	0.01UF	10	1	10
.18	RESISTOR				
i	R1	4K OHM	5	1	5
ii	R2	1K OHM	5	1	5
iii	R3	50 OHM	5	1	5
iv	R4	170 OHM	5	1	5
19	FUSE	100mA	20	1	20
20	TUBLER BULB	12V 5W	30	3	90
i.					
ii					
.					
ii					
i					
iv					
.					
19					
20					
				TOTAL	1810

S/N	ITEM	ITEM LABEL	UNIT COST ₦	QUANTITY	AMOUNT ₦
1.	TIMER (PULSE GENERATOR)	LM555CN	40	1	40
2.	NOT GATE	SN7404	800	1	80
3.	MONOSTABLE MULTIVIBRATOR	SN74121	90	4	360
4.	-	SN74279	80	1	80
5.	DIODES	IN4001	5	8	40
6.	LIGHT EMITTING DIODES	-	10	3	30
7.	CONNECTION WIRE	-	30/M	-	90
8.	VERO BOARD	-	100	1	100
9.	SOLDERING WIRE	-	1.5M	-	20
10	VOLTAGE REGULATOR	SN7805	50	1	50
11	VOLTAGE REGULATOR		50	1	50
12	TRANSISTOR	KIA7812 BFY52	20	3	60
. 12 .					

S/N	ITEM	RATING	UNIT COST	QUANTITY	AMOUNT

S/N	ITEM	RATING	UNIT COST(₦)	QTY	AMOUNT
13	TRANSFORMER	240/9V	150	1	150
.	TRANSFORMER	240/12V	150	1	150
14	CAPACITORS				
15	C1	6800UF	10	1	10
1	C1 AND C4	0.02UF	10	2	20
ii	C3	2200UF	10	1	10
iii	C5	330UF	10	1	10
iv	C6	0.01UF	10	1	10
. v	C11,C12,C13,C14	4.70UF	10	4	40
16	RESISTORS				
i	R1	15K OHM	5	1	5
ii	R2	30K OHM	5	1	5
iii	R3	9K OHM	5	1	5
iv	R4	38K OHM	5	1	5
v	R5	IK OHM	5	1	5
.vi	R6	4K OHM	5	1	5
vii	R7	30K OHM	5	1	5
17	FUSE	100mA	20	1	20
18	TUBLER BULB	12V 5W	30	4	120
.					
ii					
i					
iv					
.					
v.					

4.2 RELIABILITY

The term reliability describes the security of a system. It is difficult to evolve a definition satisfactorily in all circumstances, the following meets most requirements: Reliability is also the characteristic of a component or of a system which may be expressed or defined by the probability that a device or system performing its function adequately, for the period of time intended under stated conditions, frequency of failure and not on the failure probability alone.

Reliability concept has always been associated, in a good qualitative way, with good design, endurance, consistuent quality and dependability. In recent years, however, the much greater complexity of electrical and electronic equipment and seriousness of a failure in the system has made it necessary to attempt not only to improve the reliability of equipment but also to asses it in qualitative terms.

This assessment of reliability is not a simple matter and it will be appreciated that the achievement of high reliability is an aim in which many people must be involved. The component manufacturer, the designers, the production team, the test and quality control Engineers, the installation Engineers and the customers must all contribute to this aim, and it is the objective of this chapter to indicate some of the consideration which are involved.

For some devices and systems, reliability is expressed per unit of time, whereas reliability is stated per unit of use for others.

During the useful life of an electronic product, the failure rate denoted by "X" is approximately constant and is the number of failure per unit time and is a useful measure of a system reliability. The reciprocal of the failure rate is known as the "Mean time" Between Failures (MBTF) which is usually stated in hours. Where failure rate (λ) are constants, one quantitative measure of reliability is this Mean Time Between Failures (MBTF). A filament lamp for example might have an expected life of 3000hrs.

Reliability generally, in the sense just defined varies over time and is stated as a reliability function, R(t) which gives the probability that an item will function without over time (t).

The value of R(t) can be found in principle for life trails on a sample of items sufficiently large to give statistically valid resulted. The sample of items is tested to failure and the proportion of failed items is plotted as a function of time. The result is called the life time distribution function, F(t) which is the probability function.

Since the proportion of failed items can not decrease, the slope of F(t) is never negative. F(t) can also be interpreted as the proportion of items life less than or equal to t. Then 1-F(t) is the proportion of items with exceeding t, which is also the probability that an item will function without failure over time t or R(t).

4.2.1 IMPORTANCE OF RELIABILITY

Reliability is important because human lives and properties depends on correct function of either electrical or electronics system in their surrounding. The failure results in huge financial losses and a times loss of life. This reliability importance serves as a guarantee and invoke competition among manufacturers. Customers requirement also need to be satisfied.

The reliability of the designed system (i.e Combinational Logic Circuit design and Monostable Multivibrator design methods) is calculated using tables 4.20 and 4.21

$$\text{Reliability } [R(t)] = e^{-jnt} \quad \text{-------- (i)}$$

where,

$1/w^6hr = w^6hr^{-1}$ = Constant failure rate.

jn = total failure rate

R(t) = reliability at time t

t = time

hr = hour

C = typical component

n = normal condition

j = number of component

k = number of sampled component

$\hat{\lambda} = \Sigma\ \hat{\lambda}C1jn + c2jnj + ... + \hat{\lambda}Ckjn$

t = 168 hrs

$R(t) = e^{-\hat{\lambda}jnt} = R(168) = e^{-\hat{\lambda}jn(168)}$ -------- (ii)

From the table 4.20, the reliability for combinational Logic Circuits design is calculated as follows:

$\hat{\lambda}jn = [14.40 + 20.00 + 0.20 + 1.60 + 1.00 + 5.10 + 0.345]/10^6hr$

$R(168) = e^{-}\ 42.65 \times 168 \times 10^{-6}hr^{-1}$

$= e^{-}\ 4.265 \times 10^{-5} \times 168$

$= 0.933$

From table 4.21, the reliability for Monostable Multivibrator method of design is calculated as follows:

$R(t) = e^{-\hat{\lambda}jnt} = R(168) = e^{-\hat{\lambda}jn(168)}$

$\hat{\lambda}jn = [24.00 + 22.00 + 0.18 + 5.20 + 1.00 + 6.80 + 0.255]/10^6hr$

$R(168) = e^{-}\ 59.44 \times 10^{-6} \times 168$

$= e^{-}\ 5.994 \times 10^{-5} \times 168$

$= 0.91$

Tables below shows the failure rate of electronic components in normal conditions (t=†20°C):

S/N	COMPONENTS	QUANTITY	$\lambda X10^{-6} hr^{-1}$	TOTAL $\lambda JX10^{-6} hr^{-1}$
1.	CAPACITORS	06	2.40	14.40
2.	DIODES	10	2.00	20.00
3.	INTEGRATED CIRCUITS (IC)	10	0.02	0.2
4.	RESISTORS	04	0.40	1.60
5.	TRANSFORMERS	02	0.50	1.00
6.	TRANSISTORS	03	1.70	5.10
7.	CONNECTION WIRE	23	0.015	0.35
	TOTAL			42.65

Table 4.20: Failure rate of electronics components in normal condition (t=†20°C) for Combinational Logic Circuit design method.

S/N	COMPONENTS	QUANTITY	$\lambda X10^{-6} hr^{-1}$	TOTAL $\lambda JX10^{-6} hr^{-1}$
1.	CAPACITORS	10	2.40	24.00
2.	DIODES	11	2.00	22.00
3.	INTEGRATED CIRCUITS (IC)	9	0.02	0.18
4.	RESISTORS	13	0.40	5.20
5.	TRANSFORMERS	02	0.50	1.00
6.	TRANSISTORS	04	1.70	6.80
7.	CONNECTION WIRE	17	0.015	0.255
	TOTAL			59.44

Table 4.21: Failure rate of electronics components in normal condition (t=†20°C) for Monostable Multivibrator method of design.

4.3 SPACE

The number of Integrated Circuits (IC) and all other components including wire connection were considered from the pin diagram for each method of design which shows that the combinational Logic Circuits (10) and many wires connections (23-lines) while the Monostable Multivibrator method of design has (9) Integrated Circuits and (17-lines) wire connections.

Therefore, since the sizes of Diodes, Resistors, Transistors are small compare to ICs size and space occupied by wire connection, we can now conclude that combinational Logic method of design occupies more space.

4.4 SPEED:

Speed can be calculated using the longest wire connection. i.e. the circuit with longest wire connection delays in speed time compare with the one with short wire connection.

From each methods of design pin connection diagram we can see that Monostable Multivibrator method have lesser number of wire connections due to limit number of components compared to Combinational Logic Circuit method. And for these reasons, Monostable Multivibrator design method is faster (i.e having greater speed) than Combinational Logic Circuit method of design.

Apart from determination of speed from wire connection, and how long the wires are, speed can also be determined from each and individual ICs speed of operation (frequency). And it can be concluded that Monostable Multivibrator method of design is faster in operation than Combinational Logic Circuit method due to high frequency Ics used in its design.

4.5 COMPARISM AND EVALUATIONS OF THE METHODS:

From the comparism evaluations carried out in the project, it can be concluded that Monostable Multivibrator method of design which occupies lesser space, have smaller cost of production, speeds faster and having better reliability value is proposed for the construction for future development of traffic light in our environment.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATION

5.1: CONCLUSION

From the result of the studies carried out in the course of this project, that is using Combinational Logic Circuit method and Monostable Multivibrator method of design for traffic light controller system using production cost, reliability, space occupation and speed as criteria. It can be concluded that the use of any of the method of designs mentioned above depends on financial status, availability of Materials and the environmental factors. But traffic light realization using Monostable Multivibrator method of design is more appropriate based on recommendation below.

5.2 RECOMMENDATION

Recommendation made depends on the research carried out on this project using cost of production, reliability, space occupation and speed as points of comparism and evaluations.

Monostable multivibrator method of design with low cost of production, occupies less space, faster and has more or less equal reliability with the other method (Combinational method) is recommended for our environment for further development work which can be carried out due to advantages seen from observation made from the research and work carried out in this project.

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