DESIGN AND CONSTRUCTION OF A PROGRAMMABLE TIMER

BY

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DEDICATION

I dedicate this work to my parents Hon. And Mrs. S.O. Aboh. Your great love, sacrifice and infinite courage in the midst of seeming insurmountable odds has inspired and energized me all the way. You're the greatest set of parents in God's earth.

ACKNOWLEDGEMENT

Firstly, I thank God almighty, the father of our Lord and saviour Jesus Christ of whose I am and whom I serve; for His loving kindness and exceedingly great mercies that has kept me.

I acknowledge the immense and fatherly contribution of my supervisor, a scientist and technocrat of international repute, Engr. M.D. Abdullahi towards the success of this work. Sir, the bane of Africa is a result of the short supply of men of your calibre.

My parents Hon. & Mrs. S.O. Aboh have been most outstanding in ensuring my complete development and growth. I thank my sisters Patience and Vera for their care, prayers and love- it made a lot of difference. My brother, Ochepa has been most helpful, being my closest confidant, companion and despite his loadol schedule, my auxiliary cook in Minna. Such a wonderful family as you can only be a gift from God.

My profound thanks goes to my uncle, Engr. G.O. Ochepa. He's been my mentor, guardian and after my parents, my biggest financier. My appreciation also goes to his wife, Mrs. Ochepa for her care throughout my stay in Abuja and most especially during my 6 months SIWES programme. May God richly bless and reward you. I also thank my following uncles and aunties for their immense contribution to my education; SP G.U. Ochepa, Arch. & Mrs. S.A. Adai, Mr.Ochai Ochapa(O/C Homicide, State CID, Minna), Ms Grace Adai, Ms Joy Adai, Mr. & Mrs. S.A. Oduma and Mr. Attah Aboh.

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Thank you all and God bless you real good.

Furthermore, I appreciate the contribution and assistance of my project partner, Simeon Adama to the success of this work. I thank my colleague and dear friend Inalegwu Obekpa, the hidden guru and innovator. I'm also indebted to my following colleagues at Minna; Awara Gabriel, John Odang, Godreigns Amedare, Harold Samuel, King Orumah, Daniel Onjeh, Agebe John, Alphonsus Abah, Samuel Ifere, Pst. James Okpanachi, Pst Mike Benjamin, Pst Joshua Ochoge, Pst Paul Yakubu, Joy Enyi, Henrietta, Chinedu Ahanobi, Marcel Nto, Haruna Kolo, Nada, Elijah Danjuma and so many others too numerous to mention.
Finally, I express my profound appreciation to the head of department and the entire staff members of the department of Electrical & Computer Engineering, Federal University of Technology Minna. May God reward you accordingly.

CERTIFICATION

This is to certify that this project titled design and construction of a programmable timer, was carried out by Aboh Godwin Aboh under the supervision of Engr. M. D. Abdullahi (FNSE) and submitted to the department of Electrical and Computer Engineering, Federal University Of Technology Minna in partial fulfillment of the requirement for the award of a Bachelors of Engineering (B.ENG.) Degree in Electrical and Computer Engineering.

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ABSTRACT

The programmable timer is a simple, user friendly device that can be programmed with respect to time, to turn on or off a supply. When interfaced with a device say, a heater, the user can afford to set the count-down time to say, 15 minutes and can hence enjoy the luxury and security of attending to some other needs knowing fully well that the circuit will cut off mains supply after 15 minutes.

The timer circuit is based on the application of counting pulses generated by means of quartz crystal which vibrates at a frequency of 32768Hz, divided by a 14 stage ripple carry binary counter/ divider/oscillator (4060B) to give a clock pulse at 2 pulse per second, then divided by a flip-flop.

A relay, which is a sort of "electrical brain", performs the function of automatically triggering the timer on or off when a preset number of pulses has occurred.

It incorporates basically; decoders, counters, an oscillator, the control unit, relay and a seven segment LED display.

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CHAPTER ONE

INTRODUCTION

1.1 GENERAL INTRODUCTION

The timer is intended to provide controls for processing or manufacturing needs, or in domestic appliances based on an exact timing base where the measurement of time and time- interred control are critical to successful operation without intermittent human input.

The timer circuit is divided into six major units. These are: the power supply unit (PSU), the clock generator, the counters, the seven-segment display unit, the control unit, and the relay trigger unit.

The power supply unit receives an input 6V direct current supply from dry cells which drives the crystal. The cells convert the chemical energy of its internal constituent to electrical energy needed by the circuit.

The clock generator generates clock pulses. The crystal –controlled clock generator used in the design employed highly stable and accurate components called quartz crystal. It oscillates at an accurate frequency. This particular clock generator was chosen because of the stability of its output frequency component with the Schmitt-trigger oscillator, the 555 timer, and RC- crystal oscillator.

The seven-segment display unit outputs decimal characters. The seven-segment display consists of seven lines which are connected in common-cathode. The display of binary numbers as decimal characters is enabled by BCD to decimal decoder / drivers. It takes a four-bit BCD input and provides an outputs that drives an appropriate segment of the display.

The counters are designed to work on the principle of connecting a separate set of decoder / driver and display to each counter rather than the multiplexing technique. The counters used in this project are down counters (asynchronous counters). They count from a user input value down to zero. Down counters are most suitable for this particular project since it is designed to know the number of input pulses that occurs.

The control unit consists of logic gates in form of ICs, flip-flops and switches. The major function of this unit is to preset the counters to a desired starting count asynchronously (independent of the clock signal).

The relay trigger unit, takes care of the execution and control operation. The task is executed when the 8-input OR-gate sensor indicates that the preset number of pulses has occurred and thus enables the relay to trigger off. The pull switch control of the relay opens or closes when a control current passes through the coil and an electromagnet field is formed. Incorporated also in this unit is the transistor driver circuit for relay coil, used to control direct current from logic levels.

1.2 LITERATURE REVIEW

Over the years, numerous models of timer devices have been used by man to achieve a reliable and accurate time reference base for scheduling one or more domestic and industrial events with reference to time. However, with man's quest to make life more comfortable and safe, effort is being made to move from old methods to inventing the best techniques.

The earlier means used include spring- wound timers (in an alarm clock), fluid dash-pots, pneumatic devices, inert devices, etc.

However, the technology advancement in this era has brought us to situations in industries where time – interval control are critical to the successful operation of certain processing or manufacturing operation which may not permit human intervention or supervision hence, programmable timers will play a very vital role in controlling such events.

The basic principle of operation of the timer is based on the application of counting pulses generator rated by means of quartz crystal which vibrates (resonates) at a frequency of 32768 Hz which is divided by a 14-stage ripple carry binary counter/ divider/ oscillator (4060BIC) to give a clock pulse at 2 pulse per second and is again divided by a flip-flop. The relay triggers automatically when the preset number of pulses has occurred to switch off the desired system.

The design of this project is an innovative trend, which uses down counters which will count down from a maximum count to zero instead of the widely used up counters.

CHAPTER TWO

DESIGN AND ANALYSIS OF COMPONENTS

2.1 PRINCIPLES OF OPERATION

The timer uses one of the common applications of counters which counts pulses coming out of a pulse generator at a frequency of 1Hz (i.e. one pulse per second 1PPS). This clock signals are generated by a highly stable and accurate component called a quartz crystal, *which* vibrates (resonate) when excited at a precise frequency. This operating frequency (32768Hz) is then divided by a frequency oscillator/divider (4060BIC) and a flip-flop to give 1PPS.

The clock pulse generated at a frequency of 1Hz (i.e. one pulse per second) is fed into a MOD-10 counter (decoder counter) of the SECOND section (see fig. 2.0 below) which counts and displays seconds from 59 through 0. The MOD-10 counter output recycles every 60 seconds.

The same signal is fed to the MINUTE section, which counts and displays minutes from the maximum preset minute through zero.

The relay unit triggers automatically at the end of the count of 0 of the maximum preset count to switch off the system.

The block diagram of the principle of operation of the timer is shown in figure 2.0 below.

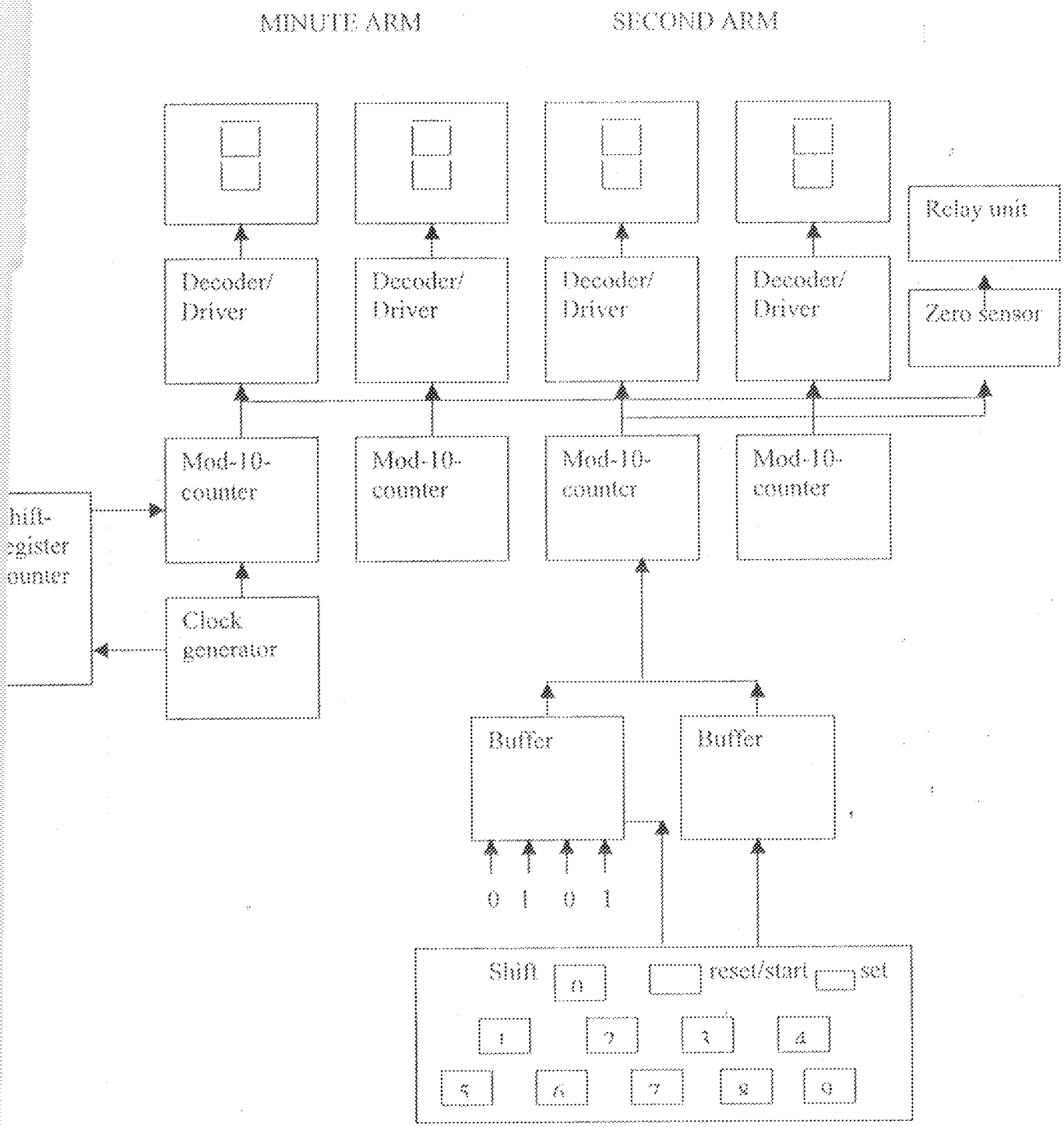


FIG. 2.0: BLOCK DIAGRAM OF THE TIMER

2.2.0 LOGIC FAMILY SELECTION

There are so many different logic families produced by different manufacturers.

At present, there are three main logic families in common use. There includes:

1. Transistor-Transistor Logic (TTL)
2. Complimentary Metal-Oxide Semiconductor (CMOS)
3. Emitter-Coupled Logic (ECL)

Others include:

4. Resistor-Transistor Logic (RTL)
5. Diode-Transistor Logic (DTL)
6. Integrated Injection Logic (IIL)

Complimentary metal-oxide semiconductor (CMOS) or Transistor-Transistor Logic (TTL) should be able to satisfy most user's needs except where the ultimate in speed is needed when emitter-coupled logic (ECL) should be chosen.

The CMOS family is widely used. It has very low power consumption and are perfect battery operated electronic devices which satisfies the requirement for this project. Many large scale integrated circuits (LSI) such as digital wrist watches and calculator chips are manufactured using the CMOS technology. The older 7400 series of TTL logic devices has been extremely popular for many decades. Its major disadvantage however is its high power consumption.

In the late 1960s, manufacturers developed CMOS digital ICs and since then, many types of CMOS circuits are available and several families of compatible CMOS ICs have been developed also. The first was 4000 series, then came 74C00 series and so on. For this project work, the 4000 series are used.

The following reasons explain why the CMOS family are used for this project.

a. They do not respond to very fast noise pulses or circuits glitches because of its slower speed.

b. They have a large (good) noise immunity (rejection) than other logic families.

c. It is possible to pack more gates into the IC without running into heat dissipation problems because of lower power consumption.

d. They are readily available in the market

e. They impose fewer restraints on the power supply (+3v to +18v at very low currents).

2.3.0 THE POWER SUPPLY UNIT (PSU)

The power supply unit forms an important aspect of the project construction. It is a very important primary factor that determines whether the project works or not.

Generally, CMOS are usually driven by a battery supply and they use voltages ranging from (+3V to +18V). For this project 9V supplied from the battery is used to drive the circuit. Therefore, the difficulty of designing the power supply unit is extremely limited and also the use of power supply regulator IC is not required because of the voltage range.

The batteries convert the chemical energy of the constituents to electrical energy. The figure below shows the circuit symbol for a battery.

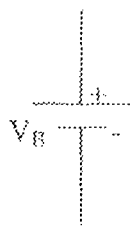


FIG: 2.1 CIRCUIT SYMBOL OF A BATTERY

The process of power delivery to the circuit can only last for a finite time. As the current is drawn from the battery, the chemical components in the battery are consumed, the battery decreases towards zero, and we say that the battery is discharged at this point. However, the rate of discharge depends on how much current is drawn from the battery by the circuit. At higher currents, the battery lifetime is shorter. The figure below shows the battery discharge curve for different current values.

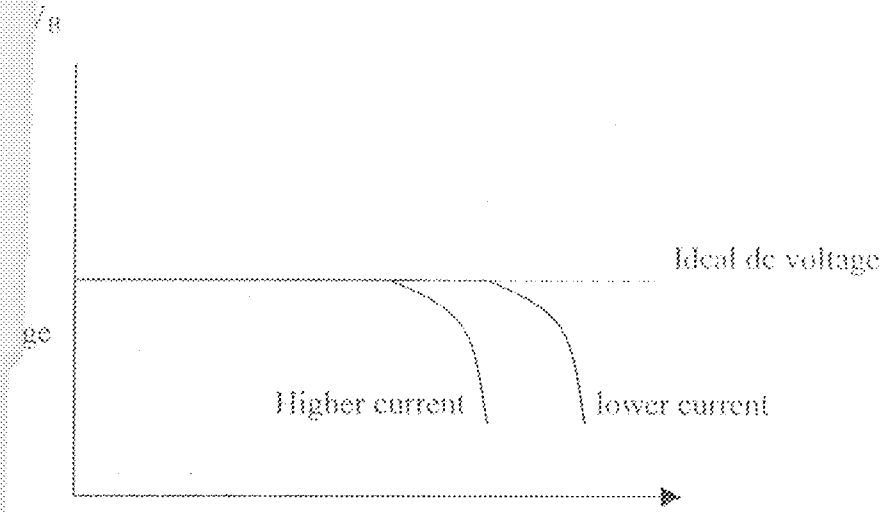


FIG. 2.2 . BATTERY DISCHARGE CURVE FOR TWO DIFFERENT CURRENTS

2.4.0 THE CLOCK (PULSE) GENERATOR

2.4.1 THE QUARTZ CYRSTAL

The clock pulse generator used in this project is the Quartz Crystal. The quartz crystal has a mechanical resonant frequency at which it oscillates when excited.

A piece of quartz crystal can be cut to a specific size and shape to vibrate (resonate) at a precise at a precise frequency that is extremely stable with temperature and age. Frequencies from 10KHz to 80MHz are readily achievable. The operating frequency for the crystal used in this project is 32768HZ (32.768KHZ), that is 2^{15} counts per second.

Timers need to have accurate, stable clock pulses available. A quartz crystal, together with a simple circuit to generate digital pulses, fits the need of this project perfectly compared to the use of 555 timer and Schmitt trigger as clock pulse generators.

2.4.2 CLOCK FREQUENCY DIVIDER/COUNTER

The oscillator frequency generated by the quartz crystal cannot be fed into the counters directly thus, frequency divider/counter/oscillator (4060BIC) is used. It contains 14 flip-flops, each dividing the frequency of its input by 2 giving a clock pulse at 2 pulse per second which is again divided by a J-K flip-flop to give one pulse per second.

The output of each flip-flop is a square wave fed into the counters.

2.5.0 SEVEN SEGMENT DISPLAY AND DECODER/DRIVER

2.5.1 SEVEN SEGMENT DISPLAY UNIT

The display type used in this design is the Light Emitting Diode (LED) seven segment display. It is a simple display that can display the digits the digits 0-9 and the hex extension (A-F), albeit somewhat crudely (the hex letters are displayed as "AbcdEF").

The LED used in the design is a common-cathode type where the cathodes of all the segments are tied together and connected to ground.

The display readout is driven by a BCD to seven segment decoder/driver with active HIGH outputs that apply a HIGH voltage to the anodes of those segments to be activated. The seven segment display is available in form of an IC.

The anodes are connected to the output of the CD4511B decoder. All the anodes of the LEDs are connected through the current- limiting resistors, to the appropriate outputs of the decoder/driver. By controlling current through each LED, some segments will light (1) and others will be dark (o) so that the desired character pattern will be generated.

The figure below shows a seven segment LED indicator arrangement.

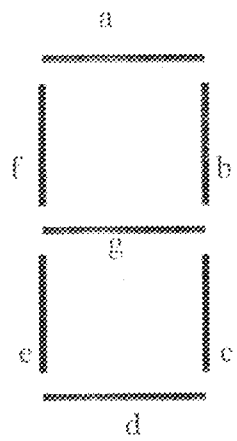


FIG 2.4 : A 7-SEGMENT LED INDICATOR ARRANGEMENT

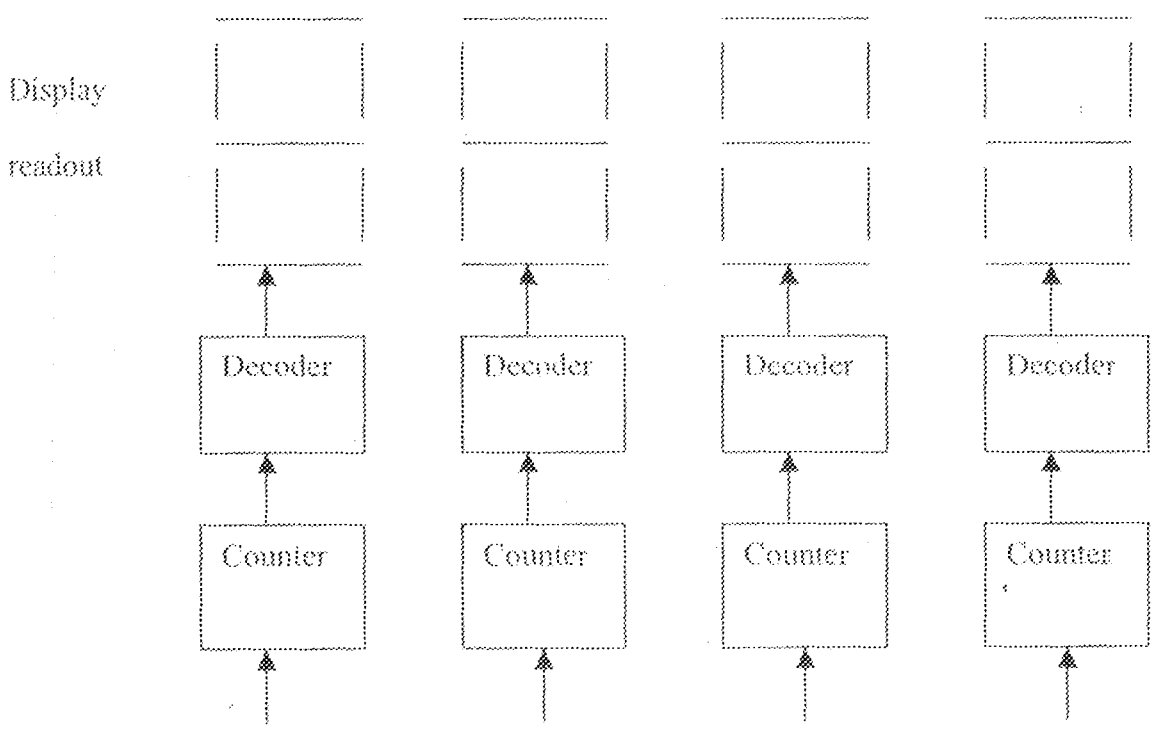
The clock pulse counted by the down counter is clearly readout from this segment unit.

The LEDs are chosen for this project because of their bright display compared to the Liquid- Crystal displays (LCD).

2.5.2 BCD- TO – 7- SEGMENT DECODER / DRIVER

A decoder is a circuit used to change a coded input such as the BCD to another code. The CD4511B used in this design takes a four-bit BCD input from the output of CD4029B counters and provide the outputs that passes current through the appropriate segments to display the decimal digit.

The decoder/driver inputs that come from the output of the counter is pulsed continually and the output of the decoder/driver is activated sequentially to turn devices on/off at a specified time via the relay.


Display
readout
Decoder
Decoder
Decoder
Decoder
Counter
Counter
Counter
Counter

2.6.0 THE CONTROL UNIT

The control unit is the pivot of the timer. It determines how the timer functions. It's major function is to preset the counters to the desired starting count or resetting of the counter as the case may be.

2.6.1 THE SWITCHES

All the switches used in this design work are on a panel (pad) from which the operation of the timer is carried out using appropriate buttons to perform a desired operation. The panel is a matrix of switches arranged in columns and rows. Depressing a button (switch), short –circuits a row and a column. The panel is connected to each counter. Each switch has its unique function.

2.6.2 THE S-R LATCH

The CD4027B integrated circuit has provisions for J.K, Set, Reset, and clock input signals. Therefore the clock and J.K. inputs are grounded which permits the use of J-K master flip-flop as SET(S) – RESET(R) LATCH. Set and Reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input and the output signals are produced as buffered signals Q and $\bar{Q}$. Hence this requires high technical knowledge to achieve.

2.7 THE RELAY UNIT

This unit consists of the relay and a transistor.

The relay is an electrically controlled switch. it consists of an electromagnet and a set of switch contacts: normally opened and normally closed.

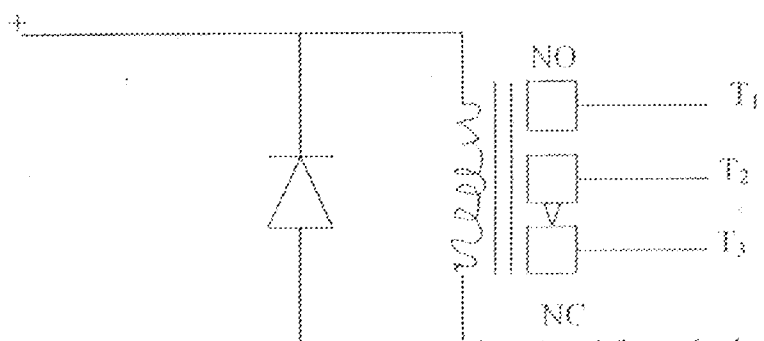
A normally opened contact is one in which the relay is de-energized when it is opened while the normally closed contact is one which is closed when the relay is de-energized Thus the contacts change state when the relay is energized.

A voltage spike, dangerous to the transistor is produced when the relay is de-energized. Thus a diode is connected across the inductor in reverse mode to protect the transistors.

The transistors form a complimentary switch, thus when the transistors are turned "ON", the relay is de-energized and vice-versa.

The circuit diagram of the relay is given below.

FIG 2.6 6V RELAY



When the transistors are saturated upon receiving signal from the logic levels, it switches off the relay which in turn isolates the equipment from mains supply.

2.8 THE BUFFER

A buffer has high input impedance and low output impedance. It is used in circuits to protect sensitive, low voltage components.
Hex non- inverting 3-state buffer used in this project, acts as an intermediary component between the counter and panel and prevents undesirable signals from going into the counter.

CHAPTER THREE

CONSTRUCTION OF COUNTERAND DISCUSSION OF RESULT

3.1 CLASSIFICATION OF COUNTERS

Counters are classified into two broad categories according to the way they are clocked: asynchronous and synchronous. In asynchronous counters, commonly called RIPPLE COUNTERS, the first flip- flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop. In the case of synchronous counters, which were used in this project, the clock input is connected to all the flip-flops so that they are clocked simultaneously.

3.2 SYNCHRONOUS COUNTERS

A synchronous counter is one in which all the outputs are changed at the same time by the input clock.

When the J and K inputs are low on a J K flip-flop, the output does not change when the flip-flop is clocked; and if J and K are high, the flip-flop toggles when it is clocked.

In other words, each flip-flop should have its J and K inputs connected such that they are HIGH only when the outputs of all lower order flip-flops are in he HIGH state. The synchronous counters are otherwise known as PARALLEL COUNTERS.

3.3.0 SYNCHRONOUS DECADE COUNTERS (MOD-10-COUNTERS)

The counters used in this work are synchronous MOD-10- counters. Counters could also be designed to have a number of states in their sequence that is less than the maximum of 2^n. The resulting sequence is called a TRUNCATED SEQUENCE. To obtain a truncated sequence, it is necessary to force the counter to recycle before going through all its normal states. For example, the BCD decoder counter must recycle back to the 0000 state after count of nine (1001),is to decode count ten (1010) with NAND gate and connect the output of the NAND gate to the clear (CLR) inputs of the flip-flops.

CIRCUIT DIAGRAM OF A MOD-10-COUNTER

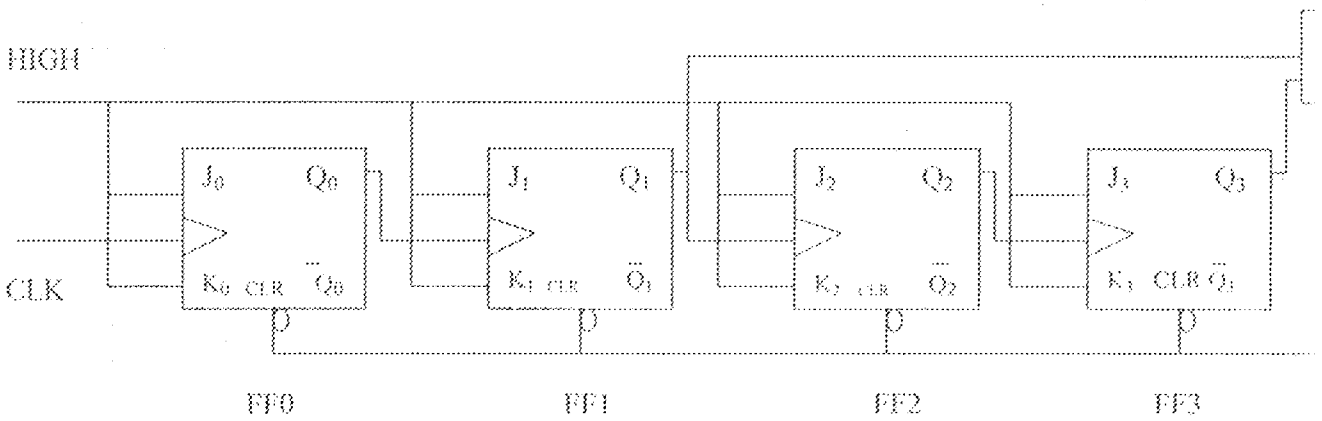


FIG 3.1 MOD-10- COUNTER

A decade counter requires four flip-flops (three flip-flops are insufficient because $2^3 = 8$ i.e. 2^n). This type of counter is useful in display applications as used in this project work in which BCD is required to be converted to a decimal readout.

3.3.1 SYNCHRONOUS MOD-10-BINARY DOWN COUNTERS.

The synchronous (parallel) DOWN counters used in this work counts down from a input starting count to zero. Just as in UP counters, each flip-flop toggles when clocked if J and K are HIGH.

The CDA029B counter used consists of a four-stage binary or BCD – decade Up/Down counter. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock.

Binary counting is accomplished when the BINARY/DECADE input is high. The parallel down counters are made to count down by using the inverted output of each flip-flop to drive the following J, K inputs.

This DOWN COUNTERS are normally used in situations where the desired number of input pulses that have occurred must be known as is the desire in this project.

THE DIAGRAM OF A J K MOD-10-DOWN COUNTER

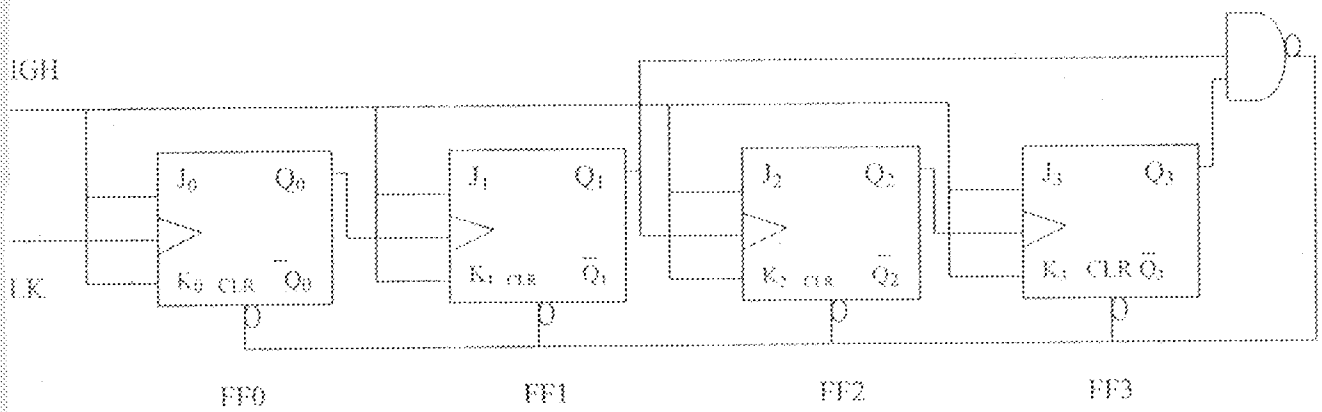


FIG 3.2 MOD-10-DOWN COUNTER

THE TRANSITION TABLE FOR A J K FLIP FLOP

TRANSITION AT OUTPUT	OUTPUT TRANSITION		FLIP-FLOP	
	Q_N	Q_{N+1}	J	K
0 ⟶ 0	0	0	0	X
0 ⟶ 1	0	1	1	X
1 ⟶ 0	1	0	X	1
1 ⟶ 1	1	1	X	0

Figure: 3.4.

KEY:

Q_N: Preset state of the flip-flop before clock pulse.

Q_{N+1}: Next state of the flip-flop after clock pulse.

X: "Don't care " condition.

3.4 FLIP-FLOPS

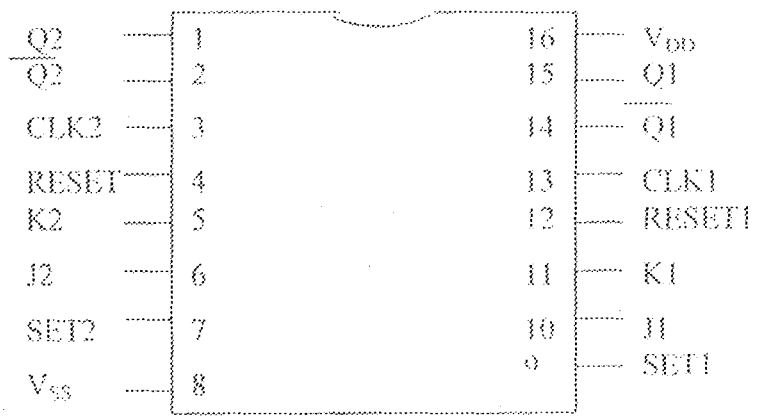
Flip-flops (FF) are synchronous bi-stable devices. The term synchronism means that the output changes state only at specified point on a triggering input called clock (CLK), i.e. changes in the output occur in synchronism with the clock.

An edge-triggered flip-flop changes state either at the positive stage (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its input only at this transition.

The CD 4027B IC used is a dual J – K master flip-flop, the flip-flop is used to perform toggle function. The logic functions present at the J and K inputs changes state in synchronism with the positive going tradition of the clock pulse. On each successive clock spike, the flip-flop changes to the opposite state, this mode is called TOGGLE operation.

THE CD4027B DUAL J – K MASTER FLIP-FLOP

FIG. 3.4 THE CD4027B DUAL J-K MASTER FLIP-FLOP



POSITIVE EDGE-TRIGGERED 4027 TRUTH TABLE

INPUTS	OUTPUTS	COMMENTS
S R CK J K	Q $\bar{Q}$	
L L ↑ L L	Q $\bar{Q}_0$	No change
L L ↑ H L	H L	RESET
L L ↑ L H	L H	SET
L L ↑ H H	$\bar{Q}_0$ Q_0	TOGGLE
L H X X X	0 1	
H L X X X	1 0	
H H X X X	H* H*	

Figure 3.6

KEY:

↑ :Clock transition LOW to HIGH

X : Irrelevant ("don't care")

Q_0 : Output level prior to transition.

3.5 SHIFT - REGISTER COUNTER

A shift-register is used to shift the data or value of flip-flops from left to right. Shift register counter shifts the output of the last flip-flop in the connection back to the first flip-flop.

JOHNSON COUNTER

A 4-stage divide-by-8 Johnson counter was used as MOD-8 counter, this means it has eight distinct states before the sequence repeats. Although this circuit does not progress through the normal binary counting sequence, it is still a counter because each count corresponds to a unique set of flip-flop states.

The design of Johnson or twisted-ring counter is such that the inverted output of the last flip-flop is connected to the input of the first flip-flop. On each positive clock-pulse transistor, the $\bar{Q}_0$ output is connected back to the D input of Q_3. This means that the inverse of the level stored in Q_0 will be transferred to Q_3 on the clock pulse, Q_3 into Q_2, Q_2 into Q_1 and Q_1 into Q_0 randomly.

JOHNSON SEQUENCE TABLE

Q_3	Q_3	Q_1	Q_2	CLOCK PULSE
0	0	0	0	0
1	0	0	0	1
1	1	0	0	2
1	1	1	0	3
1	1	1	1	4
0	1	1	1	5
0	1	1	1	6
0	0	1	1	7
0	0	0	0	8
1	0	0	0	9
1	1	0	0	10

Figure 3.8

3.6 DISCUSSION OF RESULTS

It was expected that the clock generator when excited should generate clock pulses using quartz crystal whose operating frequency is 32.768KH and this was achieved.

The down counter which was obtained as an IC to minimize cost of building from discrete components, also functioned normally as expected, producing counts from 9999 to 0000 via the decoder/ drivers and was displayed on the seven segment display unit.

The relay was expected to switch off the equipment at the end of set input countdown to 0000 of the timer and this was successful.

The result of this project therefore was very satisfactory at testing. In other words the design, research and construction is a success.

3.7 THE CONSTRUCTION COMPONENTS

With little limitations the construction of the timer was successful. Most of the components used were in the form of integrated circuits (IC).

A detailed list of the components used are listed below. All the ICs used are of the Complementary Metal-Oxide semiconductor (CMOS) family.

S/N	COMPONENT TYPE	QUANTITY
1	CD 4511 B decoders	4
2	CD 402gB counters	4
3	CD 4073 B tri-3-input AND gate	1
4	CD 4060 B Divider / oscillator	1
5	CD 4081 B Quad-2-input AND gate	1
6	CD 4011 B Quad –2-input NAND gate	1
7	CD 4022 B stepper	2
8	CD.4503 B Buffer	2
9	CD 4027 B Dual-J-K Master F-F	2
10	CD 4078 B 8-input NOR gate	2
11	CD 4069 B Hex inverter (NOT gate)	2
12	CV Relay	1
13	Transistors. 2SC403 2SC445	1
14	Resistors .1KU, 33K,2 2k, 1M	1
15	Diode IN4001	20
16	Bush buttons	12
17	Quartz crystal	1
18	Capacitors. Ceramic. 75pf. 30pf	1

19	Soldering lead	Few yards
20	Seven segment LED indicator	4
21	Vero board	
22	Connection wires	numerous
23	404071 Quad 2+ input or gate	2.

CHAPTER FOUR

CONCLUSION AND RECOMMENDATIONS

4.1 CONCLUSION

The design and construction of the programmable timer was quite eventful. Some of the components used were not readily available but in the end, the work was completed. From the test of the prototype, the project works to desired specification and projection. I sincerely believe and hope that the circuit would be appreciated and utilized by target domestic and industrial concerns where it is applicable

4.2 RECOMMENDATIONS

Though the aim of this project work has been successfully achieved, they were however some technical difficulties. Problems were encountered in the area of producing rectified 9V supply required to power the circuit design from AC mains supply, which eventually made me settle for the conventional but more expensive use of DC supply . For purpose of future work, attempts should be made towards the use of AC rectified supply to power CMOS logic .

It is my view that the practical curriculum of the department be reviewed to the end that more current and relevant areas of practical electronics be emphasized.

4.3 REFERENCES

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   Paul Horowitz

3.ELECTRONICS II

   D.C. Green

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