DESIGN, CONSTRUCTION AND TESTING

OF

A 500VA DIGITAL UPS/INVERTER

THIS THESIS IS PRESENTED

BY

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SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY.

NOVEMBER 2007.

DECLARATION

I OKEBUGWU CHIMAROKE , do declare that this project is the result of my original work and that no part of it has in any way being reproduced for publication nor has this thesis been submitted to this or any other institution for the award of a degree or diploma.

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Date

CERTIFICATION

This is to certify that this thesis (design, construction and testing of a 500VA digital ups/inverter), constructed by OKEBUGWU CHIMAROKE meets the standard expected for the award of bachelor of Engineering degree (B.ENG) by the Electrical and Computer Engineering Department, Federal University of Technology, Minna.

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Engr. Eronu

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Date

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Engr. M.D. Abdullahir
Head of Department

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Date

DEDICATION

This thesis is dedicated to the almighty God who through his infinite mercy has kept me up to this day and has been my fortress and refuge in times of perils .

Also, to my indispensable parents for their care , love and support they gave to me.

To all those who directly and indirectly contributed to this achievement, especially to my brothers and sister, I say a big thank you because you all have been a blessing to me.

ACKNOWLEDGEMENT

All thanks to the Almighty God for making my dreams and aspiration come to fruition. His mercy, care, love and grace on me cannot be over emphasized. Once again, you are worthy to be praised.

My heart goes out to my parents ,Mr and Mrs M.C. Okebugwu for their relentless support, encouragement ,prayers and provision throughout my academic pursuit. I see it as an opportunity accorded to me and not my right , I say thank you.

Also, I appreciate the effort of all those who directly or indirectly contributed immensely to my achievement in life. Especially, Engr. Okebuwgu Ugochukwu, Acct. Maduboku Ngozi, Okebugwu Chibuihe,Dr. Okebugwu Alozie and Engr. Okebugwu Olisaemeka;you are all a gift from God to me.

My sincere and heartfelt thanks goes out to my friends who stood there for me in times of trials and tribulation

Also, I want to appreciate the effort of my supervisor, Engr. Eronu for the support he accorded to me during the course of this project.

Lastly, I would like to appreciate with joy and happiness the immense contribution of Dr.Okebugwu Alozie who took it as a responsibility bestowed upon him to see to it that my graduation becomes a reality.May the Almighty God bless you.

TABLE OF CONTENT

ABSTRACT

Due to the inadequate supply of electricity for domestic use from the primary source (power holding company of Nigeria), it has become imperative and an onus task to produce or source for a secondary source of power generation that is completely independent of the primary source. the inadequacies of the primary source could be attributed to various factors that could be controlled or checked , but this boils down to the fact that supply of electricity for domestic , industrial and commercial consumption for the consumers is not determinable.

The purpose of this work is to develop an alternative source of power generation .this alternative or secondary source is known as a digital ups/inverter. This device must be capable to produce continuous and uninterruptible a.c voltage, so that consumers do not detect a complete failure or change in power source.

The ups/inverter was designed using mosfet as the main switching component and the switching pulse were generated by a pulse width modulated I.C.

The device can power loads up to 500watts from an ordinary 12volts car battery.

CHAPTER ONE

1.1 INTRODUCTION

Incessant power failure has become a disturbing and common phenomenon today. Its occurrence has led to the damage and loss of so many domestic and industrial appliances and consequently also to the loss of both human lives and properties in places where constant power supply is inevitable. Such places include hospitals, factories, libraries, theatre rooms, laboratories, hotels, banks, and similar institutions just to mention a few.

As a result of this scourge, there is a vital need for an alternative source of power supply that will be more reliable and efficient for the provision of adequate electrical energy in the form of an alternating current, especially in times of failures from the public supply like NEPA.

This has actually led to the research and discovery of the **INVERTER** designed to handle electric power backing up problems, which ensures constant power supply to its consumers in case of power failure from public utility.

Different countries or nations operate on various voltages and frequencies as their main (utility). The major voltages used are: -

(1) 220 — 240, 50Hz. e.g. Nigeria, Ghana, Britain, Germany etc.

(2) 110— 120V, 60Hz e.g. U.S.A, Japan Korea etc.

This device will serve as a secondary power supply in remote areas where the utility of the utility is not available.

Secondly, as a backup in places where the utility is present. It can also serve as a standby power supply when enough d.c is available (i.e. enough charged car batteries).

It has been designed to handle a number of appliances that may urgently require power, such as CPU, VDU, TV sets, lightings, audio sets such as PAS (Public Address System), life

support equipments in the hospital etc.

To this end 500VA output is the maximum it will be designed for, in order to handle just a few of the electronic devices simultaneously.

1.2 WHAT IS POWER INVERTER

An inverter in electronic term is a devise that is capable of changing electrical energy from d.c to a.c and so a d.c power inverter is an electronic arrangement used to convert a lower d.c voltage to a higher a.c voltage output at a particular frequency. Therefore, in this project work, a 12volts car battery (d.c power source) is been inverted to a 220 V/Hz a.c power output.

The proposed electronic power inverter scheme has a variety number of applications in standby power supplies, which are used in industries and commerce to prevent interruptions in process of productions. Also, to protect human life and for many other purposes when the primary source **(mains)** experiences a power failure.

Some practical and field applications of this project i.e. Electronic Lower inverter, can be found in;

(1) The energence fluorescent light used in homes, hospitals and generator control rooms.

(2) The Uninterruptible Power Supply unit used with computer systems to keep the system in operation at all times.

(3) It can also be used at the research centres and local areas where the a.c supply generated by the supply authority could not be reached

(4) Television sets, video cassettes recorder and other appliances that run on a.c

(5) It can also be used in areas where constant a.c supply is not accessible.

1.3 AIMS AND OBJECTIVES

The design of electronic power inverter is aimed at developing another means of

generating power supply from d.c — a.c inversion using a readily available source of direct current from the battery. Also, the charger was incorporated so as to serve as a means of charging the battery when the current is available.

The design of the 500watts electronic power inverter is simple and electronic components employed for the circuitry are readily available in the market.

The design takes into consideration the following: -

(1) Overall cost.

(2) Availability of components used.

(3) Output power rating.

(4) Size and rate of the device

The electronic power inverter was designed to provide the following: -

(i) To provide noise free, vibration and fumes of a generator. This is because it allows out to obtain silent a.c power without the need of a generator.

(ii) To serve as a standby supply of electricity when there is mains failure.

(iii) To provide a cheap alternative to a standby generating set.

(iv) To provide adequate power for household appliances like TV, VCR, stereo and no of the small appliances independent of public supply in all areas where there is no constant supply from the primary source.

CHAPTER TWO

2.0 LITERATURE REVIEW

Development of an Electronic Power Inverter is a new technology of obtaining an a.c from d.c source before this development, standby generating sets was the only source of alternative to the NEPA mains. The mains in Nigeria is quite unreliable and generating sets are also expensive to procure. The development of an electronic power inverter has therefore made it possible for us to obtain a.c from the batteries at a much more cheaper rate.

The worlds first high performance power inverter was introduced in 1983 by **HEART INTERFACE**, has been a leader in inverter/charger technology. It was the first reasonably priced commercial market inverter/charger.

In 1984 Heart Interface patented and introduced inverters utilizing field effect transistors (i.e. mosfets - metal oxide semiconductor field effect transistors), for the main power output device. The use of mosfets made the design smaller than Bipolar Junction Transistor.

2.1 PROJECT OUTLINE

This project report write-up centres on the design, construction and testing of a 500watts electronic power inverter, and it explains step by step analysis of the stages involved.

Chapter One directly dwells on the introductory aspect.

Chapter Two outlines the literature of review.

Chapter Three outlines the process of designing the electronic power inverter.

Chapter Four outlines the process of assembling the various components of the electronic power inverter and testing.

Chapter Five gives the concluding remarks, recommendation and references.

2.2 DESIGN SPECIFICATIONS

OUTPUT POWER: 500 VA

OUTPUT WAVEFORM: PULSE WIDTH MODULATED.

OUTPUT FREQUENCY: 50Hz ± 10%

OUTPUT VOLTAGE: 240V ± 10%

CHARGER TYPE: CONSTANT VOLTAGE.

CHAPTER THREE

DESIGN AND ANALYSIS

3.0 PRINCIPLE OF OPERATION

The principle is base on the performance of push pull amplifier. The push pull amplifier is driven from a 50Hz oscillator via a driver stage. The oscillator stage generates waveform of about 50Hz and 1800 out of phase to allow alternate switching of the push pull inverter stage. The push pull stage (where conversion is done) is a class B amplifier. The amplifier needs secondary element to operate. Thyristor, bipolar transistors and mosfets are often used. The switching is done on the secondary of the transformer, which consequently include a high voltage on the primary.

The current demand from the battery, require that charging has to be regular if the battery must not run down permanently, hence a battery charger stage which is a regulated d.c from main voltage is used to charge the battery with a logic control sensing circuit to cut off the charging voltage when the battery is fully charged.

Also a relay is biased to switch main voltage to output when there is a public supply to conserve power for the unit to make it friendlier.

3.1 OSCILLATOR STAGE

The oscillator stage is the heart of digital UPS design. The inverter need to generate a.c voltage at a frequency of 50Hz. hence, there has to be some kind of oscillator circuit for this to be achieved. The oscillator stage here is a pulse width modulator IC. The pulse width modulator has an internal RC oscillator, which could he made to oscillate to frequencies in excess of 1MHz

depending on external components used. The advantage of using pulse width modulator is that the inverter gives a low harmonic content of the frequency, which is suitable for inductive loads.

The pulse width modulator is made of a generates sine wave and modulator triangular wave at a relatively higher frequency. The ouput results in waveforms of unequal length and pulses. The circuit of the oscillator is shown below

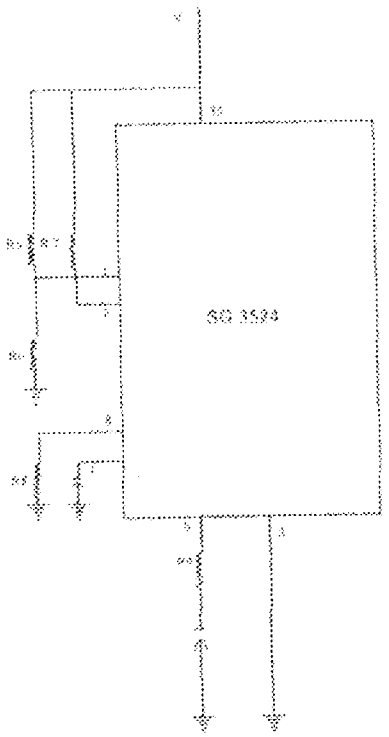


Fig. 3.1 Pulse width modulator

The oscillator outputs of a frequency that 180° out of phase from each other between pin 11 and 12. the output of the oscillator state now goes to a driver stage, which feeds the inverter transistors. The frequency of the oscillator is given by

F = 1/RC (where R and C are the frequency determining components)

For F = 50Hz using capacitor capacitance 0.1μF, the value of resistor R can be calculated thus from,

F = 1/RC

$R = 1/FC$

$R = 1/50 \times 0.1 \times 10^{-6}$)

R4, R5 and R6 are resistors that bias the internal amplifier in the pulse width modulator.

3.2 DRIVER STAGE

The input of the mosfet have a very high input impedance which make the driver stage dispensable but when mosfets are connected in parallel, it is often require that their gate be isolated. The driver stage not only matches the oscillator to the amplifier, but also, ensure that the gate of the parallel mosfet are properly isolated from each other even if they are driven from the same source.

The driver stage is an emitter follower transistor configuration, the emitter follower doesn't really amplify current but increases the current sourcing capability to the limits of the Follower transistor. hence, the emitter follower ensures transfer from the oscillator to the base of the push-pull amplifier. The fig below shows the driver stage.

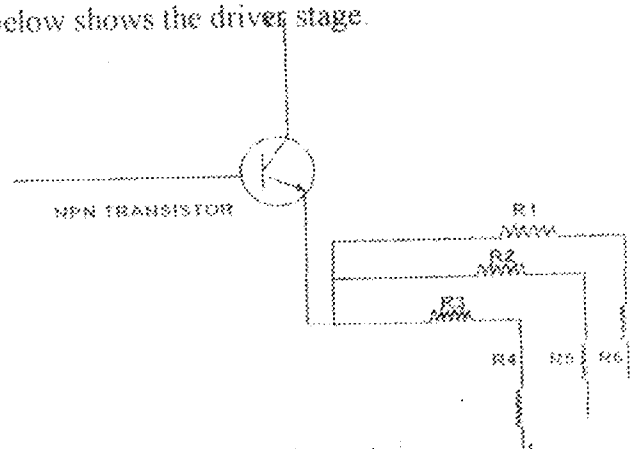


Fig 3.2 Driver Stage

Resistor R1 to R6 is a potential divider used to isolate the various gate voltages

Since, I_c/I_b hfe

$I_b = I_c/h_{fe}$

For an hfe of 1000 (using Darlington transistor) I_b will be relatively smaller compared to

I Hence, a small `B allow the require k to get to the gate via the emitter

3.3 CLASS B AMPLIFIER STAGE

The class B amplifier is where voltage polarity and power generation takes place. A čenire tap transformer is required for switching of the push-pull arrangement. TI and i'2 are the power mosfet and DI and D2 are to protect the switches from reserve voltage spike. The fig below shows the push-pull amplifier stage.

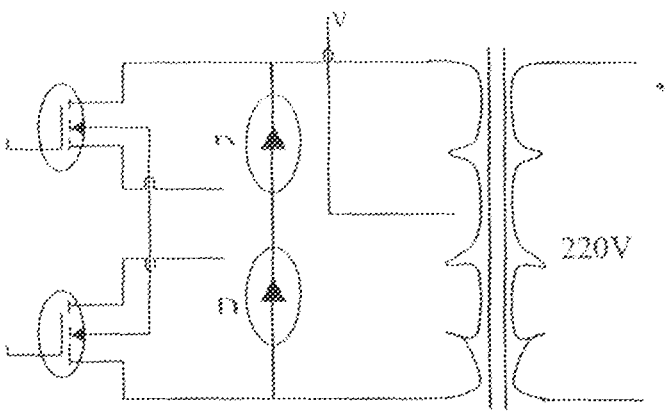


Fig 3.3. Class B amplifier stage

When large amount of power is needed the mosfet is cascaded to get the amount of were required. The power to be generated depends on the capacity of the mosfet and the ting of the transformer.

The class B amplifier has a maximum efficiency of 78%, to achieve an UPS of a particular were output; the efficiency losses must be put into consideration

Power output for our design is 500 VA.

By using a power factor of 0.7 (due to losses).

The output power = 0.7 x 500 VA = 350 watt

For power to be equal to 350W,

I = 350/12 (using 12V battery)

I= 29.17A

This implies that the power element must have a current handling capability in excess of 29.1 7A.

Since maximum a.c power is given by

$P_{ac} = V_{cc} I_{max}/2$

$P_{ac} = \frac{12 \times 29.17}{2}$

$= 175$ watts

The power dissipation of the circuit is given by

$P_{diss} = (2 \times Pac)/\pi$

$P_{diss} = \frac{2 \times 175}{\pi}$

$= 111.39$ watts

This means that the energy dissipated as heat on the mosfet on full load will be approximate 111.39 watts. The choice of mosfet selection depends on maximum current and power dissipation of the project IRF540 MOSFET was used. The IRF540 has the following

specifications

$I_{DS\,(max)}$	$V_{DS\,(max)}$	$P_{D(max)}$
39A	60V	150Watts

Where I_D.....Drain current

V_{DS}..... Drain source voltage

P_D... .....Power dissipated

3.4 BATTERY CHARGER STAGE

The battery charger stage is made up of a sensing circuit to automatically shut down the charger when the battery is charged and a d.c voltage source, which is the charging voltage

For a sealed lead - acid battery, each cell provides 2V. Thus a 1 2V battery of this type consists of six cells connected in series. The fixed "float" voltage required per cell to maintain the charge on the battery indefinitely is between 2.3V and 2.4V. Thus, for the 12V battery the fixed "float" voltage is between

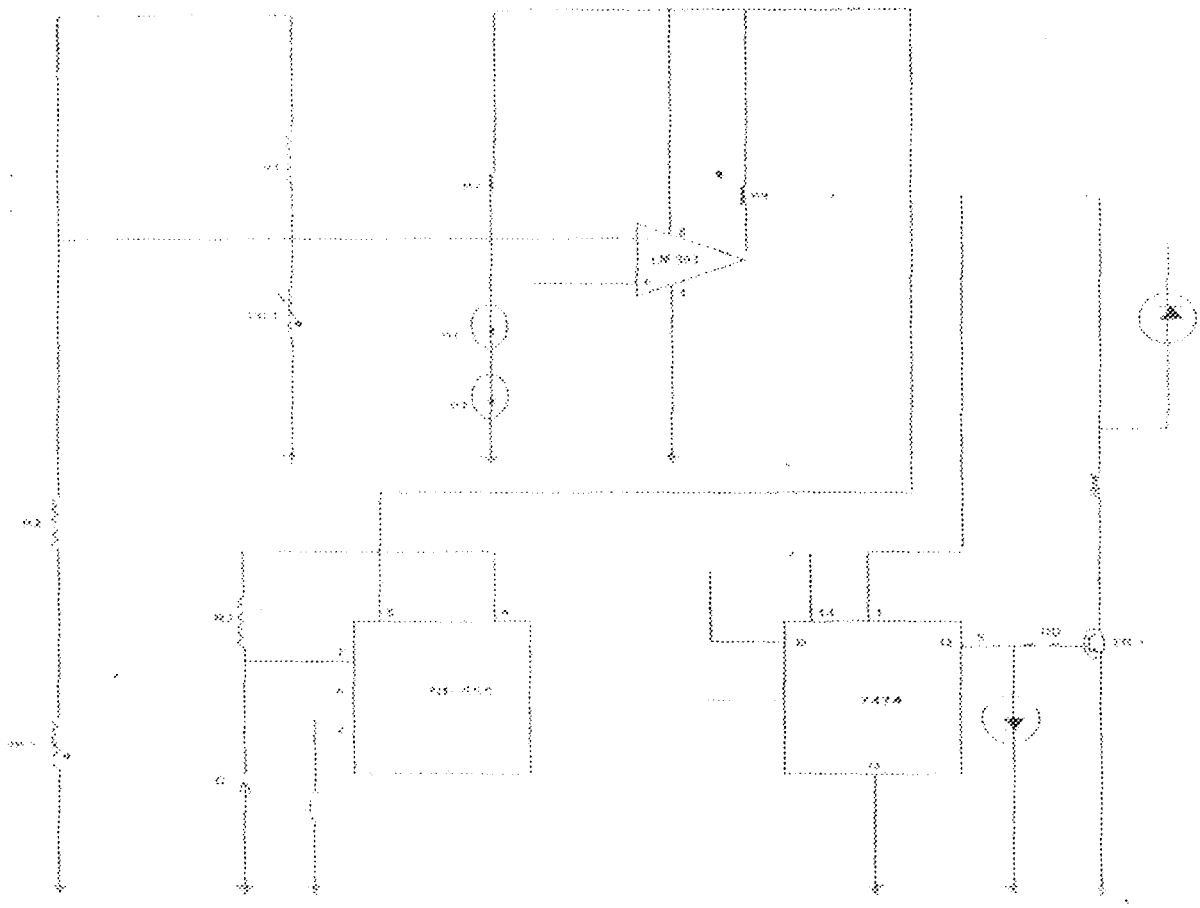
6 x 2.3 13 8V and

6 x 2.4 = 14 4V

The higher value will be picked since this mean a faster charging rate. This is desirable in a situation where frequency of black out is high

The charger stage is shown in the fig below

Fig 2.4 BATTERY CHARGE STAGE



The charging circuit is a constant voltage type. The chagrin voltage is derived from constant regulated d.c voltage while the control for the charge is composed of a combinational logic circuit.

The comparator compares the battery voltage with a fixed reference and detect when the battery is fully charged.

The monostable on the other hand detect when the battery is discharge and automatically initiates charging. We shall consider each of the charger stage separately.

3.4.1 CHARGING VOLTAGE

For a charging voltage of 14.4 d.c, the unregulated supply needs a transform,

$$14.1/(2)^{1/2}$$

= 10.18V - 10.2V

Hence, a 10.2V a.c transformer would be required

The charging current should be about 10% of the battery capacity. Hence, for a 60Ah battery, 6A would suffice. This also implies that the transformer must be able to deliver 6A current at the sped fied charging voltage. The output wave form after rectification shown in the figure below

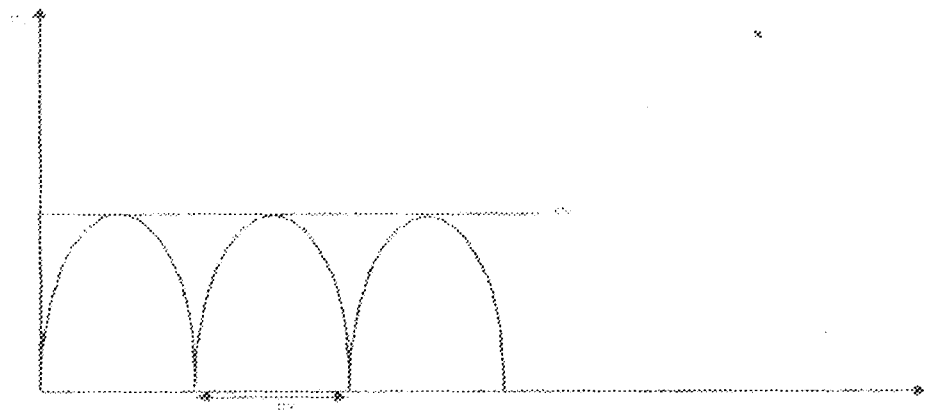


Fig3.4.1 Rectified d.c Voltage

Where dv is the ripple voltage for time dt, where dt is a dependent in power supply frequency

For an rms voltage of 10.2volts (from transformer)

V_{peak} 10 x $\sqrt{2}$ (i.e.,rms x $\sqrt{2}$)

V_{peak} 14.4V

Hence letting a ripple factor of 20% (since the ripple noise will not affect the battery in anyway)

dv = 2.88 and dt 10ms (for 50Hz)

But I/C $\frac{dv}{dt}$

$$C = \frac{dt}{dv}$$

$$C = \frac{2.88}{10ms}$$

$C = 3472\mu F$

C 3300-4F (Nearest Preferred value)

3.4.2 COMPARATOR STAGE.

The function of the comparator is to compare two voltages and give an output, which tell if they are equal or unequal. The comparator stage in this circuit is used to sense when the battery is charge. A reference voltage of 1.2V is applied to the non- inverting input of the comparator, generated by the drop across D_1 and D_2.

When the charging voltage is impressed on the battery, it drops and increases exponentially as the battery charges. When the battery is fully charged, the voltage on the battery rises to the charging voltage (i.e. 14.4V). VR_1 will be adjusted such that at 28.8V a drop of 1 .2V will be at the inverting input of the comparator. This will set the comparator at the threshold of switching and any further charging will increase this voltage, which will consequently cause the output of the comparator to drop. The drop is use to RESET the D-type flip-flop which in turn switches off the transistor controlling relay.

The comparator stage is shown fig 2.4.2

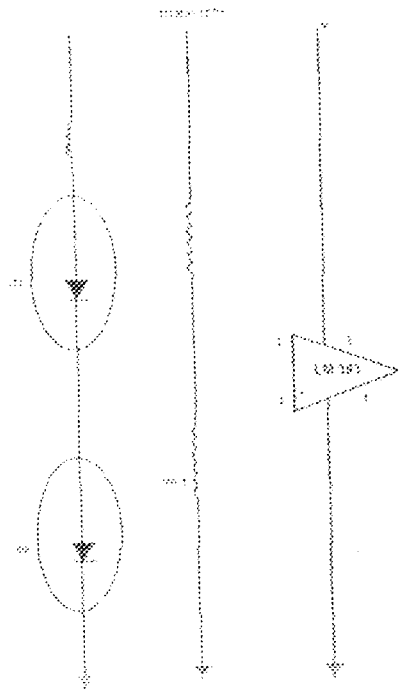


FIG 3.4.2 COMPARATOR CIRCUIT

$V_{out} = A_0 V_{in}$

Where A_0 = open loop voltage gain.

And Vin = V' - V"

V_{out} will drop to V+ for the slightest positive difference in voltage since A0 is often very large (in order of 20000)

As the battery tends to go above 14.4V, the drop across VR1 tend to exceed 1.2V, hence the output drop to V_{-}, and switches a transistor circuit which control a relay that cut off the charger.

3.4.3 MONOSTABLE DESIGN.

The monostable multivibrator is a form of relaxation oscillator that only has one stable state. When triggered the multivibrator goes to its unstable state for time

T =1.1RC and turns to its stable state. The trigger condition for the monostable is that the voltage at its trigger input be 1/3 V_{cc}

To achieve the trigger condition the voltage at the trigger is not discharge, the drop at the bigger input is just 1/3 V_{cc}. The discharge voltage of the battery is set to be +20V. Hence, the battery is assumed to be discharge when it is +20V. The Vcc of the timer is 5V. The monostable stage once triggered clocks the flip-flop and puts it in the set mode to allow for charging.

3.4.4 LOGIC CONTROL

The logic control is built around a D- type flip-flop. It is the flip-flop that tells the system when to start and stop charging the battery. The operation of the system is described in the truth table below.

Mode	D input	Ck	Q	Q	R
Setup	1	↑	1	0	1
Reset	0	X	0	1	1
Hold	X	X	0	1	0

X Don't care

↑ Rising edge

Q and Q Outputs

D Data input

The logic control circuit operates in its set and hold mode. When the monostable sends clock signal, the flip-flop shifts data from the data input to the Q output to start charging. When the battery is charged, the comparator sends a low to the reset input to set the flip-flop to hold mode to stop the charging. The diagram of the flip-flop stage is shown in fig below.

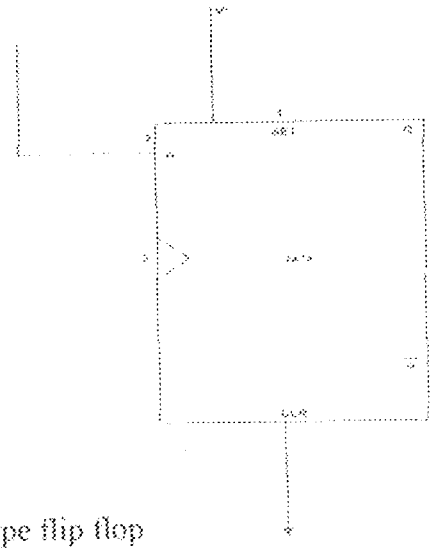


FIG 3.4.4 D-Type flip flop

3.5 DIGITAL VOLTMETER

3.5.1 VOLTAGE CONTROLLED OSCILLATOR.

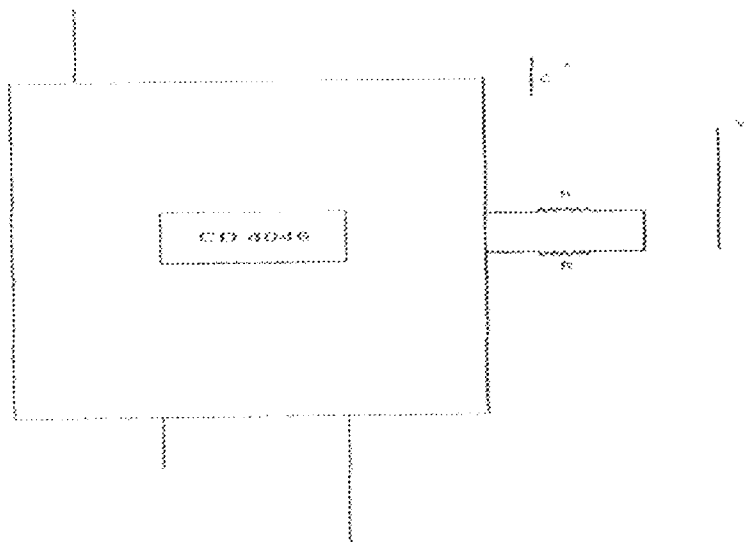


FIG 3.5.1 A VOLTAGE CONTROLLED OSCILLATOR STAGE

The CD4046 is a CMOS PLL, which has an internal Voltage Controlled Oscillator.

The system has an offset voltage near zero but this could be taken care of from the calibration circuit in the counter.

The frequency of the oscillator is given by

$$F_o = \frac{1}{1.1RC}$$

Where R & C are external resistor and capacitor values

For F_o=.....Hz, and letting C = ...μF

3.5.2 COUNTER CALIBRATOR.

The 7490-decade counter form part of the frequency counter stage. The 7490 have already been analyzed in the literature review stage. The 7490 receives clock pulses through its clock input from the AND gate.

The clocking sequence for the 7490 counter is basically for an UP COUNTER, but the nature of counting in the frequency counter is such that the counters are allowed to count for a fixed time control and the count stored in a latch before resetting occurs. For counting to occur the reset inputs (pins 2 & 3) must be LOW, and for latching to be enables the LE (Latch Enable) input must be triggered by a LOW to HIGH clock transition. Fig 2.5.2 shows the cascaded counter.

To inhibit counting the reset inputs most go LOW. Since the 7490 are a decade counter, three-decade counters are therefore cascaded together to give room for counting to 999. This cascading becomes necessary if a maximum speed of about 100km/hr is the set target.

The 7490 have no carry out output hence the most significant bit (MSB) output is connected to the clock input of the next as shown below

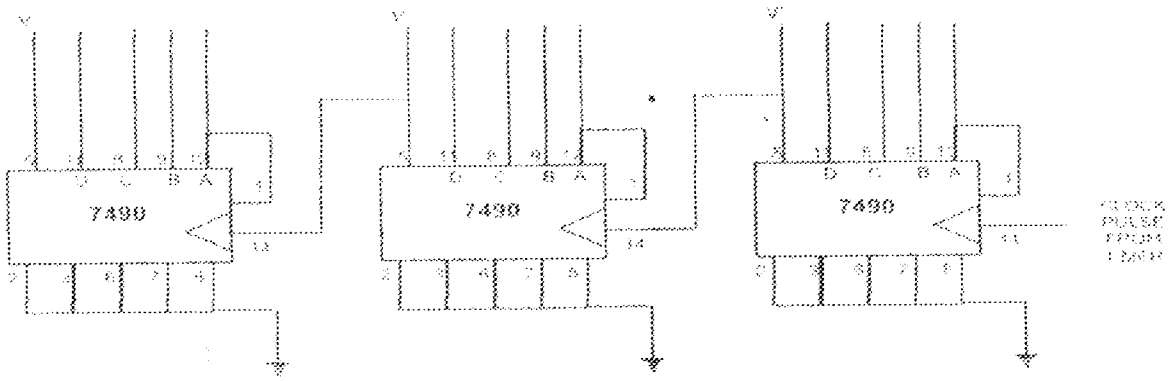


FIG 3.5.2 **CASCADE 7490 DECADE COUNTERS**

The counting control is done via the reset pins (2 & 3). Since reset pin has to be LOW For counter to operate, the sequence below shows how the counter calibrator controls counting. latching and resetting.

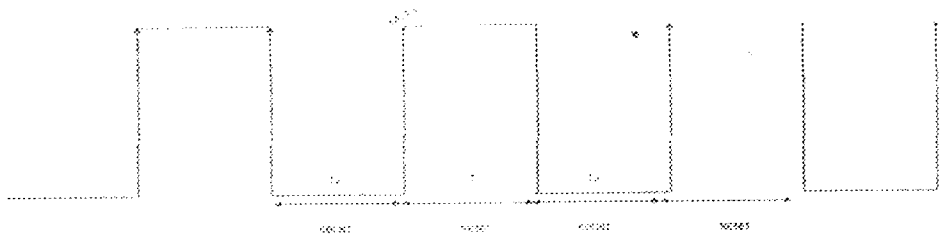


FIG 3.5.2b **SEQUENCE OF COUNT, LATCH AND RESET**

3.5.3 DECODER/DRIVERS AND DISPLAY.

The 7447 is 7 - segment decoder which accepts a 4 - bit BCD and produces the appropriate outputs for selection of segments in a 7 segment displaying arrangement used for representing the decimal numbers 0 to 9.

The output (a,b,c, d,e,f and g) of the decoder, select the corresponding segment as shown in the figure below.

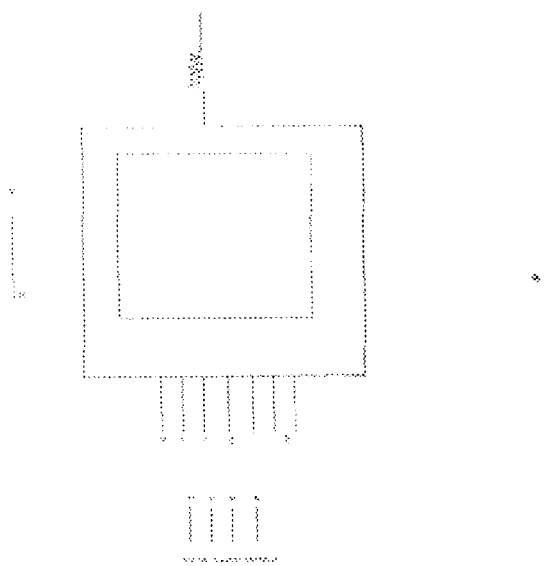


FIG 3.5.3 **SEVEN SEGMENT DIGITAL DISPLAY**

The value of the limiting resistor R_S is calculated is shown below. The display has the following specifications,

Max. Forward current (I_f) = 16mA

Voltage drop across each LED V_{LED} = 1.7V

And V^+ =5V

$V^+ = I_f R_{SC} + V_{LED}$

$$= \frac{V^+ - VLED}{I_f}$$

$$= \frac{5 - 1.7}{16mA}$$

$$= \frac{3.3}{16mA}$$

= 206.2ohms

R_S = 200ohms

3.5.4 COUNTER CALIBRATOR.

The counter calibrator generates the sequence shown in fig 3.7 and this fed to the counter and the latches. The counter calibrator is an astable 555 timers. The counter calibrator circuit is shown in fig. 2.5.4

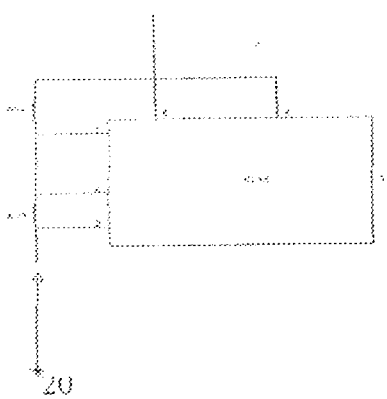


FIG 3.5.4 COUNTER CALBRATOR

Since V_{co} centre frequency is 1kHz, at maximum voltage input frequency count should be 1 60pulses since the maximum speed is 160km/hr. Hence count time

t_{on} 160

2000

= 0 08S

T_{off} 0.08s

Since $T = t_{on} + t_{off}$, considering that ton duration is of no consequence to the displayed value, we can let

$T_{on} = t_{off}$ Hence,

$T = 0.08 \times 2$

$= 0.16s$

And F =6 6Hz

For duty cycle of the output waveform to be symmetrical, R_B (~ R_{35}) must be > R_A (R_{34}), hence letting

R_{34} = 1k and C = 1 μF, then from

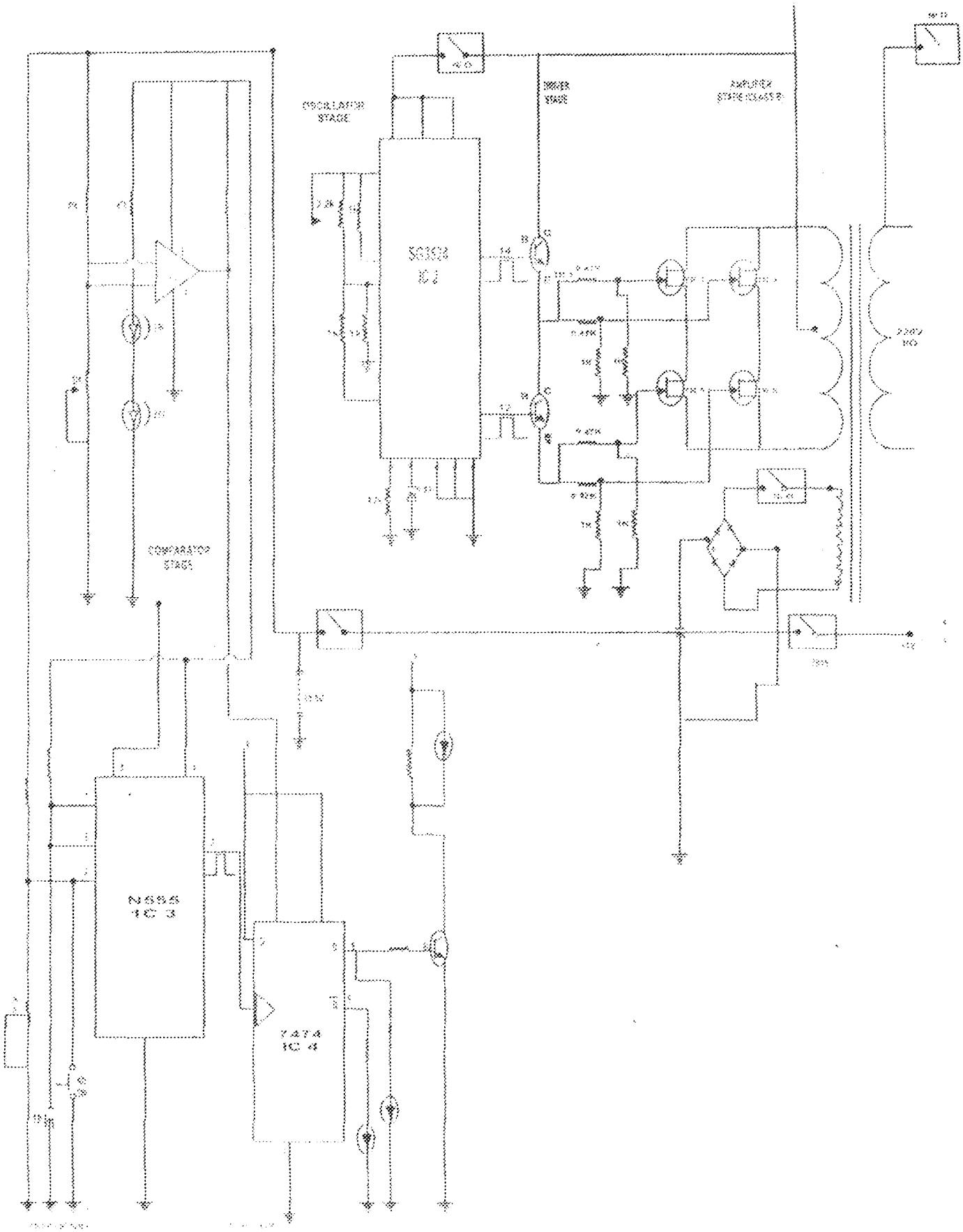
$$F = \frac{1.44}{(R_A + 2R_B)C}$$

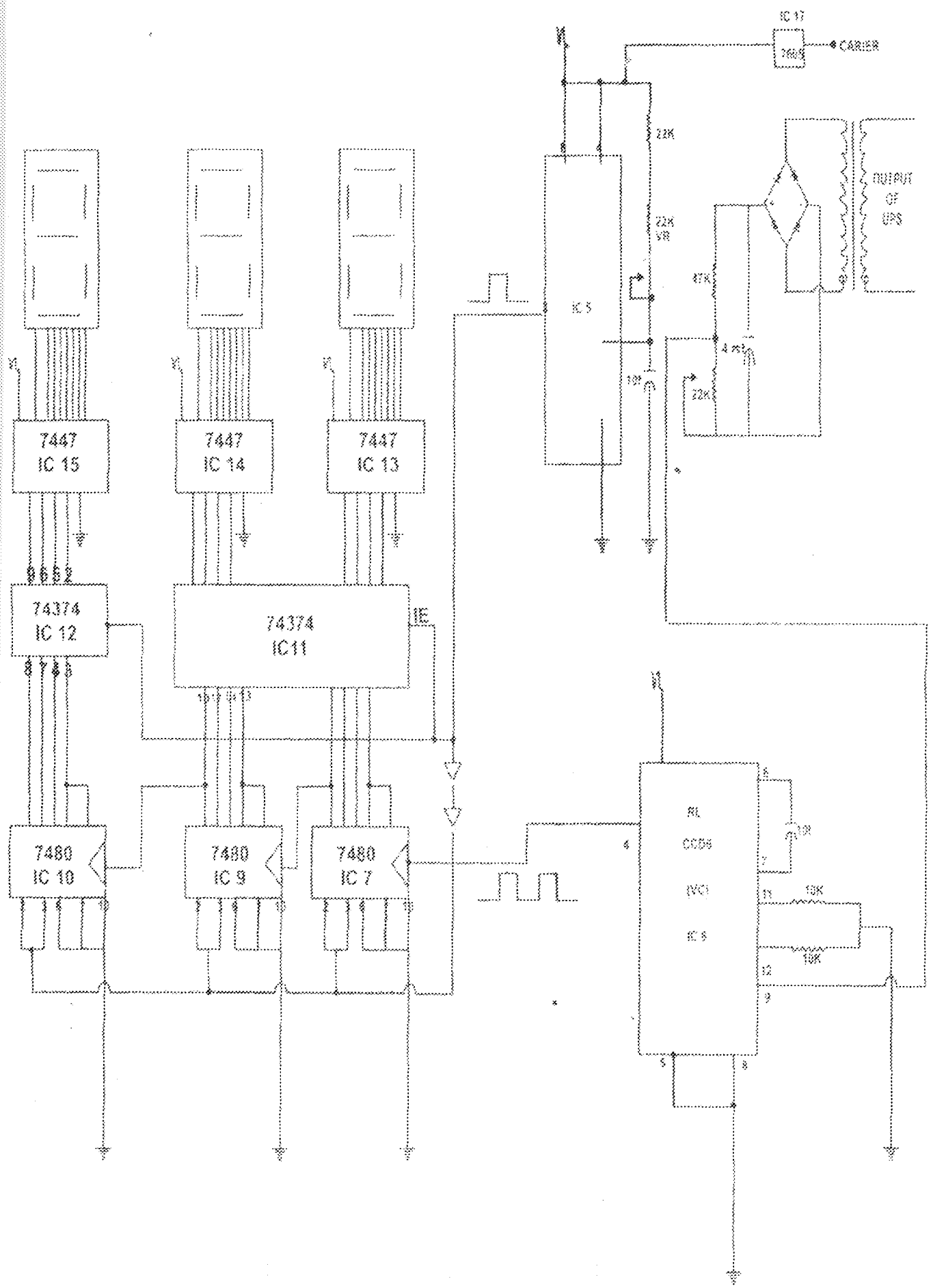
$$R_B = \frac{1.44}{Fc} \qquad R_A$$

RB = 108.5kilo-ohms

Hence R_{34} = 1k, R_{35} 108.5k and C = 1μF

The latches and used to hold the count till another calibration process takes place. This is to enable a changing input variable from the counter to be updated


OSCILLATOR STAGE
DRIVER STAGE
AMPLIFIER STAGE
SG3524 IC 2
COMPARATOR STAGE
NE555 IC 3
7474 IC 4



COMPLETE CIRCUIT DIAGRAM OF A DIGITAL UPS/ INVERTER

CHAPTER FOUR

TESTING, CONSTRUCTION AND IMPLEMENTATION

4.0 CONSTRUCTION AND IMPLEMENTATION.

The construction of the project (electronic power inverter or 500VA digital ups) was done in two different stages.

1. The soldering of the components on different Vero boards.

2. The coupling of the entire project to the casing.

From the fuished work, it could be emphasized that the coupling of the project was done on three Vero board and a printed circuit board. The printed circuit board was used to isolate the soldering of the power mosfets used I the driver stage and class b amplifier stage because of the large amount of heat dissipated from the mosfet.

The practical usage of three Vero boards enables or gives the opportunity to isolate each stage when the need for troubleshooting of the project arises and also reduces error in the soldering of the components. Hence, this gives the user the opportunity to troubleshoot the device with ease when fault arise.

The figure below gives a clearer description and self-explanatory tips in the construction of the 500va digital ups, it also indicates how each component was mounted on different Vero board.

Figure4.0 shows Vero board 1 and the various components mounted.

Figure 4.0b shows Vero board 2, which is the oscillator and driver stage.

Figure 4.0c shows Vero board 3 containing the ADC and the power supply of the charger.

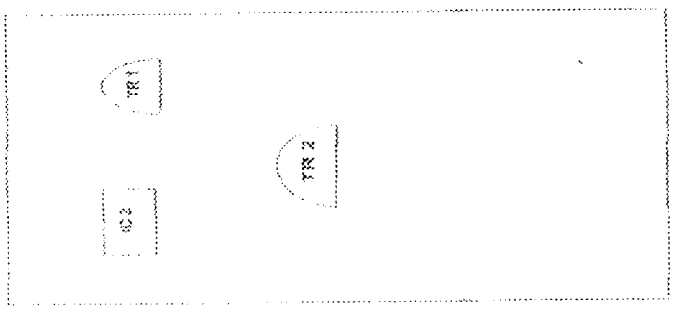


Fig 4.0.a Vero Board 1

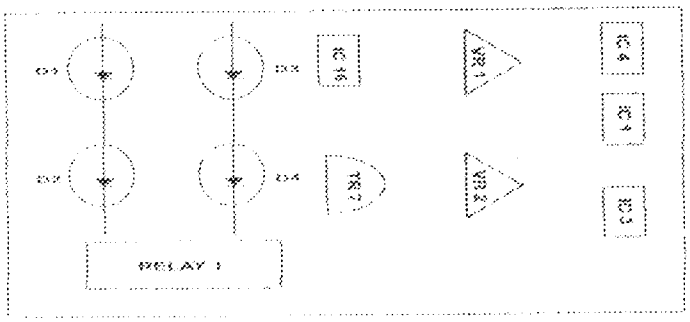


Fig 4.0.b Vero Board 2

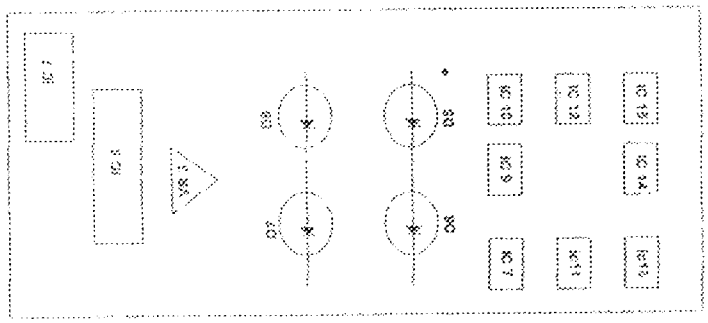


Fig 3.0 c Vero Board 3

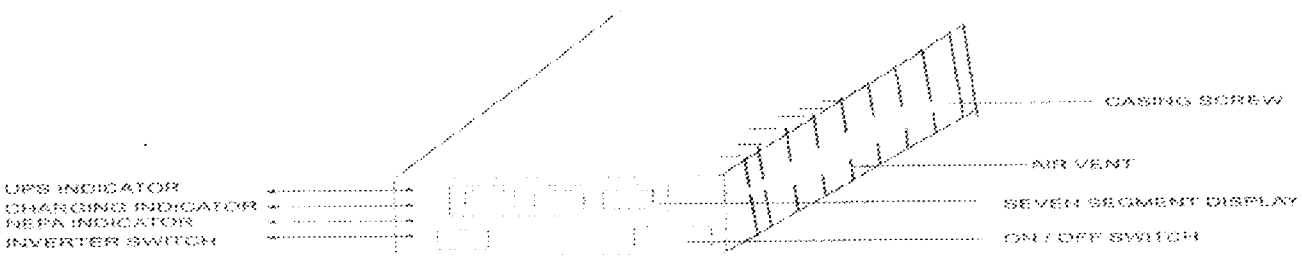


Fig4.0.d Isometric view of the casing

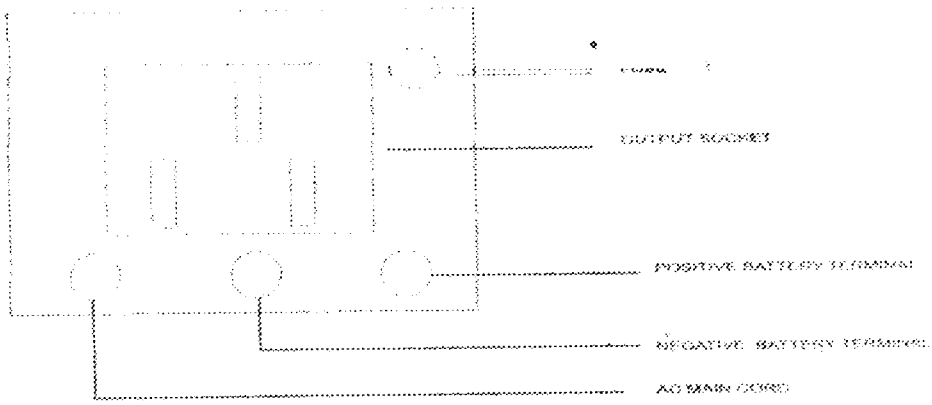


Fig 4.0.e Back view of the casing

4.1 TESTING.

After carrying out the paper design and analysis, the project was implemented and tested to ensure it working ability.

All necessary connection and soldering were carefully made and the digital ups was connected to a 12volts 60AH battery.

During the testing, it was observed that the op-amp voltage swings were not symmetric and the output of the inverter was high at no-load condition.

The output voltage was then measured, thereby making it safe to connect various loads to the output of the inverter unit.

4.2 PROBLEMS ENCOUNTERED.

Series of problems were encountered during the implementation, construction and testing of the project, which are as follows;

1. The transformer was difficult to obtain but was later ordered.

2 The transformer was heating during charging, a cooling fan is highly recommended.

3 The efficiency of the system is about 70percent. Hence, a 600va ups was designed so that the efficiency losses would be compensated.

4 The power mosfets were dissipating heat. Hence, heat sinks were placed on each to allow for proper heat dissipation.

5 The UPS goes high on no-load condition. Putting a feedback circuit to control the output could solve this problem.

6 The PLL is not linear for the entire voltage range. Hence, only voltages between 180 and 240 are accurate.

7 A software module should be designed for the ups/inverter.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATION

5.0 CONCLUSION.

The project was designed considering some factors such as economy, availability of components and research materials, efficiency, compatibility and portability and also durability.

The performance of the project after test met design specification and hence can be said to be satisfactory

The general operation of the project and performance is dependent on the user ,who is-prone to make human errors such as battery polarity reversal, overhauling etc. however, there is provision for overload protection using a fuse in the output.

In addition the construction was done in such a way that it makes maintenance and repairs an easy task and affordable for the user.

The project has really exposed power electronics and practical electronics as well as me to digital generally which is one of the major challenges I shall meet in my field now and in the future.

The design of the digital ups/inverter was quite challenging and tedious when compared to a regular inverter.

I wish to thank the department, my supervisor and project co-ordinator for giving me the opportunity to carry out this project work. However, like every aspects of engineering, there is room for improvement and further research on the project as suggested in the recommendation below

5.1 RECOMMENDATION.

a. I would recommend that further work be done on the area of the digital display to get a wider linear range.

b. The department should obtain more digital simulators and equipments

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