DESIGN AND CONSTRUCTION OF "FEDERAL UNIVERSITY OF TECHNOLOGY MINNA" LIGHT SEQUENCER DISPLAY.

BY

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FEDERAL UNIVERSITY OF TECHNOLOGY

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MARCH 2000.

DEDICATION

I dedicate this project to the LORD for guiding and protecting me thus far. I will forever sing praises to your name.

I also dedicate this project to my parents Gboyega and Moji Olatunji for inspiring me and ensuring that I get a qualitative education. I love you both very much.

CERTIFICATION

This is to certify that this project titled "DESIGN AND CONSTRUCTION OF FEDERAL UNIVERSITY OF TECHNOLOGY MINNA LIGHT SEQUENCER DISPLAY" was carried out by OLATUNJI IFEDAYO OLALEKAN under the supervision of Mr. I. A. Danjuma and submitted to Electrical and Computer Engineering Department, Federal University of Technology, Minna in partial fulfillment of the requirements for the award of Bachelor of Engineering (B. ENG.) degree in Electrical and Computer Engineering.

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DECLARATION

I, Olatunji Ifedayo O. hereby declare that this project was wholly conducted by me under the able supervision of Mr. I. A. Danjuma of the Department of Electrical and Computer Engineering, Federal University of Technology, Minna.

Signature

21-03-2000

Date

ACKNOWLEDGEMENT

I would like to express my gratitude to GOD ALMIGTY, who has guided me thus far in all spheres of life particularly while working on this project. It is to you LORD that I give the entire honor and glory.

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ABSTRACT

This project report presents the design and construction of a light sequencer display. Although, most practical light sequencer displays in use today consists of those controlled by an Electrically Erasable Programmable Read Only Memory (EEPROM). The EEPROM is programmed by a programmer in such a way that the visual display will light in the order in which it was programmed in the EEPROM. Although, we also have other more sophisticated visual displays but, for the purpose of this project a shift register (74LS164) was used to display our output sequentially using light emitting diodes (LEDS) in place of the more sophisticated and expensive EEPROM.

The shift register (74LS164) shifts the output in a serial-in-parallel-out (SIPO) mode, in order to display our characters both in the sequential and group modes.

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CHAPTER 1

GENERAL INTRODUCTION.

1.1 INTRODUCTION

Notice board have a very important place in the advertising industry. The purpose of this board is to create a very simple way of dissemination of information to the general public. This has necessitated the design of notice boards that can easily attract or draw the attention of people to the board and hence to read the text display on the board. Thus they have become indispensable in the advertising industry as a result of their simplicity and reliability.

This board may come in different types which may be classified into (i) electronic boards (ii) non electronic board.

The electronic board have become preferable in recent years due to its relatively low cost of production, as a result of the development that has occurred in the electronic industry. Also, the electronic boards possess an attractive quality that makes them very simple to read and understand.

Thus, this project involves the design of an electronic display board which will go a long way in improving and solving the problems encountered in the advertising industry.

1.2 AIMS AND OBJECTIVES.

The aim and objective of this project is to make or present a more effective way of dissemination of information because it is more attractive. The project is meant to create a more versatile way of passing information digitally. Although, opticians have observed that the eyes is more attracted to moving objects. Thus, the main aim is to create an attractive visual display to the human eye. Thus, everybody including those in moving cars will be attracted to the display and will read it.

Another aim or objective of this project is to enable the human eye read or see moving display when it is dark. This will therefore, overcome other forms of dissemination of information that are not as sophisticated and of technological advancement as that of moving visual displays, billboards and signboards.

In conclusion, the moving display will be readable both in the daytime and in the dark, and it is more attractive to the human eye.

1.3 LITERATURE REVIEW.

Signboards have been in existence for centuries and are used as marketing tools. They are tools in the sense that signboards can be used for advertising products, services e.t.c. Thus, in this way, signboards can actually help in promoting a manufactures products and services.

Nowadays, electronic signboards are being used. The electronic sign boards have so many advantages over the normal (non-electronic) signboards and bill-boards. These advantages include;

1. Electronic signboards are more interactive in the sense that they can be used to display as many messages as possible on the same board.

2. Electronic signboards are more visually attractive at nights than other normal signboards and billboards. They can be easily read and noticed in the night.

3. Electronic signboards are also flexible in the sense that they can display different modes (i.e. sequential, random, group modes e.t.c) over a period of time.

Electronic signboards can be used for advertisement to the public. "The advertised message, or advertisement is delivered to it's intended audience through the various media including newspapers, magazines, television, radio, bill-boards and direct mail"

Other applications of electronics signboards include promotion of goods and services by making the visual display attract customers. Electronic signboards are also used in schools, hospitals, hotels, restaurants, and e.t.c.

1.4 PROJECT OUTLINE.

The first chapter attempts to explain in details what this project intends to achieve i.e.its aim and objectives. This chapter also includes the Literature Review and the Project Outline.

The second chapter deals with the system designs of the power supply, square wave generator (astable multivibrator), driver circuitry and the display unit consisting of LEDs (light emitting diodes).It also contains internal descriptions of the integrated circuits (ICs) used i.e. the shift registers and the JK flip-flop used for the toggling unit.

The third chapter explains the construction of the various stages designed in Chapter Two. The testing of each stage, recording of the results obtained after testing and comparing the obtained results with the calculated design values in Chapter Two.

The fourth chapter contains the Conclusion and Recommendations on how this design can be improved upon.

CHAPTER 2.

SYSTEM DESIGN AND ANALYSIS.

This chapter reveals the detailed explanation of the various components used in the design of this project.

2.1 DESIGN OF SQUARE WAVE GENERATOR (ASTABLE - MULTIVIBRATOR).

The square wave generator is designed using a 555-timer integrated circuit (I.C). The 555 timer combines a relaxation oscillator, two comparators, an RS flip-flop and a discharged transistor. The figures below show part of the internal construction of an RS flip-flop and also the symbol of an RS flip-flop.

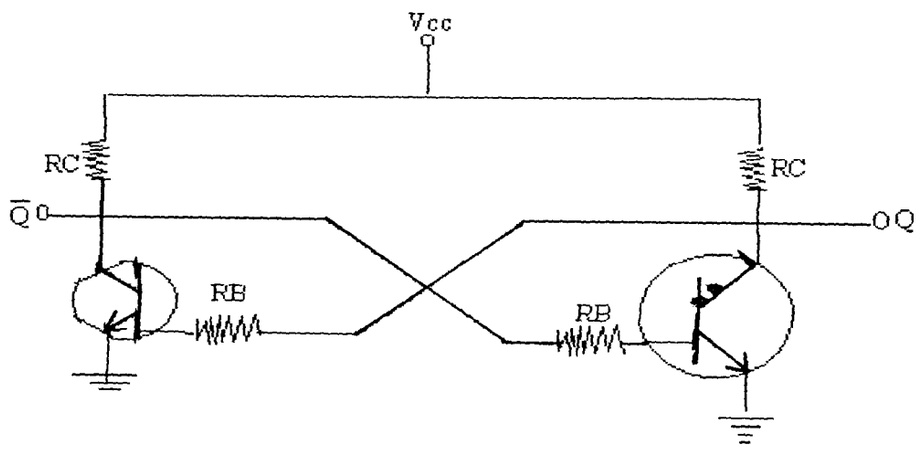


Fig. 2.1 (a): Part of an RS flip-flop.

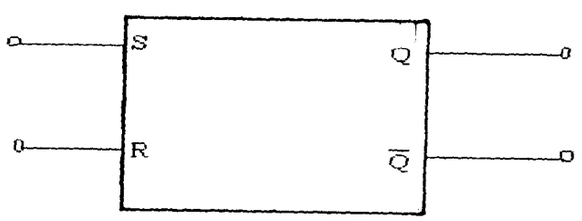


Fig. 2.1(b): Symbol for RS flip-flop.

It can be seen from figure (a) above that an RS flip-flop consists of a pair of cross-coupled transistors. Each collector drives the opposite base through a resistance R_b. In a circuit like this,

one transistor is saturated and the other is cut off. For instance, if the right transistor is saturated, its collector voltage is approximately zero. This means that there is no base drive for the left transistor and so it goes into cut-off and its collector voltage approaches $+V_{cc}$. The high voltage (i.e $+V_{cc}$) produces enough base current to keep the right transistor in saturation.

On the other hand, if the right transistor is cut-off then its collector voltage drives the left transistor into saturation. The low collector voltage out of this left transistor then keeps the right transistor in cut-off. Depending on which transistor is saturated, the Q output is either low or high. By adding more components to the circuit, we get an RS flip-flop that can set the $\overline{Q}$ output to high or reset to low. Incidentally, a contemporary (opposite) output Q is available from the collector of the other transistor at any point in time.

Figure 2.1(b) above shows the symbol of an RS flip-flop of any design. The flip-flop latches in either of two states. A high S input sets Q to high while a high R input resets $\overline{Q}$ to low. Q (output) remains in a given state until it is triggered into the opposite state. The figure 11 below shows the truth table for RS flip-flop.

S	R	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	X	X

X - Not allowed condition

Fig 2.2: Truth table for an RS flip-flop.

Figure2.3 below could be used to explain the basic timing concept of a 555 timer.

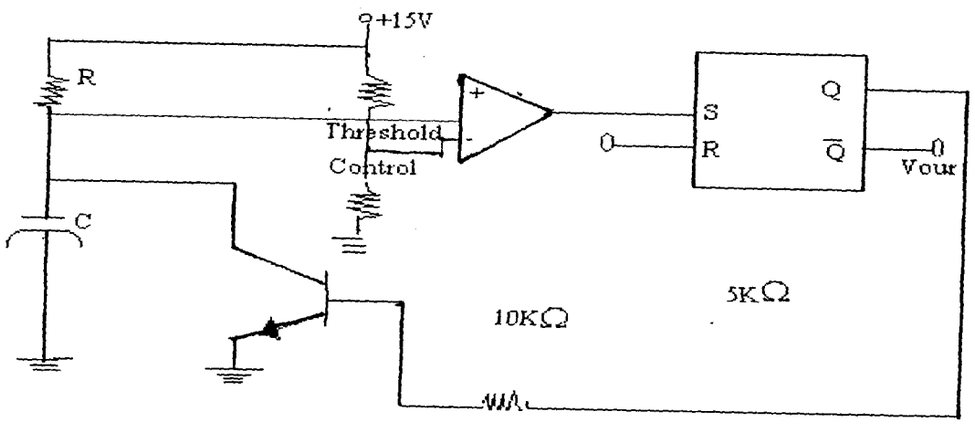


Fig. 2.3(a): Basic timing

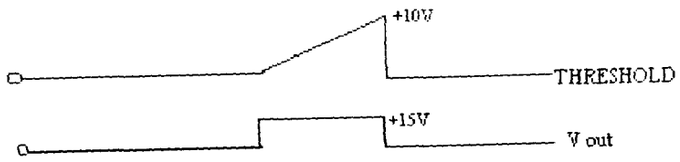


Fig. 2.3(b): Capacitor and output voltage waveforms.

Assuming that Q output is high. This saturate the transistor and clamps the capacitor voltage at ground i.e. the capacitor is shot circuited and cannot charge.

The non-inverting input of the comparator is called the threshold voltage and the inverting input voltage is referred to as a control voltage. With the RS flip-flop set, the saturated transistor holds the threshold voltage at zero. The control voltage on the other hand, is fixed at 10V due to the voltage divider.

Suppose, we apply a high voltage to the R input, this resets the RS flip-flop. Output Q now goes low and cuts off the transistor. Capacitor C is now free to charge through R towards the applied voltage. As the capacitor charges, the threshold voltage increases. Eventually the threshold voltage becomes slightly greater that the control voltage (i.e. +10V). The output of the comparator goes high forcing the RS flip-flop to set the high Q output saturates the transistor and this quickly discharges the capacitor. From the waveform in figure 2.3(b), you can see that there is an exponential rise across the capacitor and a positive going pulse appears at the Q output.

The figure 2.4 below shows a simplified block diagram of the 555 timer (eight pin I.C). Notice that the upper comparator has threshold input (pin 6) and a control input (pin 5). In most applications, the control input is not used so that the control voltage equals $+2V_{cc}/3$. As before, whenever the threshold voltage exceeds the control voltage, the high output from the comparator will set the flip-flop.

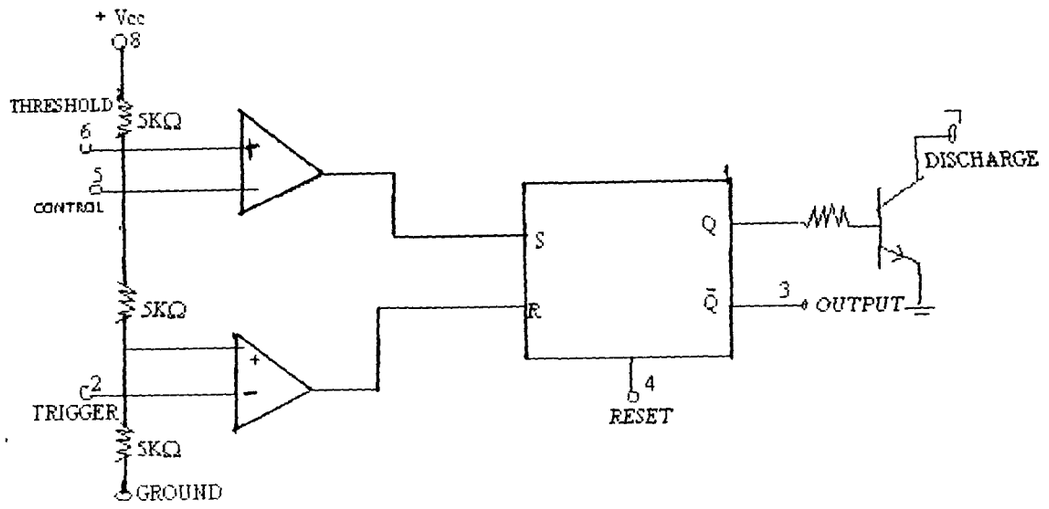


Fig 2.4 : Schematic block diagram of NE 555 timer.

The collector of the discharge transistor goes to pin 7. When this pin is connected to an external timing capacitor, a high Q output from the flip-flop will saturate the transistor and discharge capacitor. When Q is low, the transistor opens and the capacitor can charge as previously described.

The complementary signal out of the flip-flop goes to pin 3, which is the output of the timer. When the external reset (pin 4) is grounded, it inhibits the device (i.e. prevents it from working). The ON/OFF feature is sometimes useful. In most application, however the external reset is not used and pin 4 is tied directly to the supply voltage.

Notice the lower comparator's inverting input is called the trigger (pin 2). Because of the voltage divider, the non-inverting input has a fixed voltage of $+V_{cc}/3$. When the triggered input voltage is slightly less than $+V_{cc}/3$, the operational-amplifier output goes high and resets the flip-flop.

Finally, pin 1 is the chip's ground while pin 8 is the supply pin. The 555 timer can work with any supply voltage between 4.5Volts and 16Volts.

The 555 timer can be connected to operate in two modes, which are the monostable mode and the astable mode.

ASTABLE OPERATION.

Figure 2.5 shows the 555 timer connected for astable or free-running operation.

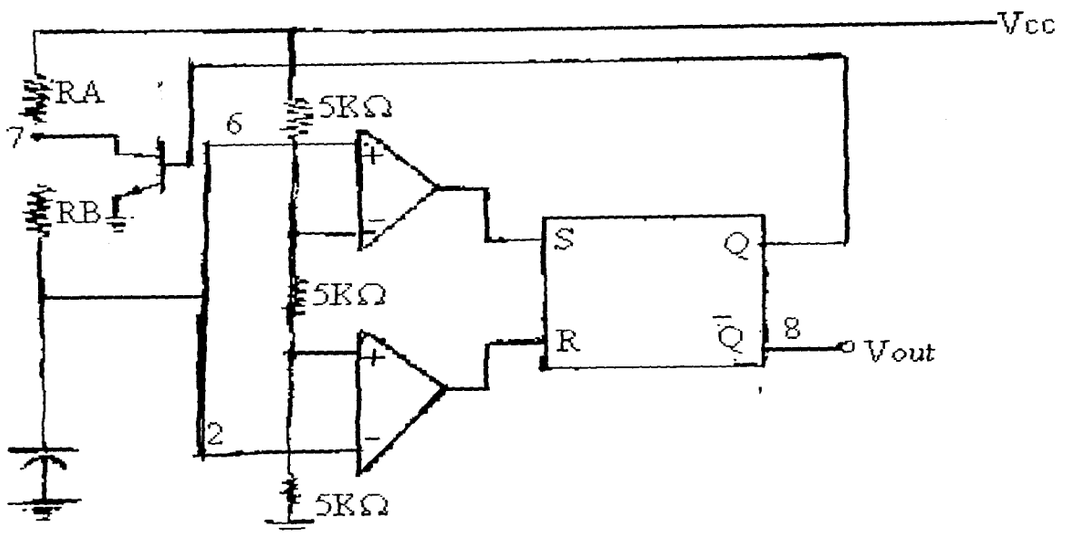


Fig.2.5(a):555 Timer connected as astable multivibrator.

When Q is low, the transistor is cut-off and the capacitor is charging through a total resistance of R_A+R_B. Due to this, the charging time constant is $(R_A+R_B)C$. As the capacitor charges, the threshold voltage increases. Eventually, the threshold voltage exceeds +2Vcc/3;then the upper comparator has a high output and this sets the flip-flop. With Q high, the transistor saturates and grounds pin 7. Now the capacitor discharges through R_B. Therefore, the discharging time constant is R_B C. When the capacitor voltage drops below +Vcc/3,the lower comparator has a high output and this resets the flip-flop.

Figure 2.5(b) illustrates the waveforms. As you can see, the timing capacitor has an exponential rising and falling voltage. The output is a rectangular wave. Since the charging time constant is longer than the discharging time constant, the output is not symmetrical and the high output state lasts longer than the low output state.

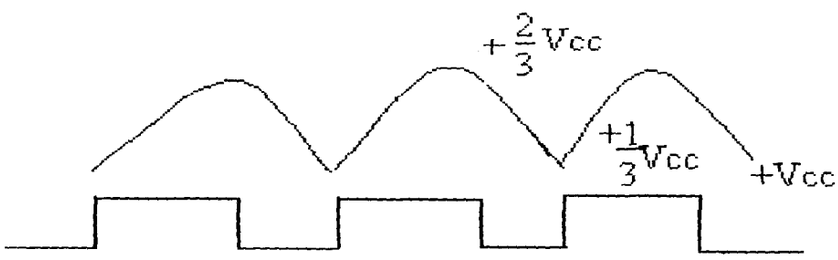


Fig 2.5(b) : 555 timer's Capacitor and Output Waveforms

The frequency of the output waveform is given as;

$$f = 1.44/(R_a+2R_b)C$$

Period of oscillation T is given as;

$$T = 1/f = 0.693(R_a+2R_b)C$$

The figure below shows the schematic diagram of the 555 timer.

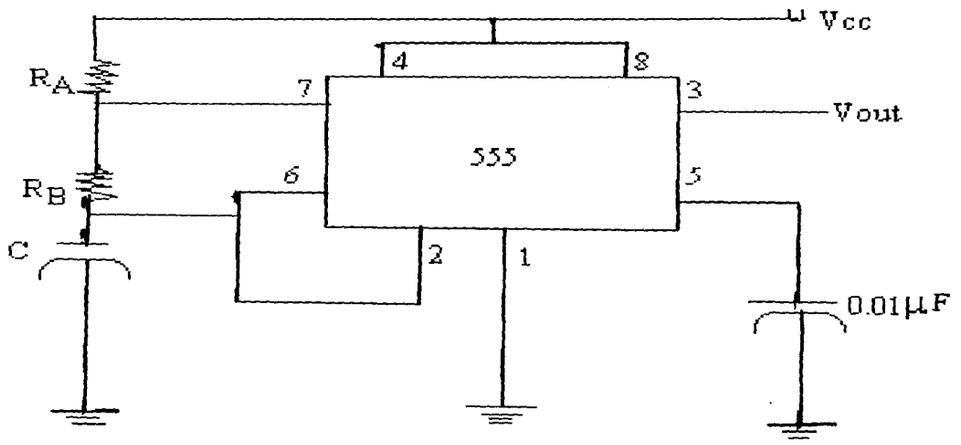


Fig 2.5(c) :Schematic diagram of 555 timer in astable mode.

Again, the pin 4 (i.e. reset pin) is tied to the supply voltage and pin 5(i.e. control pin) is bypassed to ground through a 0.01μF capacitor. An astable 555 timer is often called a free-running multivibrator because it produces a continuos train of rectangular pulses. Apart from the square wave generator, the 555 timer can also be used in different other applications such as Voltage Controlled Oscillator, Ramp Generator e.t.c

For this project, the values of the resistors and capacitor used were as follows;

$R_A = 1K\Omega$;

$R_B = 10K\Omega$;

$C = 100\mu F$

Frequency $f = (1.44/(1K\Omega+2 \times 10K\Omega) \times 100\mu F)$

$= (1.44 \times 1000 /(100 \times 21))$

$= 14.4/21 = 0.69Hz$

Frequency (f) of oscillation = 0.69Hz.

2.2. INTERNAL DESCRIPTION OF SHIFT REGISTERS (74LS164)

A shift register is a device used for the temporary storage of digital information, which then can be shifted or moved at a later time.

The shift register can be constructed using flip-flop to take the forms of;

(a) Serial In/Serial Out (SISO). (b) Parallel In/Parallel Out (PIPO).

(c) Serial In/Parallel Out (SIPO).

Data can be stored i n the shift register by either loading in series with shift pulses or in parallel by setting the flip-flops. The data can be shifted to the right one place with every shift pulse.

Figure 2.6 (a) and (b) below shows a four stage shift register using JK flip-flops arranged to allow input binary data to be shifted to the right serially with each successive clock pulse. The flip-flops are connected as D-types so that after the clock pulse the datum at each flip-flop output is the same datum as its input prior to the clock pulse. The truth table in figure shows the effect on the data bits for given binary values at the register input for serial clock pulses.

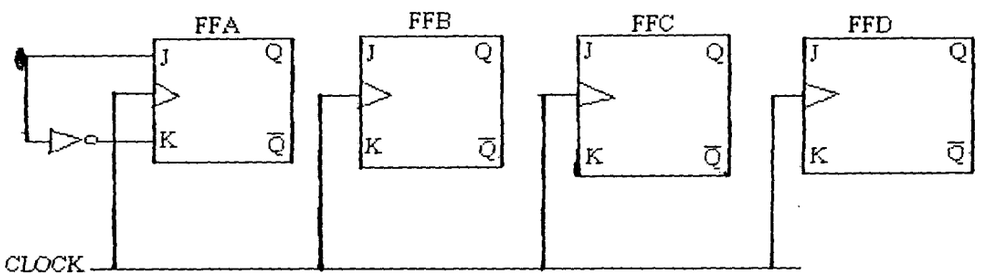


Fig 2.6(a): Four- Stage Shift Register using JK flip-flops connected as D-type

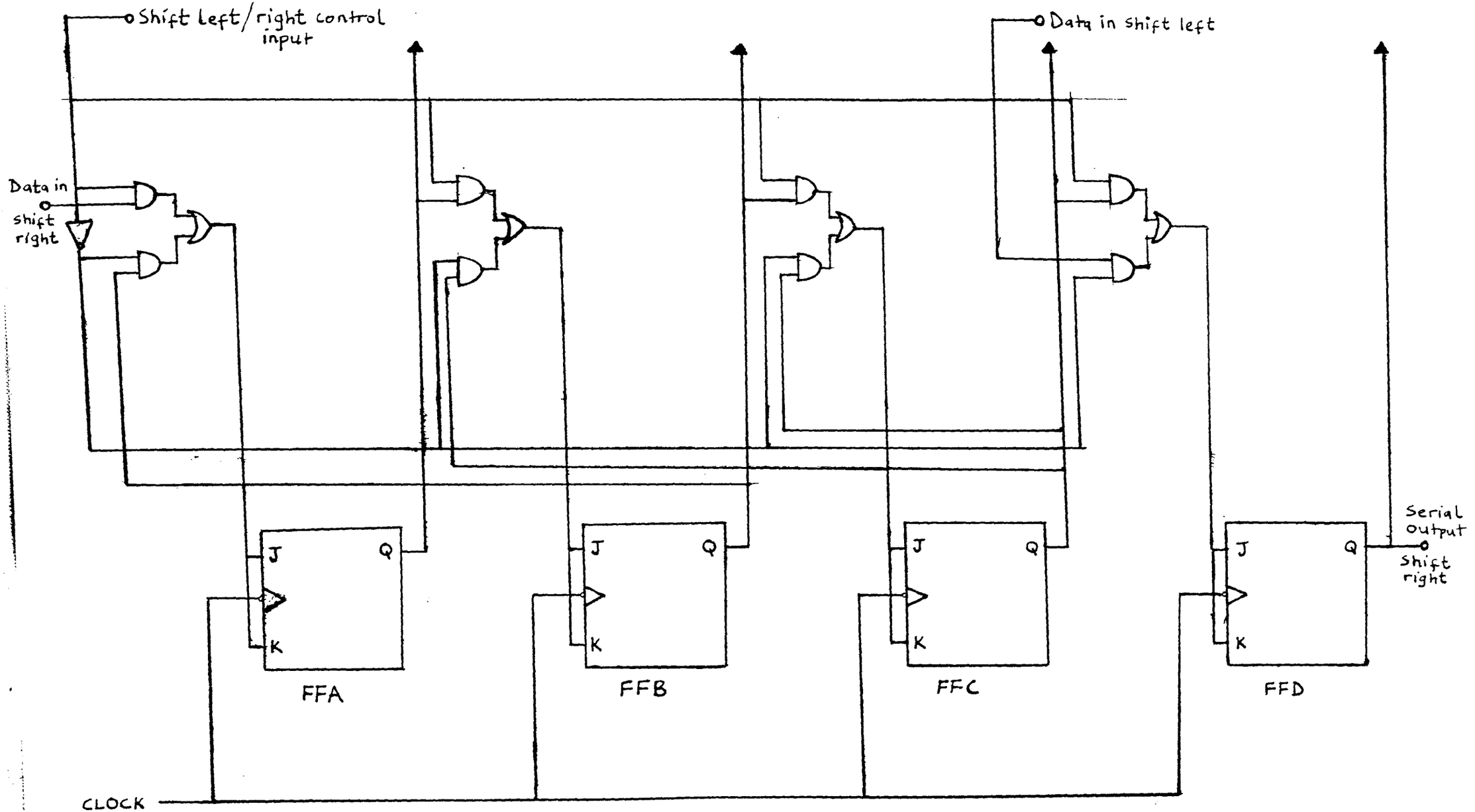
CLOCK PULSE	DATA IN	OUTPUT LEVELS			
		A	B	C	D
0	X	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	0	0	1	1	0
4	0	0	0	1	1
5	1	1	0	0	1
6	1	1	1	0	0
7	0	0	1	1	0

Fig. 2.6(b): Truth table showing the effect of the clock on shifting right one of the input bits to the data-in terminal

Assuming that all flip-flop outputs are initially 0 then data presented at the input may be shifted right by the clock pulses. The data on the input line is connected directly to the J input of FFA but to the K input via an inverter. Thus the J and K input of the first flip-flop are complementary. This means that what ever the input on the J input to this stage is gated to the Q output at the end of the clock pulse. The same effect must occur at flip-flops B, C and D since the J and K input of these flip-flops are connected directly to the Q and Q^ outputs respectively of the preceding stage.

Thus if you say a logic 1 is applied to J input of flip-flop A it will be moved progressively through to the output of flip-flops B, C & D with successive clock pulses. This can be seen in the truth table of figure 2.6(b) above.

Shift registers can also be configured to shift left by appropriately connecting the output of a stage to the input of the preceding stage and feeding the input data to the J input of the final flip-flop. More commonly a shift-left or shift right facility may be employed with the direction of the shift determined by the logic level on the control input and the connection between stages made via logic gating circuits. A simple arrangement is shown in the figure below.


Shift left/right control input
Data in shift left
Data in
shift right
J
Q
K
FFA
FFB
FFC
FFD
Serial output
Shift right
CLOCK

The control input for shift right, assuming it is logic level 1, allow the top of the AND gates to be enabled and since the control input to the bottom row of AND gates is inverted before connection, this gates are disabled. Thus the gating circuit allows shift right data input via the OR gates to be applied to the flip-flop J terminal and after clocking at its output Q terminal, starting at FFA.

Assuming logic 0 on the control input then the top row of AND gates is disabled and the bottom row enabled. Thus a shift-left data input may be applied, via the OR gate, to the input of final flip-flop (FFD) after clocking at its output Q terminal. This output is now connected via the logic gate network to the J input of FFC ready for the next clock pulse. Again the flip-flops shown are JK and it is assumed that Data transfer occurs on the negative edge of the clock pulse.

Shift registers have many practical applications including that of a temporary storage element or buffer stage. This is especially useful in those computer applications where the processor with its high-speed operation may have to deal with slower peripheral devices. In the case of output data transfer from the processor to a peripheral device, the buffer register may store the output data, allowing the processor to proceed with other task while waiting for the peripheral device to accept the data. Since most peripherals deal with serial data (i.e. data clocked out one bit at a time) while the processor deals with parallel data (all bit in the data word shifted at the same instant), there is a need for a shift register that can handle parallel data. For data transfer from processor to peripheral devices, the register would be parallel loaded and serially read out. This type of register is a parallel-in, serial-out device, frequently reduced to PISO. For data transfer from peripherals to processor, the information is fed in serially and read out in parallel. Thus the register is a SIPO or serial-in, parallel out device. Which is the register used in design of this project. Finally register are also available in parallel in, parallel out (PIPO) forms. Thus implying that data are fed in parallel and also read out in parallel.

There are different shift registers in existence today which can be connected to operate in different forms. For this project, a serial-in parallel-out shift register was required. Thus prompting the use of an eight-bit serial-in parallel-out register i.e74LS164. Figure 2.7 below shows 74LS164 logic circuit diagram. The 74LS164 has gated serial inputs A and B allowing

control over the input data, since a low at either or both inputs inhibits entry of new data and reset the flip-flop at the next clock pulse. Both inputs high will set the first flip-flop high at the next clock pulse. Data at the serial inputs may be changed while the clock is high, or low, but must meet the set-up requirements to be entered. Clocking occurs on the low-to--high transition of the clock input. The function table and typical clear, shift and clear sequences are shown in figure 2.8 (a) and 2.8 (b) respectively.

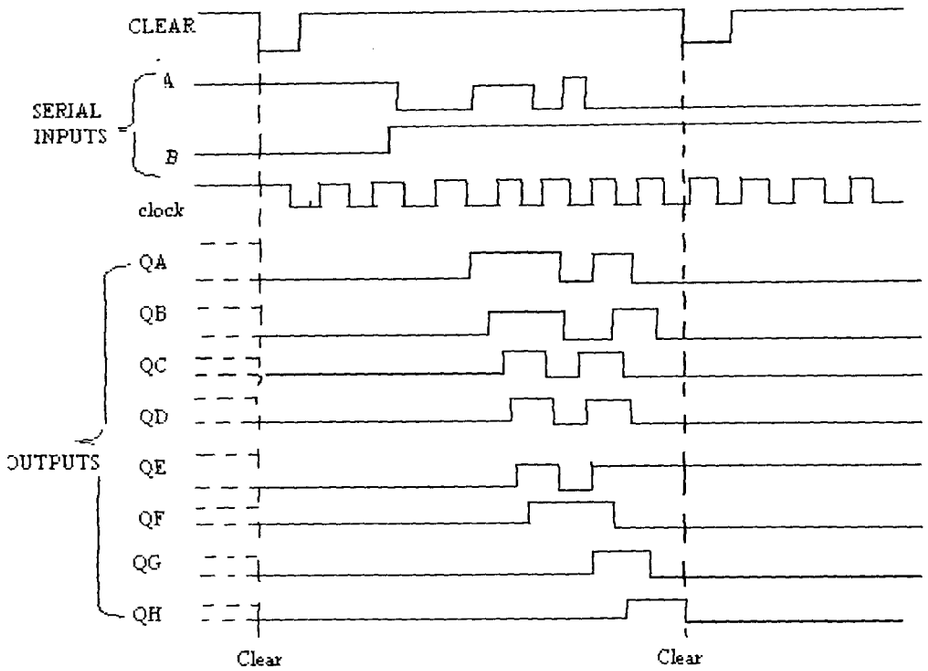


FIG2.8(a): Shows the clear and shift-clear sequences for the 74LS164 eight-bit serial-in, parallel-out register.

	74LS	74	74L
Shift Frequency (MHz)	25	25	6
Serial Data Input	Gated D	Gated D	Gated D
Asynchronous Clear	Low	Low	Low
Shift - Right Mode	Yes	Yes	Yes
Shift - Left Mode	No	No	No
Load	No	No	No
Typical. Total Power (MW)	80	175	30

FIG2.8(b): Specifications of the 74LS164 eighth-bit SIPO shift register.

2.3. DESIGN OF THE DRIVER CIRCUITRY.

Usually, when signals passes through a device there is usually a drop in the signal. Thus, a driver circuit is required to boost the signal at the output in order to compensate for the drop. The driver circuit is designed using a transistor. Figure 2.9 shows the symbol of a NPN transistor.

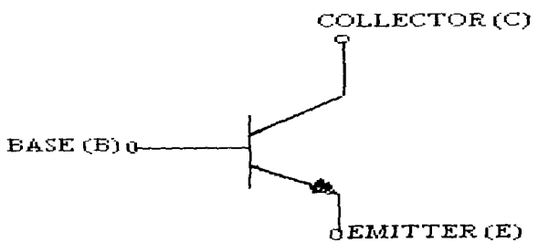


Fig 2.9: Symbol of a NPN transistor.

The transistor as the ability of providing a power gain. Thus making it possible to power a device from a transistor observing that the output signal is greater than the input signal.

For this project the driver circuitry consisted of 35 1N4001 diodes, 35 transistor (BC338), and 70 resistors.

Each driver stage consists of 2 diodes, 1 NPN transistor and 2 resistors of 10KΩ and 100Ω. Each driver stage is connected to just one character or letter e.g. letter F. Thus, since we have 35 characters in all, then, we have 70 diodes, 35 N-P-N transistors and 70 resistors in all.

The driver circuits were applied to the output of the registers via a diode each for the sequential and group modes to boost or drive the signals from the shift registers to the light emitting diodes.

2.4. INTERNAL DESCRIPTION OF THE TOGGLING UNIT (JK FLIP-FLOP 74LS73).

Toggling was used to change the display modes from either sequential to group mode or group to sequential mode by the use of JK flip-flop (74LS73) which is a sequential logic circuit.

Logic circuits can be classified into the combinational logic circuit, which are composed of gates. And the sequential logic circuit which includes devices called flip-flops. Flip-flops are inter-connected to form sequential logic circuits for data storage, timing, counting and

sequencing. Flip-flops have an extremely valuable memory characteristic i.e. a flip-flop will remember its output even after the input are removed. A logic gate however will not remember its output state after the inputs are removed.

There are different types of flip-flops e.g. D flip-flop (data flip-flop), R-S flip-flop (reset-set flip-flop),JK flip-flop e.t.c. These flip-flops have two inputs i.e. data input and clock input. Flip-flops usually have complementary outputs Q and Q (i.e. opposite of Q). The Q output is the normal output while the Q output is called the complementary or inverted output of the flip-flop. The > on the clock input of the D logic symbol denotes that this flip-flop transfers data from input to output on the positive going edge (↑) of the clock pulse (i.e. leading edge).

The figure below shows a logic symbol for a D flip-flop.

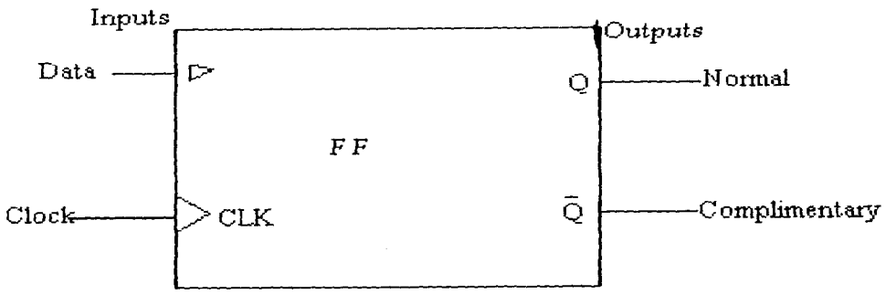


Fig.2.10(a): Logic symbol for D flip-flop.

MODE OF OPERATION	INPUTS		OUTPUTS	
	D	CLK	Q	Q
SET	1	↑	1	0
RESET	0	↑	0	1
HOLD	X	No clock pulse	Same as before	

0 = LOW 1 = HIGH

X = IRRELEVANT ↑ = LOW-to-HIGH transition of clock pulse.

Fig.2.10(b): Mode truth table for D flip-flop.

The modes of operation for the flip-flop are shown in the left column of the table in figure 2.10(b) above. To set the flip-flop means to load logic 1 into normal Q output. From the first line of the truth table in figure 2.10 (b), we can see that placing a logic 1 at the D input and

pulsing the clock (CK) input causes output Q to be set to logic 1.The second line shows the flip-flop being reset. The reset means to clear the Q output to logic 0.To hold means to store the output data. When the flip-flop is in the hold mode, changes in logic state at the data input will cause no change in the output. The hold condition therefore illustrates the memory characteristics of the D flip-flop.

The JK flip- flop is the most widely used in sequential logic circuit owing to its adaptability. The JK flip-flop has two data inputs labelled J and K plus a clock input (CK). The JK flip-flop also has the customary Q (normal) and Q^ (complementary) outputs. Figure 2.11(a) and 2.11(b) below shows the logic symbol and the mode truth table for JK flip-flop. Figure2.11(c) shows the internal construction of JK flip-flop using AND gates and SR flip-flop.

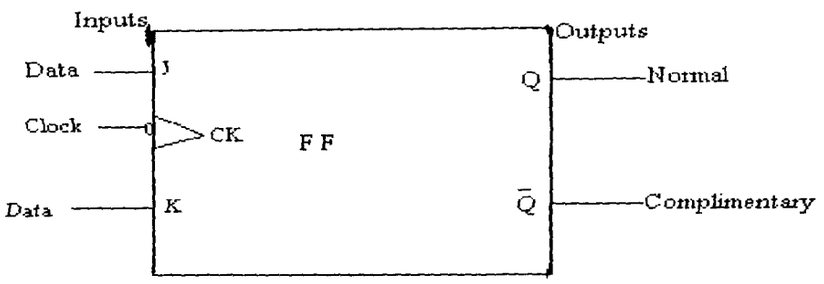


FIG 2.11(a): Logic symbol for JK flip-flop.

Mode of operation	Inputs			Outputs	
	J	K	CLK	Q	Q
Toggle	1	1	↓	Opposite state	
Set	1	0	↓	1	0
Reset	0	1	↓	0	1
Hold	0	0	↓	No change	

0 = LOW 1 = HIGH ↓ = HIGH- to-LOW transition of clock pulse.

FIG 2.11(b): Mode truth table for JK flip- flop.

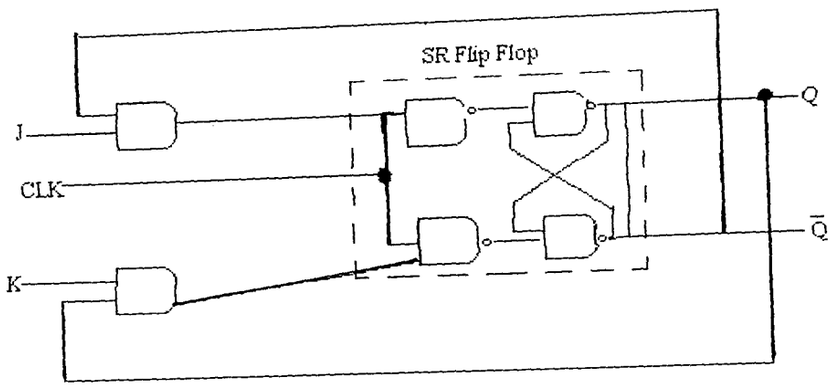


FIG 2.11(c): Internal construction of JK flip-flop using AND gates and SR flip-flop

A JK flip-flop has four modes of operation, which can be described from figure 2.11(b) above. The toggle mode of operation means that on each successive clock pulse, the output will change to their opposite logic states. In the toggle mode, output Q of a JK flip-flop will go high-low-high-low e.t.c on repeated clock pulses.

The truth table in figure2.11 (b) shows that the JK flip-flop will toggle when both data inputs J and K are high providing a clock pulse arrives at the CK input. The actual toggling action takes place when the clock pulse changes from high to low as shown by the arrow (↓) in the truth table.

The JK flip-flop is in the set mode when data inputs J = 1 and K=0.The second line of the truth table in figure (b) shows that a high-to-low transition of the clock pulse then sets Q to logic 1.The reset mode (clearing Q to logic 0)is the third line of the truth table. The last line of the truth table in figure (b) illustrates the hold mode (or do nothing mode) of the JK flip-flop. When both data inputs (J and K) are low, a clock pulse at the CK input will have no effect on the data inputs.

Flip-flops can be classed as either edge triggered or level triggered devices. The JK flip-flop is a negative-edge-triggered flip-flop. This is shown both in the truth and on the logic symbol in figure (a) above. The bubble at the CK input of the JK flip-flop logic symbol implies that it takes a low signalto activate the clock. Because the JK flip-flop is edge triggered it actually takes a H-to-L (HIGH-to-LOW) transition (negative going) of the clock pulse to trigger the flip-flop.

Figure 2.12 shows the Dual JK Edge Triggered flip-flop (74LS73) used in this project.

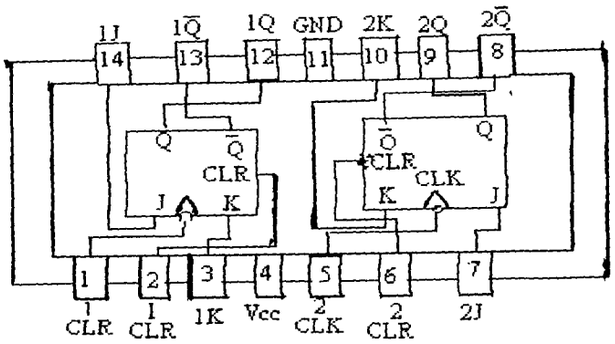


Fig.2.12:Dual JK flip-flop (74LS73).

2.5. DESIGN OF THE DISPLAY UNIT

(CONSISTING OF LIGHT EMITTING DIODES).

The display unit consists if a 36-inch by 6-inch plastic frame and wooden frame used to cover it. Holes were bored (drilled) on the frame, with the diameter of each hole the same as the diameter of the light emitting diodes used.

Then for each of the characters, the LEDs' were arranged to form each of the letters for all the 35 characters or letters i.e. FEDERAL UNIVERSITY OF TECHNOLOGY MINNA.

CHAPTER 3

CONSTRUCTION,TESTING AND RESULTS.

On completion of the design of this project, components required for the construction were purchased and assembled together. The constructions of the different stages were carried out as shown below;

3.1 Block diagram of the system.

3.2 Circuit diagram of the system.

3.3 Display unit layout construction.

3.4 Construction of +6V D.C regulated power supply unit.

3.5 Construction of square wave generator (astable multivibrator).

3.6 Connection of shift registers (74LS164) for both sequential and group modes.

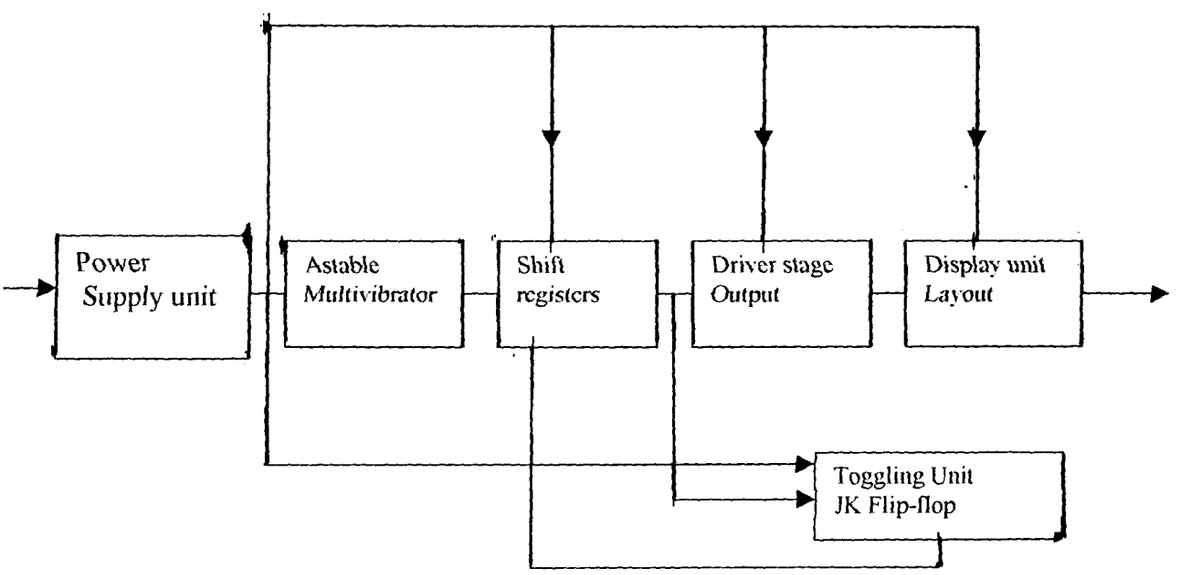
3.7 Construction of the toggling using the JK flip-flop (74LS73).

3.8 Connection of driver output to the display unit using diodes (1N4001) and transistor (BC338)

3.9 Testing of the output of each stage and their results i.e. power supply unit, output of astable multivibrator, output of shift registers (74LS164) and drivers, and the output of the toggling unit.

3.10 Connection of the sub-systems and coupling of the project modules.

3.1 BLOCK DIAGRAM OF THE SYSTEM.



3.2 CIRCUIT DIAGRAM OF THE SYSTEM.

(See attached sheet).

3.3 DISPLAY UNIT LAYOUT CONSTRUCTION.

The display unit layout was constructed making use of 36 inches by 6 inches plastic board. The board was first inscribed with a pencil, which was used to carefully spell out the "FEDERAL UNIVERSITY OF TECHNOLOGY MINNA" making use of 5 by 7 dot matrix arrangement. Holes were carefully drilled on the board making use of a drilling bit of 5mm diameter. A total of 511 holes were drilled for all the characters. The light emitting diodes (LEDs) were later inserted and glued firmly into the holes. Then, all the common anodes of each of the light emitting diodes were connected together using flexible wires and then soldered to the male connector, which was also connected to the +5Volts D.C supply through a 100Ω current limiting resistor. After that the cathodes of each of the LEDS were also connected together. Thus, all LEDs were connected in parallel with each of the anodes and cathodes of each LED connected together.

Then, each of the common cathodes for each character was connected to a flexible wire and wires were drawn out from the common cathode of each character and then soldered to the male connector.

The LEDS were trouble-shooted to observe them light and hence any damaged LED was replaced and the LEDS trouble-shooted again.

3.4 CONSTRUCTION OF +6VOLTS D.C REGULATED POWER SUPPLY UNIT.

The construction of the +6V D.C regulated power supply unit was carried in two phases. The first phase was the construction of the prototype built on a breadboard, which makes it easier to effect any changes or modification. The second phase involves the implementation of the connections made on the breadboard to a vero-board.

The power supply unit consists of the transformation, rectification, voltage regulation, and finally a power transistor.

In the first phase on a breadboard, a point was chosen as the supply (V+) and another point was chosen as ground. Thus, on the breadboard a step-down transformer of rating

15Volts, 2Amps was to the V_{cc} and ground respectively on the bread-board. A properly grounded bridge rectifier was later connected to Vcc on the breadboard. The output of the bridge rectifier was then connected to a filtering capacitor of rating 6800μF/50Volts,with its other end grounded on the breadboard. A positive voltage regulator (7806) with its middle pin properly grounded was connected to the output of the filtering capacitor and the output of the voltage regulator was connected to the base of the power transistor (2N3055). The collector leg of the power transistor (2N3055) was connected to the output of the filter capacitor and a 1KΩ resistor was later connected to the emitter of the 2N3055 transistor and finally grounded on the bread-board. An output of 5.3Volts was tapped at the emitter. These connections were then checked, hence, the power supply unit was powered by an alternating current (a/c) source to know if it met the design specifications.

In the second phase, the components were carefully removed from the breadboard and soldered onto the vero-board.

The transformer was connected to the mains power supply after being screwed on the vero-board. The output of the transformer was connected using flexible wires to the rectification stage.

The rectifier used was the bridge rectifier consisting of four 1N5401 diodes as shown in the circuit diagram. The input of the rectifier was connected to the output of the transformer while the output of the rectifier was connected to a 6800μF filtering capacitor. The output of the filtering capacitor was connected to a positive voltage regulator (7806) to regulate its output voltage to 6Volts.The input pin of the voltage regulator was connected to the output of the filter capacitor, while its middle pin was grounded and the output pin was connected to the base of the power transistor (2N3055). The collector of the power transistor was connected to the output of the filter capacitor while the emitter was connected to ground through a 1KΩ resistor. This was used to stabilize the output voltage.

The output was tapped at the emitter of the 2N3055 transistor and the output positive voltage from the emitter of the power transistor was connected to the V+ inputs of all the other components used.

It must however be noted that all the connections done above were done using flexible wires, soldering irons and soldering lead. A lead sucker was often used in case of any error in soldering. All soldering were done as accurate as possible so as to avoid bridging or short-circuiting of components.

3.5 CONSTRUCTION OF SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

The construction was carried out in two stages similar to the construction of the +6Volts D.C regulated power supply. The two stages were first a prototype on a bread-board, which was later transferred to a vero-board.

On the vero-board, the square wave generator was constructed using a 555 timer connected in its astable mode.

The 555 timer was soldered on the vero-board with its pin connected as follows;

Pin 1 was connected to ground, pin 2 was connected to pin 6 and then to ground through a 100μF timing capacitor .Pin 5 was connected to ground through a 0.1μF capacitor. This was done in order to filter out spikes.

Pin 4 and Pin 8 were connected to the supply voltage +5Volts from the power supply unit. The supply voltage was connected to pin 7 through a KΩ resistor while Pin 7 was connected to Pin 2 and 6 through a 10KΩ variable resistor. The output of the 555 timer i.e. from pin 3 was now connected to the clock input of the shift registers (74LS164) for both the sequential and group modes. The soldering was done as neat as possible to avoid short circuiting on the vero-board which could result in errors in the clock pulses.

3.6 CONNECTION OF THE SHIFT REGISTERS (74LS164) FOR BOTH SEQUENTIAL AND GROUP MODES.

The connections of the shift registers for both sequential and group modes were done both on the breadboard and veroboard as stated in other stages. A total of 8 shift registers were used for both sequential and group modes. The first 6 shift registers were used for the sequential modes while the other 2 shift registers were used for the group mode display.

Integrated circuits (I.C) sockets were soldered on the vero-board, then the shift registers were fixed into the sockets. The shift register 74LS164 as earlier explained has fourteen pins and the pins were connected as follows;

Pins 1 and 2 of the first shift register for both the sequential and group modes, which are the serial inputs of the device were connected high to the positive supply voltage from the power supply unit.

Pin 8 which is the clock input of all the shift registers were all connected to the output pin 3 of the 555timers A and B for both the sequential and group modes respectively.

The reset pins i.e. pin 9 of the six shift registers used for the sequential display were connected to the Q output of the JK flip-flop through an inverting buffer. While the reset pins of the two shift register used for the group mode display were connected to the Q^ output of the JK flip-flop through an inverting buffer transistor. Pin 14 of all the shift registers for both sequential and group modes were connected to the supply positive voltage from the power supply unit.

The output pin i.e. pins 3,4,5,6,10,11,12 and 13 of the first shift register for the sequential mode were connected to the LEDS representing each letter through a driver circuit consisting of transistor, diode and resistor for each output respectively. The last output pin i.e. pin 13 of the first shift register was connected to the serial input pins i.e. pins 1 and 2 of the next shift register i.e. the last output of each preceding shift register was connected to the serial inputs (pins 1 and 2) of the next shift register for both the sequential and group mode display. For the group mode display, the anodes of the diodes connecting different letters were connected together to form a word e.g. FEDERAL. The shift registers' pin 7 was all connected to ground.

Despiking capacitors of value 100nF were connected to the Vcc of the shift registers and ground. These capacitors were connected as close as possible to the shift registers. The capacitors help to remove spikes from the inputs of the shift registers, which could cause errors at the output of such shift registers. Such errors are when two letters come on at the same time in the sequential mode instead of coming on one after the other.

Also, for the group modes pins 4,6 and 11 were used to act as delay between one word and another and a whole shift register was connected in order to produce a delay that can

be noticeable. The same was done for the sequential mode, although, a pin was left after each word came on sequentially and a shift register which was the last was used to cause a noticeable delay.

3.7 CONSTRUCTION OF THE TOGGLING UNIT USING THE JK FLIP-FLOP (74LS73)

The construction of the toggling unit was carried out in two phases, as described earlier on for other stages i.e. the first phase was done on the breadboard and then, it was transferred to the vero-board.

A dual JK negative- edge triggered flip-flop was used with only one of the JK flip-flops actually used. The JK flip-flop (74LS73) was mounted on the veroboard through an I.C socket, which has already been soldered onto the veroboard.

The J and K inputs i.e. pins 14 and 3 were connected high to the positive supply voltage (this is because the flip-flop was connected in the toggle mode). The clear pin i.e. pin2 which is inverted was connected high to the positive supply voltage, pin 11 was grounded. All the connections above were done using flexible wires, soldering iron, soldering lead and a lead sucker.

For clocking of the JK flip-flop, the clock pin i.e. pin1 of the JK flip-flop was connected to last output of the sixth shift register used for the sequential mode display. The last output of the second shift register used for the group mode display was connected to clock input (pin 1) of the JK flip-flop. Both connections (sequential and group modes) to the JK flip-flop clock input were connected through two diodes and an inverting buffer transistor. The diodes were used as protective devices for the shift registers i.e. to protect the shift registers from sinking current when not active. This means that the two diodes act as OR gates such that only one can sink current at a particular time.

The Inverting buffer transistor was as a result of the inversion of the clock input of the JK flip-flop.

The outputs of the JK flip-flop i.e. Q output (pin 12) and Q^ output (pin 13) were connected to the reset pins (pin 9) of the six shift registers for the sequential mode display and also to the reset pins (pin 9) of the two shift registers for the group mode display. This was done through

an inverting buffer for each mode respectively. The inverting buffer at the Q and Q^ outputs of the JK flip-flop helps it to source current which the JK flip-flop cannot source itself. Thus, the inverting buffer reduces the load on the JK flip-flop.

3.8 CONNECTION OF THE DRIVER OUTPUTS TO THE DISPLAY UNIT USING DIODES (1N4001) AND TRANSISTOR (BC338).

As explained in the previous chapter, the driver stage was used to boost the output signals from the shift registers i.e. to restore voltages to proper levels. The output signals were meant to power on the LEDS. These drivers were connected using transistors (BC338), diodes (1N4001) and resistors (10KΩ and 100Ω).

Each output from the shift registers (74LS164) was connected to the base of the transistor through a diode (1N4001). A base resistance (R_b) of 10KΩ was then connected from the cathode of the diode (1N4001) to the base of the transistor. The transistors were connected in the common-emitter mode; thus, the output was tapped from the collector in order to ensure appropriate voltage gains. The emitter of the transistor BC338 was grounded.

The LEDS were connected in parallel to form different characters with their common cathodes connected to the collector of the transistor BC338 while their anodes were connected to the positive supply voltage through an 100Ω current limiting resistor for each character.

Each driver stage consisting of a transistor, diode, and resistors (10KΩ and 100Ω) was used for a particular character. Each driver was connected to the output of the shift register (74LS164) through two diodes i.e. diodes 1and 2 (as shown in the circuit diagram). Each diode was used for the sequential and group mode displays both diodes act as OR gates. That is, only one can conduct at a time. For the group mode display, the set of diodes used for a particular word were connected together using flexible wires, i.e. their anodes were connected together and then connected to the shift register output used for that particular word or group.

The display unit, as explained earlier on, was made up of a plastic frame consisting of LEDS used for the display. The LEDs were connected in common anode mode, then, all the anodes were connected to the positive supply voltage V+ from power supply unit through a current limiting resistor of 100Ω. Then, on the other hand, flexible cables were soldered to the

cathodes of each character, which were connected to the collectors of each transistor or driver used for a particular letter.

The connections were done by connecting all the wires drawn from the common cathodes of each character to the two, 25pin male connectors. Although, we had just 35 characters, so, we did not use all the pin connectors.

Also, the connection from the driver output to the common cathode of each of the characters or letters was done by connecting the flexible wires from the driver to two, 25 pin female connectors. Thus, through these male and female connectors, the display unit can be connected to the driver output.

3.9 TESTING OF THE OUTPUT OF EACH STAGE AND THEIR RESULTS.

On completion of the construction, the various stages were initially tested for continuity using a digital multimeter to ensure that there was no short or open circuit.

In testing of the project, the different modules were tested one after the other in the following order:

i. Output of the power supply unit.
ii. Output of the astable multivibrator.
iii. Output of the shift register (74LS164) and driver stage
iv. Output of the toggling unit.

3.9.1 OUTPUT OF THE POWER SUPPLY UNIT:

The output of the +6 volt regulated power supply unit was tested using a digital multimeter. The output of the transformer was tested first. The output of transformer was expected to be 15 volts and this was correct when the output of the transformer was tested using a digital multimeter.

Next, the output of the 7806 positive voltage regulator was tested. This was done by testing the +6 D.C Volts from the output of the voltage regulator using a digital multimeter. It was tested by placing the positive probe of the multimeter on the output terminal and the negative probe connected to the common or ground of the voltage regulator (i.e the middle pin).

Furthermore, checking its Vcc to ground tested the 2N3055-power transistor. The expected voltage between Vcc and ground was to be 21.2 Volts and when it was tested with a multimeter, a very close value of 20Volts was obtained and this result was satisfactory.
To test the Vcc of the 2N3055-power transistor to ground, place the positive probe at V_{cc} and the negative probe to ground.

Next, the emitter was also tested to ground since we tapped our output from the emitter, it was necessary to test this output which was used to power other transistor transistor logic (TTL) components. The emitter of the 2N3055 was tested using the digital multimeter by placing the positive probe at the emitter and the negative probe to ground.

Thus when all the above tests were satisfactory for the power supply stage, we moved to the testing of the next stage.

3.9.2 OUTPUT OF THE SQUARE:WAVE GENERATOR ASTABLE (MULTIVIBRATOR)

The square wave generator (astable multivibrator) stage was tested by connecting a light emitting diode at the output of the astable multivibrator. This was done by connecting a LED between pin 3 of the 555 timer and ground. When this was done, the LED was observed to light up at certain time intervals (T = 1.5seconds). This result was satisfactory. This time interval with which the LED came up can be reduced or increased by varying the resistance of the variable resistor.

3.9.3 OUTPUT OF THE SHIFT REGISTERS (74LS164) AND DRIVER STAGE:

The serial in / parallel out shift registers (74LS164) was tested by what is known by functional tests. These functional tests assured that these devices under test would perform its logical operation in accordance with its truth table.
The input to the shift registers was tested to make sure it was +5Volts D.C. This was done by placing the positive probe of the multimeter at pin 14(V_{cc}) and the negative probe to pin 7 (ground) and the results obtained were alright.
The outputs of the shift register were tested technically. Since the shift registers were mounted on I.C sockets, after placing each register in its socket, 8 LEDS were connected to the 8 outputs

of the shift register. Thus, since all the LEDS have all been connected. when the board was powered, each of the LEDS lighted up sequentially i.e. one after the other. Thus, this was used to verify if the shift registers were all right. If any of the LEDS were not lighting up, then such a shift register would be suspected to be bad and replaced with another one.

The output of the driver stage was tested by connecting it to the display board consisting of the LEDs, through the male and female connectors and then powering the system. Each character would be observed if it lights up or not, and thus, if a character doesn't light up the driver stage for such a character would be trouble-shooted and necessary repairs would be carried out.

3.9.4 OUTPUT OF THE TOGGLING UNIT:

The toggling unit consisting of the JK flip-flop was also tested. The test was done by making sure the two different modes of display(sequential and group modes) were connected to the JK flip-flop through the shift registers. As earlier explained, the last output of the shift registers for each mode of the display was connected to the clock input of the JK flip-flop. The display unit board was observed visually to see if the JK flip-flop will toggle from the sequential mode to the group mode and vice-versa.

Thus, after each stage test, the whole display was coupled together and tested using the display unit layout.

Sometimes, it was possible for a character not to light up, this may be caused by so many reasons. It maybe as a result of the disconnection of the flexible wire connecting the characters to the driver stage or the transistor switching the character being faulty. Thus, we carried out some trouble-shooting in order to detect and solve these problems.

Another problem encountered was that in the sequential mode of display, where each character should light up sequentially (i.e. one after the other), sometimes, two characters may light up at the same time and this was incorrect. Therefore, to solve this problem, a despiking capacitor was connected between V_{cc} and ground of the shift registers (74LS164).

After solving all problems, the whole system was tested and was certified to be in proper order.

3.10 CONNECTION OF THE SUB-SYSTEMS AND COUPLING OF THE PROJECT MODULES.

This stage involves connecting together all the different stages mentioned above so as to observe how the project operate and check for any errors. The power supply unit was connected to the astable multivibrator, shift register (74LS164),driver and the toggling unit (consisting of the JK flip-flop) stages.

Then, all the stages were screwed in a metal casing. Before being screwed in the case, it was protected by an insulator in order to avoid any short-circuiting. The insulation was first placed in the metal casing. The drivers as discussed earlier were connected to the display unit board through the male and female connectors.

A switch was fixed on the metal casing to switch power on and off. The switch was actually connected to the transformer (15Volts, 2Amps).

Thus, the metal casing consists of all the electronic components, which can be connected to the display unit board through the male and female connectors. The electronic components in the metal casing, control the basic functioning of the whole project.

CHAPTER 4

CONCLUSION, RECOMMENDATION AND RESULTS.

CONCLUSION:

In conclusion, this project thesis as explained in details the design and construction of a light sequencer displaying "FEDERAL UNIVERSITY OF TECHNOLOGY MINNA" in two different modes (i.e. the sequential and the group modes).

Furthermore, the aims and objectives of this project were not withstanding the problems encountered. I will also like to mention that the use of sequential logic circuits in design is more appropriate when you consider factors such as cost of production, space, speed, accuracy e.t.c.

Finally, this project has also exposed me to design of electronic circuits. Thus I can categorically say that the job of designing requires a great deal of mental task and then aspect of it.

It was also observed that not all I learnt theoretically is possible in practice. Certain ideas still need to be incorporated.

RECOMMENDATIONS:

The author of this project would like to recommend that further work could be done on the project. That is, this project can be improved upon by using microprocessors, electrically erasable programmable read only memory (EEPROM) chips instead of the shift registers (74LS164) that was used in this project. This will enable many different words and forms of display that is very attractive to the human eye.

I will also recommend a transformer of a higher current rating to be used and also high power light emitting diodes (LEDS) if the project is to be mounted for commercial purposes so that it can function for a very long time.

Furthermore, in the display driver circuits consisting of diodes, transistors and resistors a single IC-8 channel complementary metallic oxide semiconductor (CMOS)/transistor transistor logic (TTL) input driver can be used instead of using so many drivers and transistors.

The IC driver is known as ULN2803 and it has eight output, each of which has a maximum current per output of 500mA.Thus,a minimum of100 LEDS can be connected to a single output. This makes the construction neater and easier to trouble-shoot.

Finally, it is recommended that the university should fund projects like this as it commercially viable and has great potential of becoming a consultancy service that the university can offer to the general public. Also, I would recommend that the Electrical/Computer Engineering Department should assign projects to students that will expose the students to a more practical environment.

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