ACKNOWLEDGEMENT

I start with much gratitude to Almighty Allah, the Beneficent, and the Most Merciful. You gave me the will and showed me the light and gave me the zeal and courage to read and understand.

I wish to acknowledge the tireless efforts of my supervisor Engr. Rumala in guiding me through this project work to its successful completion. I will like to extend my sincere appreciation to my Head of Department Engr. Musa D. Abdullahi for his fatherly advise and guidance.

I also acknowledge my parents support and understanding Alhaji Umaru Ahmed and Hajiya Zainab U. Ahmed who brought me into this world and showed me that "Knowledge is Power". I appreciate that; I can never pay you back.

To my siblings who have been my side at all whether comes rain comes sunshine. I have no one but you. "Blood is thicker than water".

To Ya Manya and Ya Abu, May Allah guide and protect you.

To my guardian Umaru Salihu and his beloved wife Aunty Fati and their wonderful children Tauhida and Fouad I don't know how to thank you, I pray that Allah will reward you all abundantly.

To my friends, Dirji, Mr. Moh, Muhsin, Roxy, Mr. Carl, Mukky, Goga (Ali), Senate President. And to all other friends who I am unable to mention here, I appreciate your friendship and care, I say God bless you.

To Engr, Biggie and Nigga and other cousins who have helped me with prayers. I pray God should also guide you and help you in all your endeavors.

And finally to all my lecturers, the staffs of FUT Minna who in one way or the other have helped me to achieve my life long dream. I say thank you so very much.

ABSTRACT

The project is designed as a Digital Time-Switching device. The aim of this project is to switch ON or OFF a device automatically when a certain preset time is reached. The core of the project is a crystal oscillator which provides an exactly one second pulse or timing for the counter. Also, complimentary metallic oxide semiconductors (CMOS) are the only integrated circuits (ICs) used in the project design in order to make the circuit flexible and for it to consume low power

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CHAPTER ONE

1.0 INTRODUCTION

The project is designed as a digital time-switching device. In which a device is automatically switched ON or OFF (depending or the mode) when a certain present time is reached. The circuit is designed in such a way that the preset time goes or counts down to zero. And when zero is reached, the output is triggered. The circuit incorporates a crystal oscillator which produces an exactly one second pulse or timing for the counter. Also, all integrated circuits ICS are complimentary metallic oxide semiconductor (CMOS), which makes the circuit very flexible and to have low power consumption.

The circuit is divided into six units. The 1Hz frequency generator incorporates a 4060B crystal oscillator the frequency is really 32, 768 Hz. But the same integrated circuit has 14 dividers in-built that divide the 32,768 Hz frequency 14 times for a result of 2Hz. An additional divider (4013B in toggle mode) is added to have a frequency of 1H2 (1-second pulse). This pulse is used for timing the counters.

Using two switches for second and minutes the control unit is then used for presetting a particular number into the counters. Control latch is used for digitally switching to preset mode in which a number is preset into the timer or enable mode in which the number decrement for every one second timing.

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The counters are down type. They decrement for everyone second pulse input. They are four in all two for minute's count, and the other two for second.

The display unit holds a 7-segment decoder (4511B) and common cathode 7 segment displays.

The output-load-control latch stores logic 1 where a 0000 condition is reached on the counter or display. At such point the output load is either switched OFF or ON 1 that depending on the mode. The switching is done through a relay circuit.

The timer can be used in a wide range of ways. For instance it can be used for both industrial and domestic purposes. For example, in timing microwave ovens, heating machines, industrial machines, bombs, locks etc.

CHAPTER TWO

2.0   LITERATURE REVIEW

The chambers Twentieth century dictionary defines 'TIME' as

(i)   "The concept arising from the change experienced and observed"

(ii)   Quantity measured by the angle through which the earth turns on its axis"

(iii)   "A moment at which, or stretch of direction in which things happen".

There also goes an important saying the world exist in space and time. Time is a continuum in which events occur, the ability to note a precise point in time enables events to be referenced. As it is, time enables specific events to be referenced, in the same vein time could also be used to note when events occur.

The ability to note time allows for one to create and control an event or events also noting an event in time allows for specific actions or response to a specific event in time.

As the world and man evolved the ability and precision to note time has also evolved from the stone age where man used the Sun and sticks via the suns angle and shadows caused by the stick to note the passage of time; which evolved to the use of Hour Glass; this evolved to the use of clocks, watches and timers of various designs in our present day.

The instruments for reference to Time can be defined in terms of their design as being either analogue or digital in nature.

Instruments and Instruments system's refine, extend or supplement human facilities and abilities to observe, perceive, communication, remember, calculate or reason.

Instruments can either be classified as either Analogue or Digital Instruments. An analogue instrument is one in which the magnitude of the measured quantity is indicated by means of a pointer. In Digital Instruments, the indication is given in the form of numbers, the smallest change in the indicated quantity correspond to change of the digit in the least significant position of numbers.

Analogue Instruments utilize the following effects: magnetic, heating, electronic, electromagnetic induction or chemical effect. Majority of analogue instruments including moving, r ving Iron and electro-dynamic (dynamometer) Instruments utilize magnetic effects. Heating effects are used in either thermocouples instrument. Electromagnetic Induction effects are used in a range of A.C energy of ampere-hour meters.

Analogue meters are those involved in continuously monitoring the magnitude of the signal or measured (quantity to be measured). The moving system of an analogue instruments are acted upon by three forces

(1)   A Deflecting force

(2)   Controlling force

(3)   A damping force

Digital instruments sample the measured, perform evaluation using digital electronics and normally display the measured in

discrete numerals. In general contemporary instruments use either Light Emitting Diodes (LED) or Liquid Crystal Seven Segment Displays (LCD). The major advantage of digital display is that it eliminates parallax errors and reduces human errors associated with interpreting the position of a pointer on an analogue scale.

Most digital instruments have superior accuracy and input characteristics to analogue instruments.

Due to this high accuracy, about 80% of the IC market has been captured by digital IC's, which are mostly utilized in the computer and electronics industry. Digital ICs lend themselves easily to monolithic integration because, as in the cases of computers a large number of identical circuits used. Paul Horowitz describes, digital systems as containing digital ICs circuit whose input and output voltages are limited to two possible levels high or low. This is so because digital circuits are usually binary. Some digital circuits are referred to as switching circuits. Digital ICs include circuits such logic gates, flip-flops, clock chips, calculator chips, microprocessors and memory chips and counters which have been incorporated in this project.

The developments of microelectronics that have occurred in recent years, due to the compatibility of digital ICs has resulted in grater capabilities and improvements in performance without an increase in cost (electronics journal 1980). These attributes ensure that digital instruments will increase their proportion of the market, although they are unlikely to absorb all the market. Though analogue instruments are unlikely to be ousted, while some other hybrid

instruments (digital processing with analogue display) are gaining acceptance.

2.1 PROJECT OBJECTIVES/MOTIVATION:

The objective of this project is to design and construct a Digital Timer, which uses decade counters and decoder drivers for the operation of the timer and output display. The timer and the incorporated logic and memory modules serve to control the turn-off of any device connected to it after a specified time, which has been programmed into the timer.

And the timing is done by the use of a crystal oscillation. That is simply for accuracy.

CHAPTER THREE

3.0 CIRCUIT DESIGN & ANALYSIS

The circuit is all about complimentary metallic oxide semiconductors (CMOS) integrated circuit or logic. It provides numerous design advantages. The advantages include high fan-out, low power consumption, wide voltage range, high compatibility, cheap cost, high availability etc. These merits simply sub cedes any existing demerits. The design is merely designed for simplicity and economic values. However, each integrated circuit is attributed to unique characteristics. The components in use will be carefully examined.

The 4060B is a 14-stage CMOS oscillator/divider integrated circuit. The oscillator can be configured in both RC and crystal mode. But for the leading design crystal mode is suitable. This is because a highly stable frequency of 1Hz (1 second period) is required for an acceptable outcome. The crystal in use is a 32,768Hz type. Such high frequency type is required so that the integrated circuit divides down the frequency fourteen times to 2Hz or 0.5 seconds time period. An addition divide-by-two flip flop (4013B) is used for the final division to 1Hz of 1 second time period. This frequency result is used to trigger the counter stage.

DESIGN AND CONSTRUCTION OF A DIGITAL TIMER

BY

UMAR ABUBAKAR AHMAD
98/7275EE

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING B (ENG) DECREE IN ELECTRICAL AND ELECTRONICS, ENGINEERING
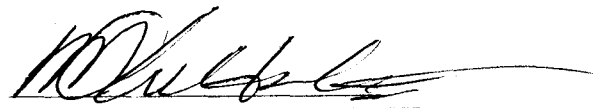
NOVEMBER, 2005

CERTIFICATION

The project has been read and approved as meeting the requirement of the department of Electrical and Electronics Engineering, Federal University of Technology, Minna for the award of Bachelor of Engineering (B. Eng) in Electrical Electronics Engineering.

_____   7/12/05
ENGR. RUMALA   DATE

_____   0/02/06
ENGR. MUSA ABDULLAHI   DATE

_____   _____
EXTERNAL SUPERVISOR   DATE

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DEDICATION

I dedicated this work to my dear parents. To my father Alhaji Umaru Ahmed, for his patience, understanding, his potent advice, simplicity, humor and for helping me to find my way.

To my mother (Mama), Hajiya Zainab U. Ahmed, for raising me to be what and who I am, for her love, her care, her encouragement and her foresight. I respect you and love you.
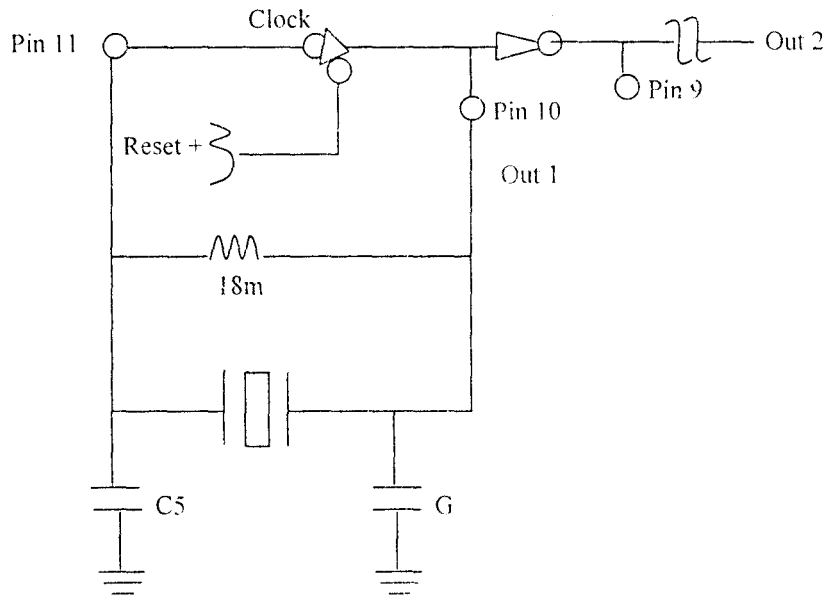
Fig. 3.1   Typical Crystal Oscillator Circuit

The value of C_5 and C_t are 30 and 68 pf respectively. Moreover, the highest division in which the $2H_z$ frequency comes out is Pin 3 of fig. 3.2 below. The output is connected to the additional divided – by – 2 – flip flop.
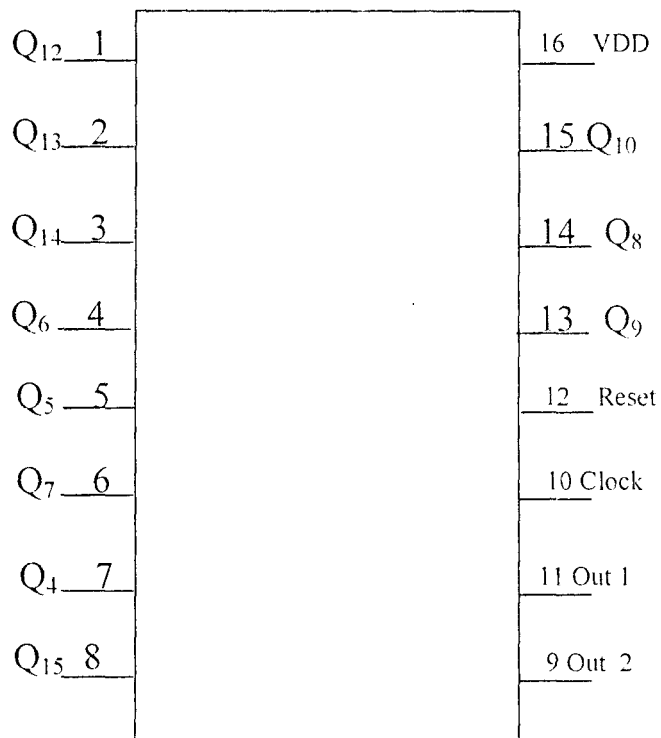

Fig. 3.2   Pin Assignment of 4060B

Fig. 3.3 shows a dual flip flop integrated circuit. This simply means two flip flop in a package. Each flip flop has its own set, REST, Clock, Q, Q and data terminals. Normally each flip-flop I configured as a SR-flip-flop. This is done by grounding the Data and clock inputs.
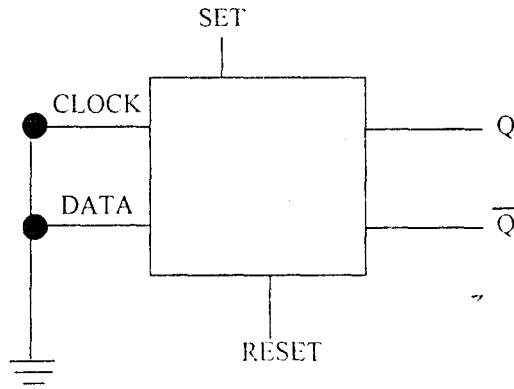

Fig. 3.3   SR – FLIP FLOP CONFIGURATION
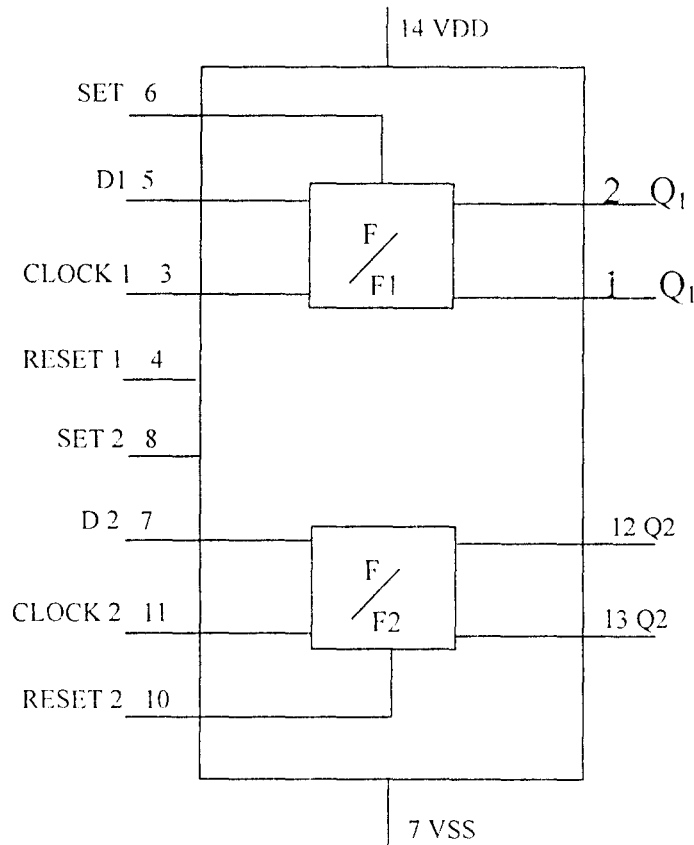
The SET and REST input are active high

Fig. 3.4   FUNCTIONAL DIAGRAM OF 4013B

Fig. 3.6 below shows the function diagram of 4018B. The integrated circuit shown is a quad 2-input AND gate in other words, the package has FOUR AND Gates. Each follows the standard 2 – input AND gate.
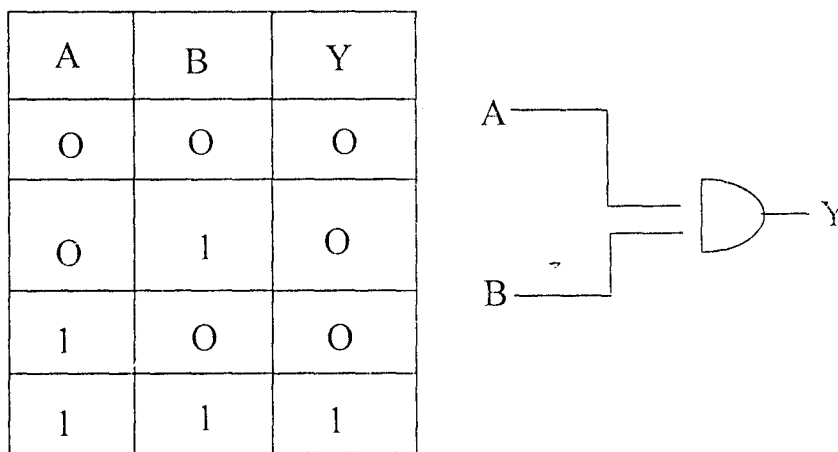
A	B	Y
O	O	O
O	1	O
1	O	O
1	1	1

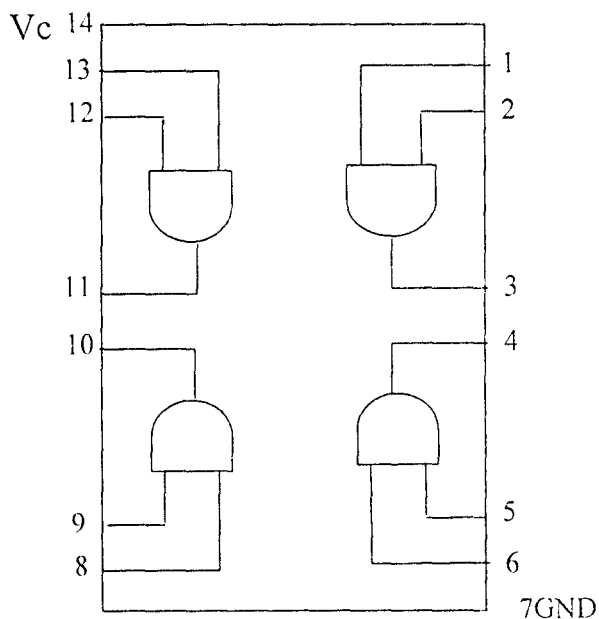**Fig 3.5**   **TRUTH TABLE OF 2 – INPUT AND GATE**

Fig 3.6   **FUNCTIONAL DIAGRAM OF 4018B**

The 4069UB is an integrated circuit package with six NOT gate logical unit. Each operates as an inverter logical device. (see fig 3.7 below).
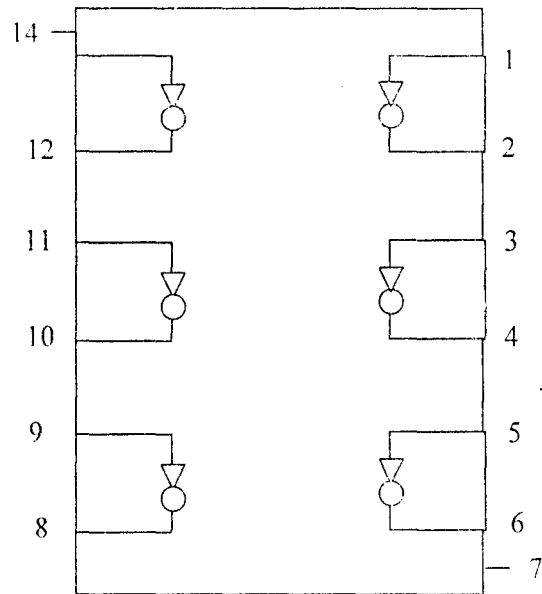

Fig 3.7   FUNCTIONAL DIAGRAM OF 4069UB

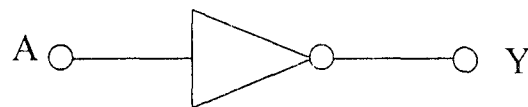| A	Y
1	O
O	1

TRUTH TABLE OF A NOT GATE

Fig 3.8

The 4029B is a presentable up/down filter counter which counts in either binary or decade mode depending on the voltage level applied to at binary/decade input. When binary/decade input is at logic "1" the counter

counts in binary, otherwise it counts in decade. Similarly, the counter count up/down input at logical '1' and vice versa.

A logic '1' preset enable signal allows information at the 'jam' inputs to preset the counter to any state asynchronously within the clock. The counter is advanced one count, at the positive going edge of the clock if the carry in and preset enable inputs are at logic 'O'. Advancement is inhibited when either or both of these two inputs is at logical '1' the carryout signal is normally at logical '1' state and goes to logical 'O' state when the counter reaches It's maximum count in the 'UP' mode or the minimum count in the 'down' mode provided the carry input is at logical 'O' state.

All inputs are protected against static discharge or diode clamps to both VDD and VSS or positive and negative terminals respectively. Fig 3.9 shows the pin assignment for 4029B.

FEATURES OF 4029B

-       Wide supply voltage range 3v to 13v

-       High noise immunity 0.45VDD (typical)

-       Low power TTL compatibility for out of during 74l or 1 during 74LS

-       Parallel jam Inputs

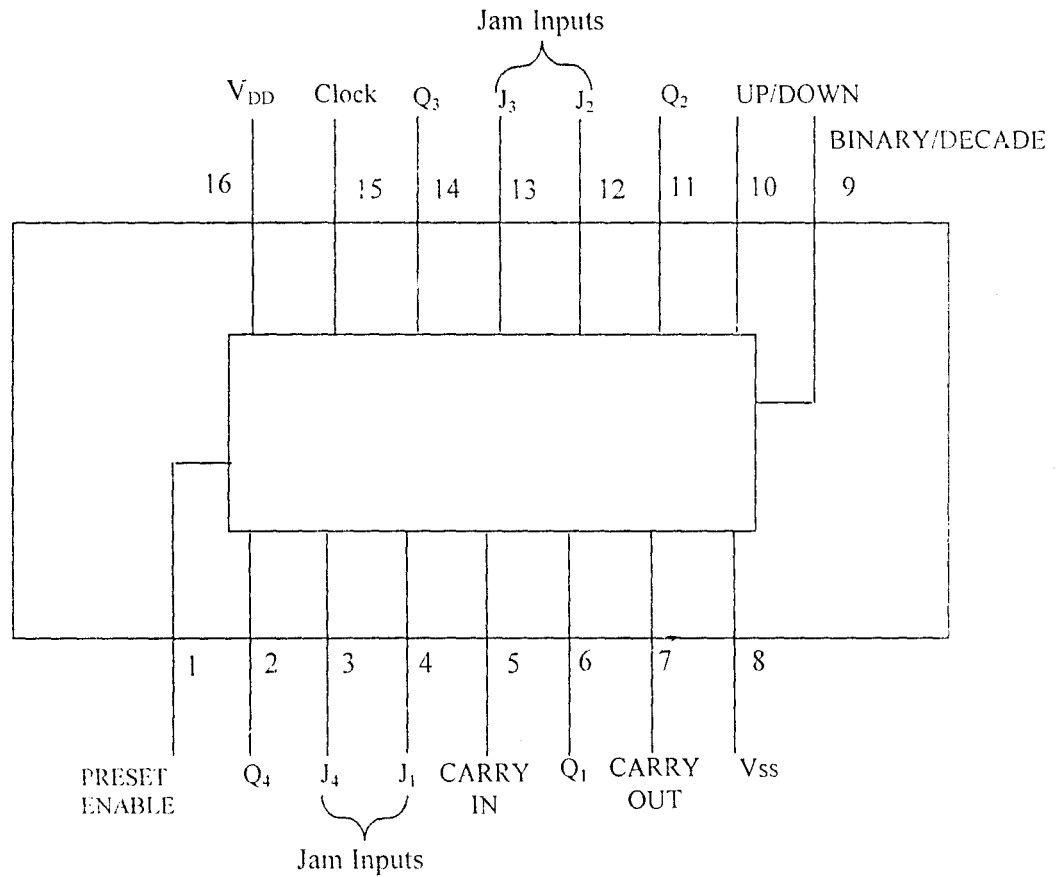-   Binary or BCD decade up/down counting

Fig 3.9   PIN ASSIGNMENTS FOR 4029Bc

The integrated circuit is configured in the serial mode or synchronous set. It provide a faster cascading techniques.

The 4511B is a common BCD-to-7 segment – latch decoder drivers constructed with n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise community features. The integrated circuit has special features, like lamp reset (LT), blinking (BC), and latch enable or strobe inputs are provided to test the display, shut off or intensity modulate it and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplex circuitry is used. The

4511B is supplied in 16 lead hermetic dual-in-line ceramic packages. Fig 3.1.1 shows the function diagram of 4511B.

The features of 4511B includes:-

-   High output sourcing capability of up to 25mA

-   Input latches for BCD code storage

-   Lamp test and blinking capability

-   7 segment outputs blanked for BCD input codes > 1001

-   100% tested for quiescent current at 20V

-   Max – input current of IμA at 18V, overfull package temperature range 100 μA at 18V at 25^{0}C.
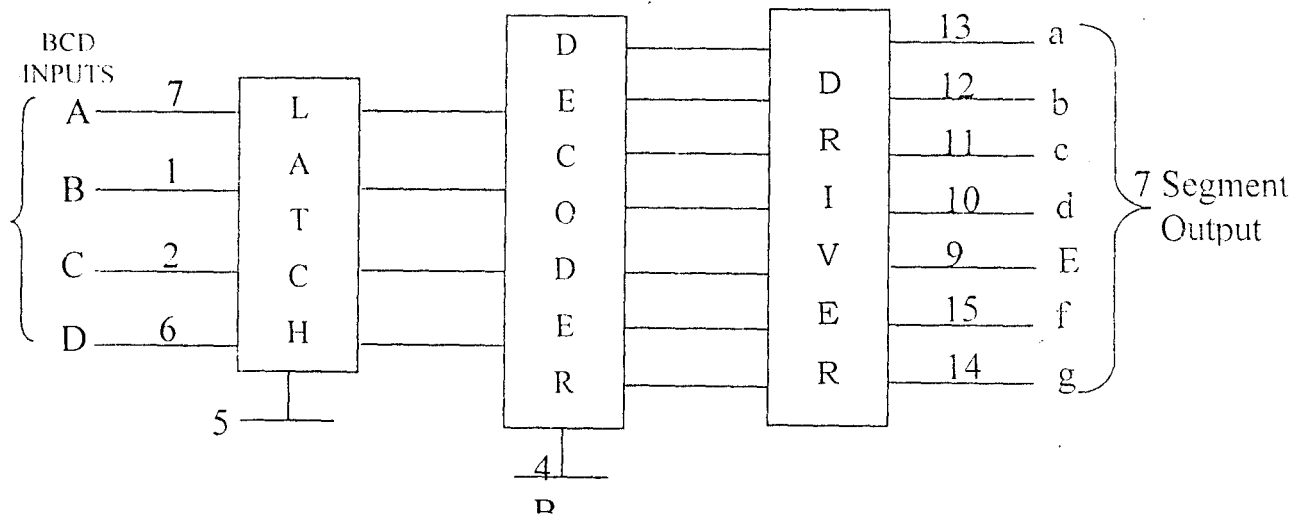
-   5V, 10V and 15V parametric ratings.

Fig 3.1.1   FUNCTIONAL DIAGRAM OF 4511B

NUMBER	CODE	DISPLAY
1	0000	O
2	0001	1
3	0010	2
4	0011	3
5	0100	4
6	0101	5
7	0110	6
8	0111	7
9	1000	8
10	1001	9

CHARACTER DISPLAY WITH CORRESPONDING CODE TABLE

An IC voltage regulator LM 7805 is being used for voltage regulator. It is a three terminal positive regular and available in TO-220/D-PAK package. It has current limiting, thermal shutdown and safe operating area protection. Making it essentially indestructible. If adequate heat sinking is provided, it can deliver over 1A output current.
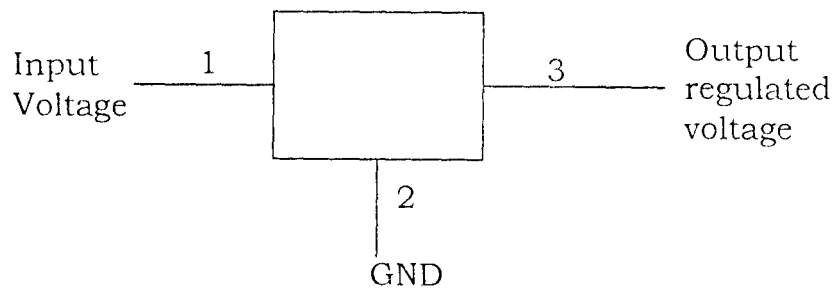
Input Voltage ——1—— [   ] ——3—— Output regulated voltage

2

GND

Fig 3.1.2   BLOCK DIAGRAM OF 7805

The device provides a stable regulated 5volts when connected and regulated.

3.1 POWER SUPPLY STAGE

All stages in the project uses +5V except the transistor stage that controls the relay, which uses a voltage of H2V. The power supply stage is a linear power supply type and involves in step down transformer, filter capacitor, and voltage regulators. The power supply circuit diagram is shown below.
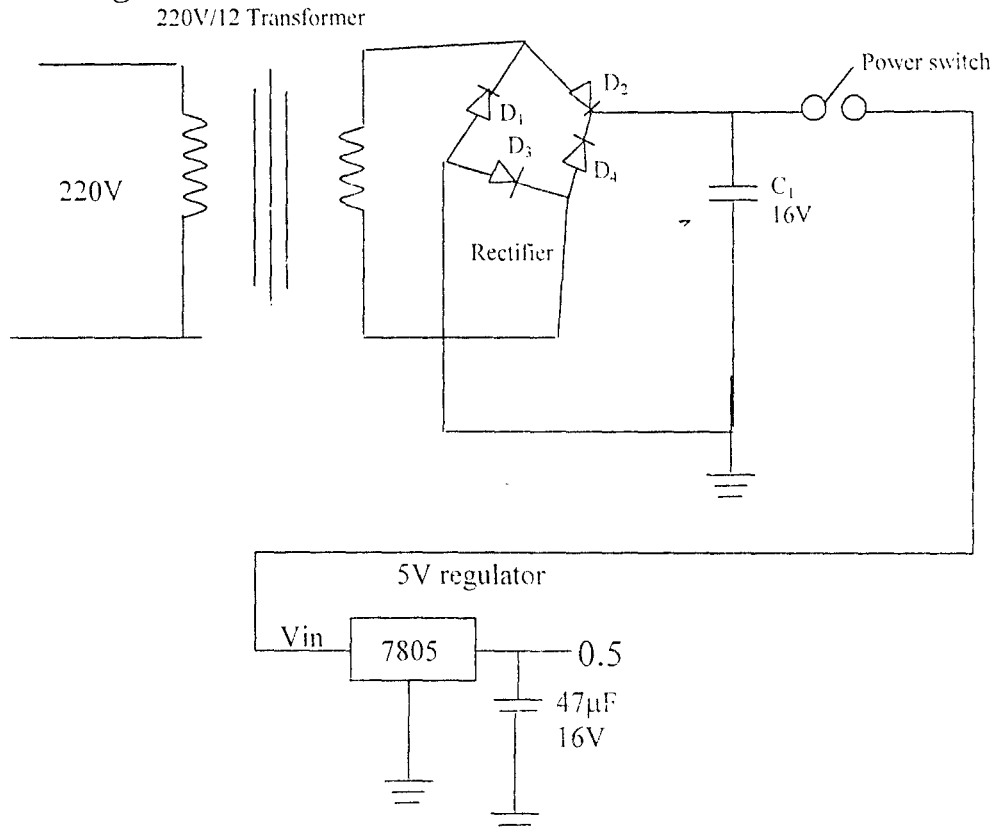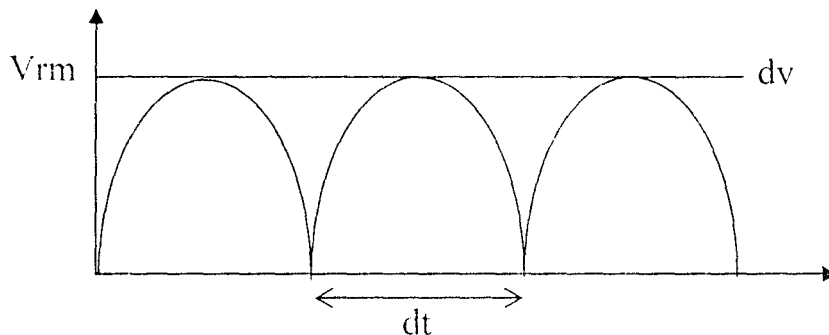

Fig 3.1.3

3.2 POWER SUPPLY CIRCUIT

The rectifier is designed with 4 diodes to form full wave bridge network. C_1 is the filter capacitor and C_t is inversely proportional to the ripple gradient of the power supply. The figure below shows ripple gradient.

Where dv is the ripple voltage for time dt, where dt is a dependent in power supply frequency.

A preferred value of 2200nf was employed for the power supply stage, which is a more conventional value.

3.3   HOW THE CIRCUIT WORKS

THE OSCILLATOR

The main unit is the oscillator. It's designed to generate 1Hz or 1-second frequency output. The corresponding integrated circuits are 4060B and 4013B the output is connected to the counter stage through control logic. As earlier stated, the oscillator is triggered by a 32,768Hz crystal and through internal division the output frequency is 2Hz. This is further divided by 2 through additional flip-flop.

THE CONTROL

The counters are set into a specific count through second and minute buttons. This is done by bridging the normal pulse path into the counter through the button. The counters respond to the forced control. After the setting, the enabling button is activated to start the counting down function of the input count to zero when the input relay is triggered on for the external control.

THE COUNTER UNIT

It holds four counters, which are grouped into two. The minute and second group of counter, the second stage has a maximum of

sixty count. The minutes has a maximum count of ninety-nine. Each group is attributed to two seven-segment display decoders. The decoders are connected to corresponding seven segment displays.

THE OUTPUT STAGE

This unit mainly holds a control relay. It is controlled or triggered ON whenever the count group zero. It is controlled through an output latch, which feed out from each counter as directed. The output latch in connected to a 2SC95 NPN switching transistor. The transistor switching on the relay where a HIGH logical level is given out by Q output of the latch. And the transistor switching off the relay where the Q output is LOW. When such happen, there is a feedback to the counter so that no other count is achieved. A new input can be made into the counter by the early minute and second preset button such that the operation starts all over again.

THE DISPLAY

These sections hold for seven segment display in which the virtual output or information in linked. The responding decade codes at the counter stage are fedout as digital format at the display. The terminal of each segment display is connected in series with a 220Ω current limiting transistor. The provide protection against light current through the segment of the display. And each of the segment display is common cathode type.

CIRCUIT OF A DIGITAL TIMER

Common Cathode
7-segment display
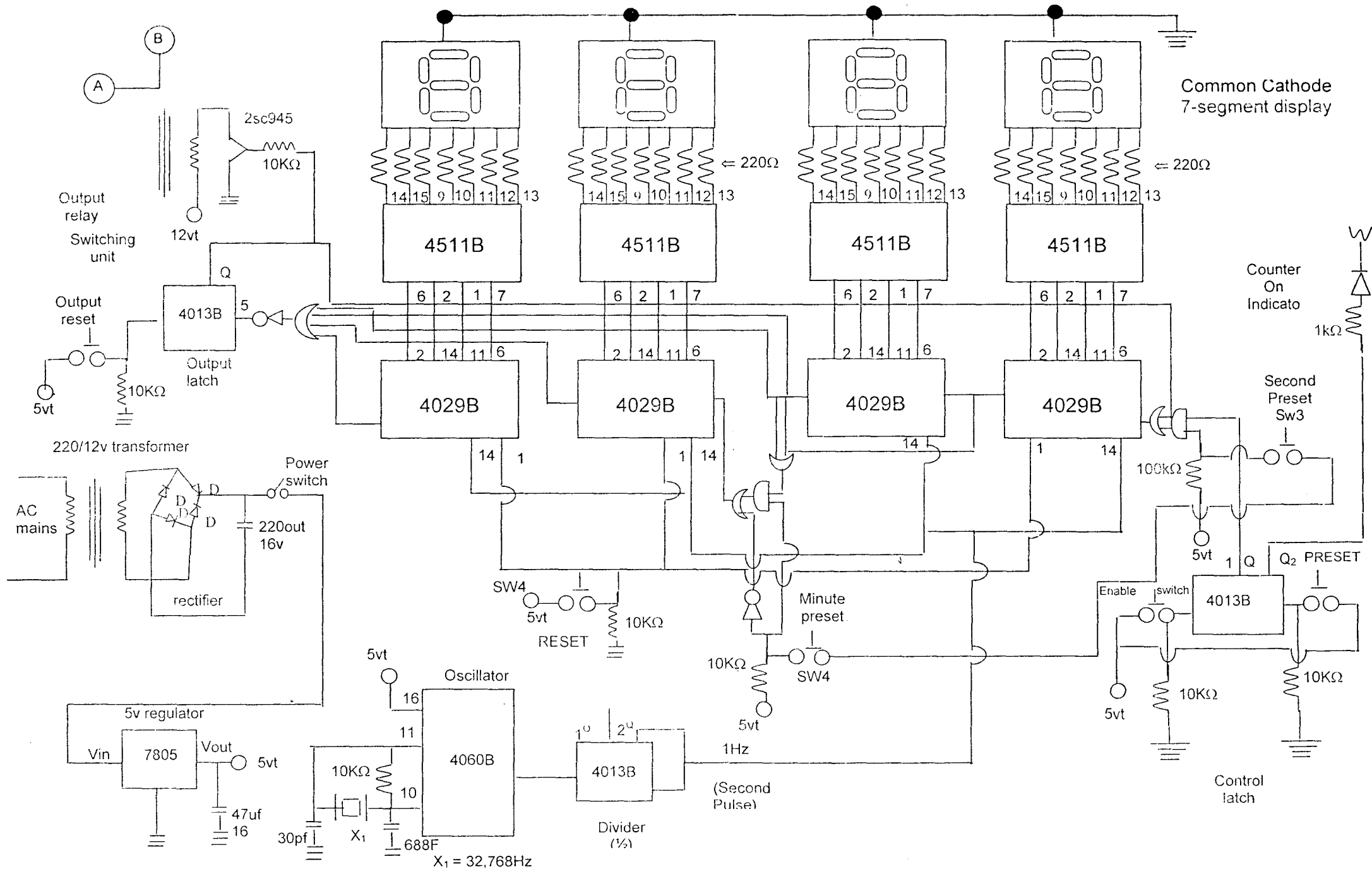
CHAPTER FOUR

4.0 TESTING

The physical realization of this project is very vital. This is where the fantasy of the whole idea needs reality. The designer will see him/her work not just on paper but also as a finished hard ware system.

After carrying out all proper design analysis the project was implemented and tested to ensure its integrity and finally constructed to meet the desired specifications.

The process of testing and implementation involved the use of some equipment stated below:

(i)   BENCH POWER SUPPLY:- This was used to supply voltage to the various stages of the circuits during the breadboard test before the power supply for the circuit was built during the soldering of the project. The oscillator stage was first tested to confirm the oscillator on the breadboard.

(ii) OSCILLOSCOPE: The oscilloscope was used to observe the ripples in the power supply waveform and also to check the frequency and the wave form of all the 32,768Hz oscillator. The oscillator was also used to check the waveform of all the other stages.

(iii) DIGITAL MULTI-METER:- This basically measures voltages, resistances continuity, current, frequency, temperature and transistor life. The process of implementation of the design on the breadboard required the measurement of parameters like voltage, continuity, resistance values of components, frequency. Frequency

measurement was used to check the frequency of the oscillator stage to ensure functionality and ensure the clock frequency is 32,768Hz.

4.1 IMPLEMENTATION

The implementation of the project was done on the breadboard. The power supply was first derived from a bench power supply at the laboratory (to confirm the workability of the circuit before the power supply stage was soldered to on the Vero board. Stage by stage testing was done accordingly to the block representation on the breadboard before soldering of the circuit commences in the Vero board. The decoder driver stages were soldered directly due to the high concentration of connecting wires and ribbon cables.

4.2 CONSTRUCTION

The construction of the project was done in two different stages. The soldering of the circuit and the coupling of the entire project to the casing.

The soldering of the project was done on a Vero board and the components were mounted on the board.

CHAPTER FIVE

5.0 CONCLUSION AND RECOMMENDATION

The project was designed considering some factors such as economy, availability of components and research materials, efficiency, compatibility and durability. The performance of the project after test met design specifications and hence can be said to be satisfactory.

The general operation of the project and performance is dependent on the user who is prone to make human error such as in the operation of the system and is also on some conditions such as operating environment; which is prevalent at that time. In addition, the construction was done in such a way that it makes maintenance and repairs an easy task. Moreover, the circuit is attributed to a crystal oscillation for an exceptional degree of timing accuracy.

5.1 RECOMMENDATION

Its recommendation that certain aspects of the projects design can be worked upon to further improve efficiency of the unit.. Errors due to timing/clocking could be improved upon. So also a LCD (liquid crystal display) could be incorporated instead of the LED seven-segment display.

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