DESIGN AND CONSTRUCTION OF UNANIMOUS VOTE COUNTER MACHINE

BY

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NIGER STATE, NIGERIA.

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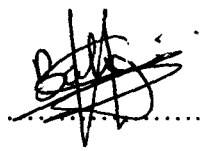
A PROJECT REPORT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF BACHELOR OF ENGINEERING DEGREE (B.ENG.) IN ELECTRICAL AND COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

NOVEMBER, 2004.

DECLARATION

I Alli Babatunde Sulaiman, hereby solemnly declare that this project work "Design and Construction of a Unanimous Vote Counter Machine" is the result of my personal effort. It has never been presented else where either wholly or in part for any degree or diploma.

All information derived from published work used in this project have been duly acknowledged.



Signed Alli B.S.

24/11/'04

Date

CERTIFICATION

This is to certify that this project work was carried out by Alli Babatunde Sulaiman in the department of Electrical and Computer Engineering and it has been found to be adequate in scope and content in partial fulfillment for the award of Bachelor's degree in Electrical and Computer Engineering (B. Eng.).

..... 8/12/04

Engr. J.G. Kolo — Date

(PROJECT SUPERVISOR)

..... 8/12/2004

Engr. M.D. Abdullahi — Date

(HEAD OF DEPARTMENT)

....

EXTERNAL SUPERVISOR — Date

DEDICATION

I dedicate this work to Almighty Allah for his guidance and mercy on me since the day of my inception, till present moment and forever.

ACKNOWLEDGMENT

It is humanly impossible for one to remember all those who has contributed in one way or the other to one's success in endeavor.

For those whose names are not explicitly in mentioned below, I grave your indulgence. My sincere and heart felt thanks goes to my family, starting from my parents Mr. M.A. Alli and Mrs. M.A. Alli who have been such wonderful parents to me. I am so proud to have such a wonderful parent and words alone cannot express how grateful I am, thank you so much for your love.

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My appreciation will not be compele without expressing my beloved gratitude to my broher Lukman (Blakky) for both his finicial and moral support also including my beloved sisters Mrs. Shoungle and Nurse fauziyat Alli. I love you all.

CHAPTER FOUR

LIST OF FIGURES AND TABLES

ABSTRACT

Due to the erratic nature of voting in the senate meeting, school board meeting, and other committees in the institute of higher learning, it becomes necessary to look for an alternative and better method of voting.

The purpose of this work is to develop a machine that will be use as an alternative way of voting it will save time and fraudulent free nature.

The components used in this design are locally available thereby making it possible to produce the design cheaply.

The counter was designed using 74LS83 and 74LS283 as a summation components. The design was designed to accommodate just twenty-four voters at same time.

CHAPTER ONE

1.0. GENERAL INTRODUCTION

As a result of the way voting is been held in the senate meeting, school board meeting and other committees in the institute of higher learning, where motion is been proposed for deliberation which then result into voting. In these deliberation, it is either supported or opposed by the members but due to waste of time in counting the members by the electoral officials during voting and fraudulent way of voting twice or been counted twice, which may result to cheating of one party or another within the committees.

Inspite of the modern technology advancement this process can be done in a more better and systematic way, where voting of is been casted at the same time by its members which then give rise to immediate display of result. This lead to the a development Digital Unanimous voter counter machine which is applicable when people are For or Against a motion and the result is to be display immediately.

The design and construction of Digital Unanimous Vote Counter Machine is an introduction to the voting process that will help in reducing fraudulent acts, waste of time in the meeting, easing and evaluating of results. It also give room for privacy during voting so that the members are not aware of each others votes.

However, these design is concerned with voting of occurrence, this a process whereby number of member For or Against a particular motion is counted properly that is, it is a process of rectifying the afore mention problems, whereby along lasting solution will be provided in such senate meetings, school board meetings and other committees as sated above.

In the design and construction of the vote counter machine, low cost available components and reliable operation where primary factors of consideration to take care of the above mentioned constraints in the conventional way of voting. I initiated this into the design by it doing the task of summing the various opinions (For or Against) a motion raised and display the result (For or Against) on a display board which is essentially a seven-segments display. It employs a handheld keypad, which is a switch held by each member, a summing section and a display unit section.

This is achieved when each member press on the Yes or No keypad, the summation of these (yes or no) are then sum up by a full adder using both 74LS83 serial adder and a 74LS283 parallel full adder which the send the result to a decoder that interprets the impulse signal into a seven-segment that serve as a display unit thus displaying the results for both Yes and No options. With the displayed results the discrepancy within the members is brought to an end.

Therefore Digital Unanimous Vote Counter machine in such committee and board meetings has become a necessary material/equipment else it will be difficult to meet up to the challenges of the new era of technology

1.1. AIMS AND OBJECTIVES

The design and construction of the Digital Unanimous Vote Counter Machine is targets towards the following:

- The use of readily available components in the markets.
- To reduce the overall cost.
- To reduce fraudulent acts and other vices that occurs during voting exercise.

- Easing and reducing task of electoral officials during practice and evaluation of figures.
- Saving time during voting by display of result immediately after voting.
- To give rise to privacy of members during voting.
- To create efficiency and flexibility.

1.2. LITERATURE SURVEY/REVIEW

Haven been privileged to watch some of the events that have unfolded in the senate meeting, school board meeting and other committee in the institute of higher learning but I do believe that there should be special measures to be invoked towards saving voting system of committees/meetings.

The practice of counting the number of particular people that support certain decision and number of people that is against such decision as been ways of practice in meetings over the years but this method serve as waste of time and other vices which may occur during counting.

The right to vote today is far more than the right of one rising hand to be counted, because voting has gone through a lot of technological advancement. It is this development in technology that has lead to the development of Digital Unanimous Vote Counter Machine which can be use in the afore mention group of meetings to meet up with the challenges of the 20^{th} century development.

These will to some extent prevent counting vices like fraudulent of officials and so on, during the exercise. This system works on principle of latch and execute mode, which

will help to give right to an equal and meaningful vote which includes the right to equal and meaningful participation.

1.2.PROJECT OUTLINE

This write up centers around the design and construction of a unanimous vote counter machine and it gives a step by step analysis of the design stages involved.

The chapter one gives a wide introduction, project aim and objectives, and the literature review.

The second chapter deals with system theory of designing the work and the calculations of the components used.

The third chapter deals with construction and testing of the unanimous vote counter machine

The fourth chapter deals with maintenance, conclusion, recommendation and references

CHAPTER TWO

SYSTEM DESIGN AND ANALYSIS

2.0 INTRODUCTION

It is a common practice in electrical, electronics and computer engineering to always describe system with the aid of block diagrams. Therefore the block diagrams of the system under design are hereby presented in figure 2.0 below.

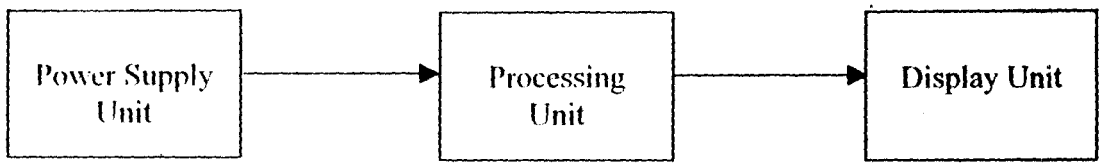

FIG. 2.0: block diagram of the Digital Unanimous Vote Counter machine.

Power Supply Unit (PSU): this is the source of the electrical energy or power to the system. Its indispensability can be appreciated from the fact that without it the system will not be able to perform any work. The unit provides 5 V direct voltages with a common ground to other unit of the system.

Processing Unit: it is the unit that deals with summation of all the voters both the support and against that is the Yes and No are store in binary before converting to display unit.

Display Unit: this constitutes the electronic components for converting the binary coded decimal to a digital display equivalent for presenting the ladder in a form comprehensible to human being.

2.1 POWER SUPPLY UNIT

Since electronic circuit being designed requires dc voltages 15 V and -5 V with their common ground, the power supply unit converts the domestically supplied 220 V-240 V ac voltage into the required dc voltages which are expected to be constant even though variations occur in the ac supply voltage.

To achieve the above dc voltage, series of stages are involved in the power supply unit and they include

- Transformation stage.
- Rectification stage
- Filtering stage
- Regulation stage

The block diagram of the power supply shows the various stages involved and their output waveform are shown below in figure 2.1

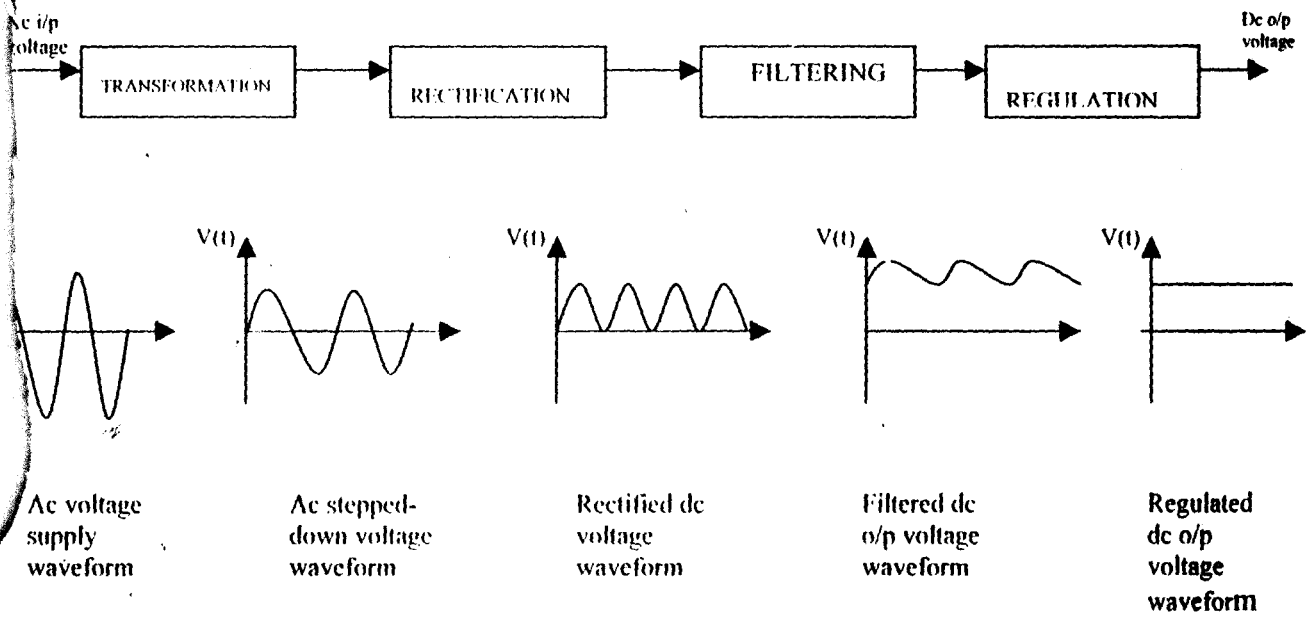

Fig. 2.1: Block Schematic of the Power Supply Unit (with corresponding output waveform of each block)

2.1.1 Transformation stage

This stage involves transforming the domestic ac supply from level of 240 into a lower level of 15 V- 0 – 15 V. therefore a stepped down transformer center tapped is required to be used.

The output current of this transformer used from the manufacturer is 500mA. The circuit diagram of the transformation stage is shown below in figure 2.2

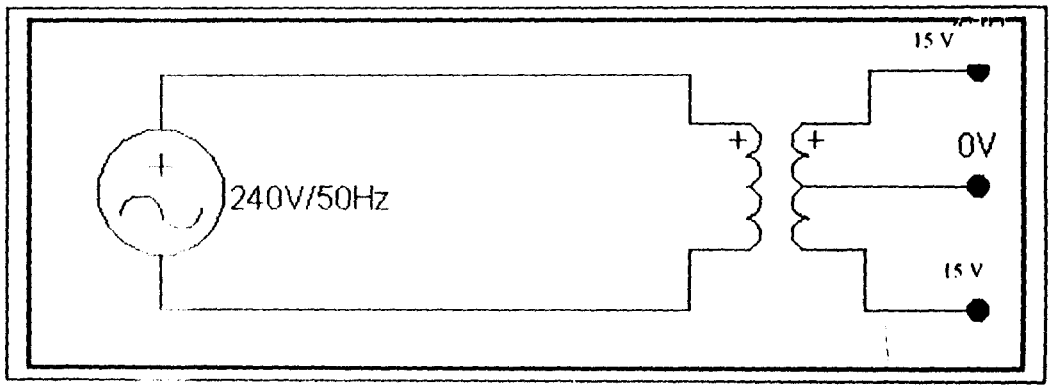

Fig. 2.2: circuit diagram of a transformer

2.1.2 Rectification Stage

The essence of this stage is to rectify the stepped down 30 V – 0 – 30V ac voltage by converting it into a dc voltage of approximately the same value by employing one or more diodes. The circuit connection that does this is known as rectifying circuit.

For the purpose of good output a full bridge rectifier was used to curb away less ripples and produce twice as much output voltage of other rectification (half-wave, double wave). The internal circuit of the bridge rectifier is presented in figure 2.3.

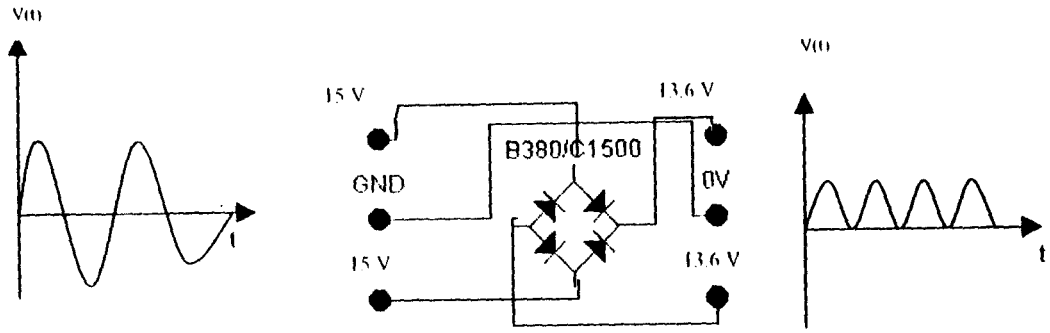

Fig. 2.3: circuit diagram of a full wave bridge rectifier

The full wave bridge has been chosen because

- It makes use of small transformer
- It has lower ripple factor compared to half-wave rectifier
- The peak inverse voltage (PIV) rating of each diode is also less

As it can be seen from figure 2.3, the output of this stage is pulsating but needs to be smoothened, consequently leading to the next stage, filtering stage.

2.1.3 Filtering Stage

The output of the previous stage –rectification consist of two components

- a dc component
- A number of ac components which form what is known as ripple.

The vitality of the filtering stage is to eliminate the ripple or at least reduce it to such a value that its influence becomes negligible in the circuit.

Various types of filters are bound but the choice of this project work is a shunt capacitor filter shown in figure 2.4.

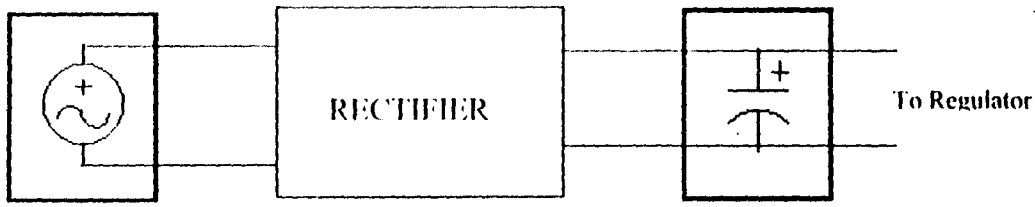

Fig. 2.4: circuit diagram showing a shunt capacitor C

Filter Design

If a light load, R_l is connected across the capacitor the ripple voltage which occurs can be approximated by a triangular wave shown below in figure 2.5. The ripple voltage has a peak to peak value of $V_{r(p-p)}$ and a time period of T_r centered around the dc level, where T_r is the discharging time. Since the charging time is negligibly small compared to T_r, then T approximately equal to T_r. $V_{r(p-p)}$ is the amount that which the capacitor voltage drop during discharging period, Tr. The charge ΔQ lost in this interval is ;

$$\Delta Q = I_{dc} \cdot T_r ;$$

Where, I_{dc} is the current flowing through the load.

Therefore,

$$V_{r(p-p} = \frac{\Delta Q}{C} = \frac{I_{dc}.T_r}{C}$$

$$\frac{I_{dc.}}{F_r.C} = \frac{V_{dc.}}{C.F_r.R_l}$$

Where, F_r is the frequency of the ripple component.

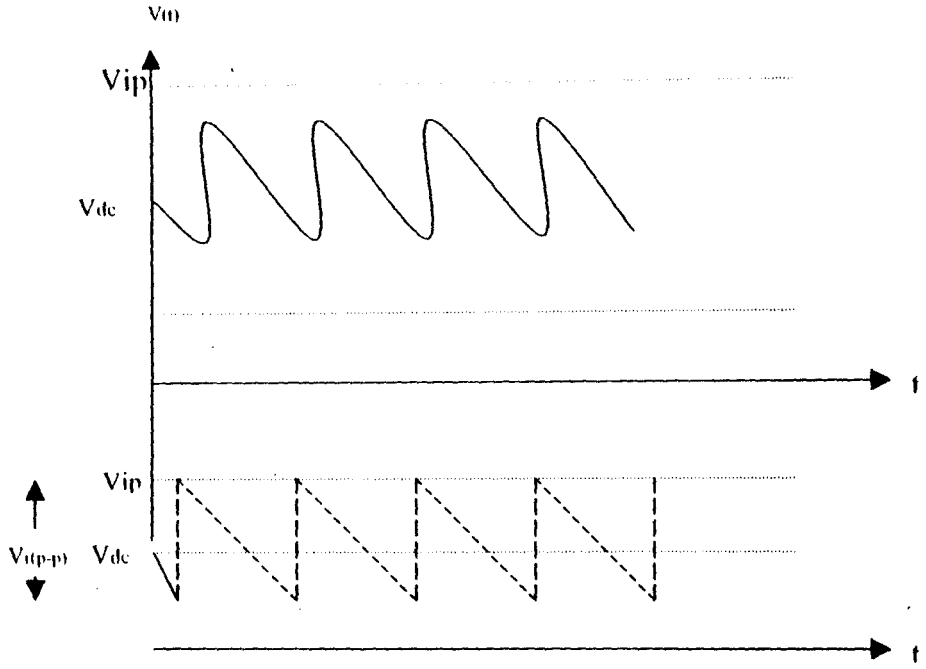

Fig. 2.5: triangular approximation of the ripple component of the output of the rectifier.

The root means square value of the triangular ripple is

$$Vrms = \frac{V_{dc}}{2\sqrt{3}F_rCR_f}$$

The ripple factor, r is define as $r = \frac{V_{r(rms)}}{V_{dc}} = \frac{I_{dc}}{4\sqrt{3}FCV_rC}$

Since the ripple frequency Fr is twice the supply frequency F and $R_L = \frac{V_{ip}}{I_{dC}}$

For this design a ripple factor of r = 1.5% is desired for better performance.

Im = 500mA

F = 50Hz

Vip = 30 V

$$\text{Then } C = \frac{500 * 10^{-3} * 2}{4\sqrt{3} * 0.015 * 50 * 30 * \pi} = 2047\ \mu F$$

C is approximately 2100 μF

Consequently to the design above, in figure 2.7 below shows the circuit diagram of the filter for 13.6 V and -13.6 V.

2.1.4 Regulator Stage

This stage ensures that the output of the power supply unit is constant voltage. One of the simpler and most common electronic ways of regulating is to make use of integrated circuit (IC) regulators which regulates the output of a dc power supply. There are fix voltage regulator ICs that maintain a specified output voltage level in-spite of changes in the ac input voltage level and loading on the dc output.

For the purpose of this design one of the voltage regulator called adjustable regulator was used to adjust the dc voltage to the required output dc voltage that is 5 V that was used for the transistor transistor logic (TTL) devices.

The output voltage was calculated below for an output dc voltage of 5 V.

$V_{out} = V_{ref} \times R_2/(R_1 + R_2)$

$I_{limit} = V_{sc}/R_{sc}$

Where V_{sc} is the silicon voltage = 0.7 V

$R_3 = R_1 R_2/(R_1 + R_2)$

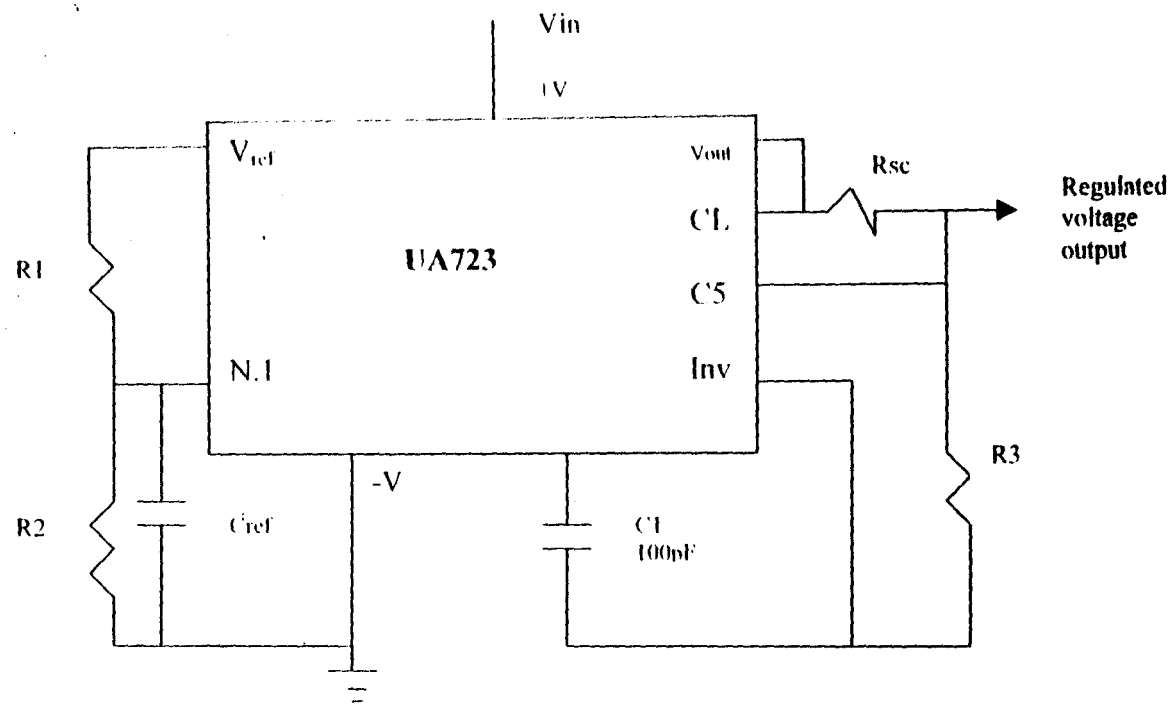

Fig. 2.6: Connection of regulator UA723

Values used are

R1 = 2.15 K

R2 = 5.0 K

Then R3 = 2.2 x 5 /(2.2 + 5) = 10.1/7.2 = 1.53 K

R3 = 1.5 K

The approximations are used on standard resistors values.

V_{out} = 5 V

V_{out} = V1 = 5 V

$V_{ref} = ((R1 + R2) /R2) \times V_{out}$

= ((2.2 + 5) /5) x 5

V_{ref} = 7.2

$I_{limit} = V_{sc} / R_{sc}$

But $R_{sc} = V_{sc} / I_{limit}$ = 0.7/5 = 0.14

Hence,

$R = 0.15\Omega$

$P = IV = 5x\ 5 = 25\ W$

R_{sc} = choke resistor $= 0.15\Omega$ by 25 W

2.2.0 PROCESSING UNIT

This is the unit that deals with how the voting are been added once the key pad has been switched for Yes or No by members of the committees. In carrying out the following steps or design were used

- Key pad
- Adders (i) 74LS83
  (ii) 74LS283
- Transistors

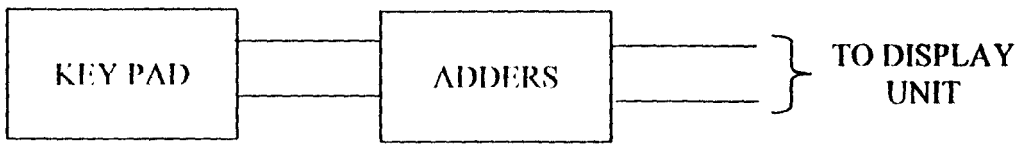

Fig. 2.6 Block Diagram of the processing unit

The figure above shows how the processing unit is been processed or the stages involved.

2.2.1 KEY PAD

The key pad used is push button types in which once the member push the button the signal will be send to the next stage of the processing unit, adders.

2.2.2 ADDERS

Very often in digital circuitry, the need arises for addition, subtraction, multiplication or division of two binary numbers. For all this arithmetic process the basic circuit employed is the binary adders since it can be modified with the additional logic circuit to perform other functions. It is divided into two

i. Half adders

ii. Full adders

Half Adders: This is the simplest form of binary adder. It accept two binary inputs on its input A and B but it does not have a carry input and produces two binary digit on its output, a sum bit and carry bit.

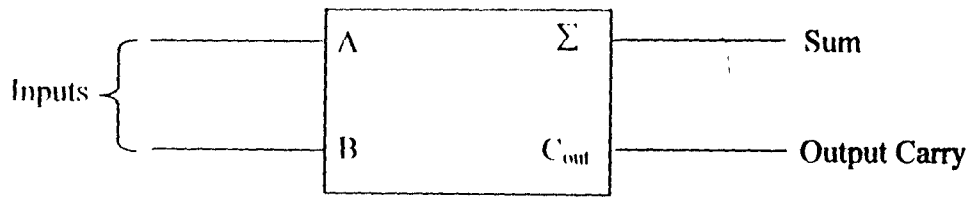

Fig. 2.7 logic symbol for half adder

Full Adders: This is a combination circuit which adds two input bits A and B together with a possible carrying input bit C_0 from the previous stage to generate a sum output and an output carry.

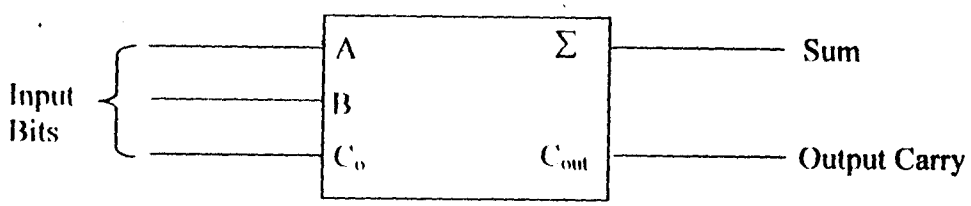

Fig. 2.7.1 logic symbol for a full adder

For the purpose of this project, the IC internal addition makes use of a full adder. The addition of each bits of A_x and B_x are added first, generating a sum bits S_x and a carry bits C_{in} is then added to it before generating the carry out bit C_{out}.

A true table of its operation generation is shown in table 2.0

INPUTS			OUTPUTS	
A	B	C_{in}	Σ	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2.0. A True table for a full adder.

Where; A and B input variables

C_{in} – input carry

C_{out} – output carry

Σ - Sum

From the true table the sum of the inputs A and B is an exclusive OR i.e. $A \oplus B$. Also for the input carry C_{in} to be added to input to generate the sum output of the full added it must also be exclusive ORed with the $A \oplus B$. $\Sigma = (A \oplus B) \oplus C_{in}$.

For generating output carry to be 1, then both input to the first exclusive OR gate are 1s or when both inputs to the second exclusive OR gate are 1s. Therefore the output carry is produce by the input A ANDed with B and $A \oplus B$ ANDed with Cin.

These two terms are ORed

$C_{out} = AB + (A \oplus B)C_{in}$

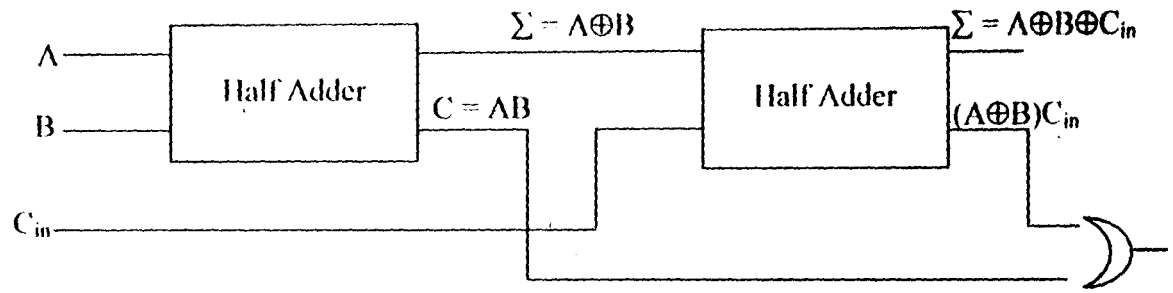

Fig. 2.7.2 Block Symbol of Generating full adder

2.2.2.1 74LS83 AND 74LS283

Adders that are available in integrated form are parallel binary adder, but for the purpose of this project a 4 bits parallel binary adders of 74LS83 and 74LS283 which of the Transistor Transistor Logic family (TTL).

74LS83

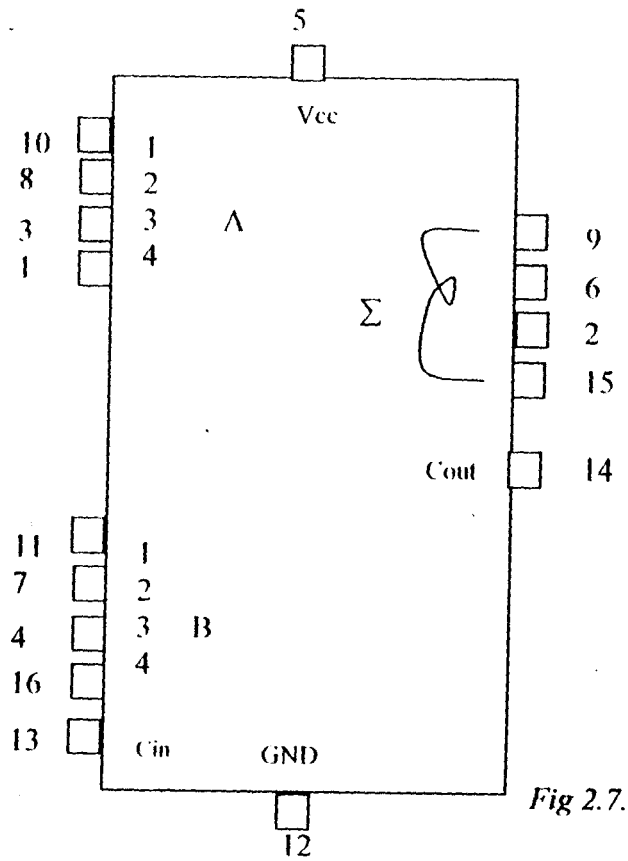

Fig 2.7.3 logical symbol of 74LS83

The input pin for the A input A_1-A_4 are numbered pin (10, 8, 3, 1,) with pin1 as the most significant bit, for the B input B_1-B_4 are number pin (11, 7, 4, 16) with pin16 as the most significant bit, pin13 is the carry in bit, for the sum out of Σ_1-Σ_4 it is number pin (9, 6,2,15) and the carryout bit is pin14. Then pin 5 and pin 12 serve as the input voltage V_{cc} and ground respectively.

In these project, the most significant bit A_4 (pin 1), B_4 (pin 16) and input carry C_{in} (pin 13) were used for the addition and other inputs bits not used were grounded. The sum bit E4 was also used as the sum output bit and the carry output C_4 (pin 14) were used.

For the addition expansion in these project, pin A_1-A_3 and B_1- B_3 were grounded because of the ripple effect, that is the 74LS83 cannot produce a potential output until an input carry is applied, then the carry input must be rippled in before the final sum is produce, though the A4 and B4 must be added before the carry input is added. The delay time for the sum to sum is 16 ns and sum into carry is 11 ns.

In order to avoid impulse signal to the input not used as input voting a 1KΩ resistor was connected to the input A4, B4, and C4, so that anytime one of the input not is off impulse signal will not be allowed into the IC.

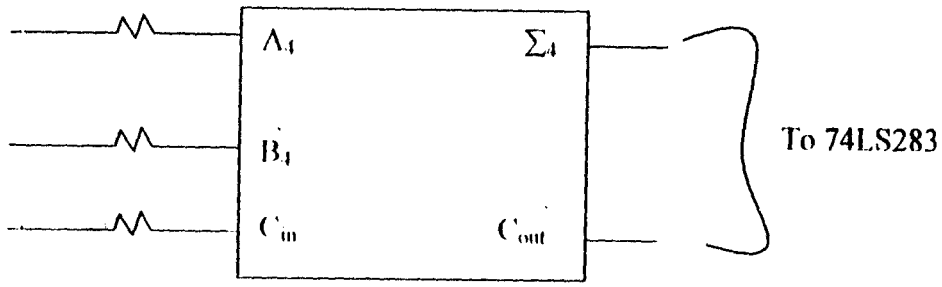

Fig. 2.7.4. Logic symbol for 74LS83 used.

INPUTS			OUTPUTS	
C_{in}	B4	A4	Σ	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2.1 A truth table for 74LS83

74IS283

This is also TTL with an eleven inputs pins five output pins. The logical symbol is shown below in figure 2.7.5.

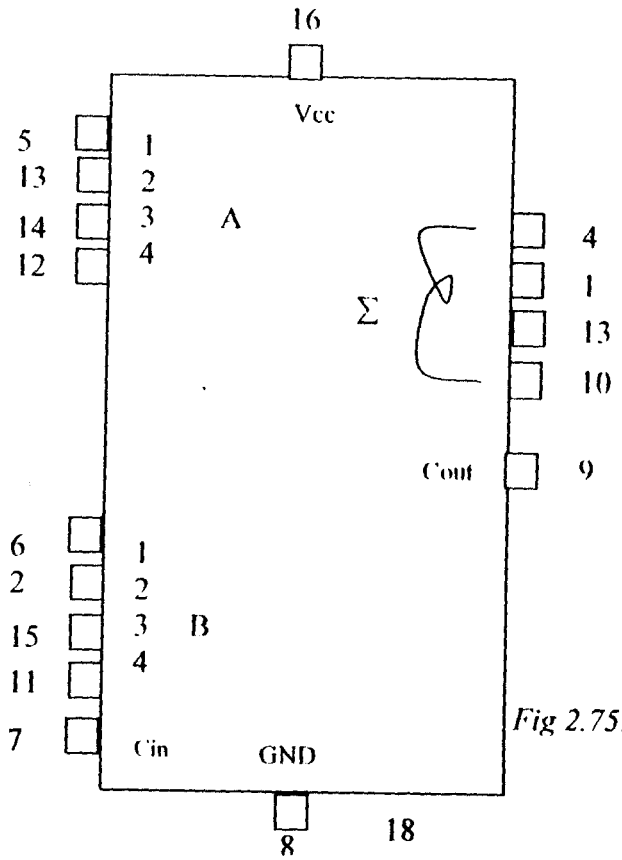

Fig 2.75: Logic symbol of 74LS283

The IC 74LS283 is functionally identical to that of 74ls83 but different pin compatibility that is the pin number for the inputs and output are different due to different in power and ground connections.

The inputs pin for A input A1-A4 are number pin (5, 13, 14, 12) with pin 12 as the most significant figure(MSB) and pin 5 as least significant figure (LSB), for B input B1-B4 are number pin (6, 2, 15, 11) with pin 6 as least significant figure and pin 11 as the most significant figure, for the sum out bits $\sum_1$-$\sum_4$ are numbered pin (4, 1, 13, 10) and carry in bit is pin 7 with carry out bit as pin 9 while pin 16 and pin 8 serve as input voltage V_{cc} and ground respectively.

In this project, 74LS283 was used for addition expansion of the voters of each section of Yes and No part, one 74LS283 was used for further expansion of two 74LS83 and another 74lS283 is used for the addition expansion of two 74LS283 before sending the impulse signal to the display unit.

For the first 74LS283 bit A1, A2 and B1, B2 were the used inputs bits from two 74LS83 and the other inputs including C_{in} were grounded, then the sum out E1-E4 were used as input as input for another 74LS283 as inputsA1-A4 while another set of 74LS283producing another sum E1-E4 from two 74LS83 which is then use as an inputB1-B4 for 74LS283. Then the addition is sent to the display unit.

The addition expansion in 74LS283 eliminates the ripple effects in74LS83 by the use of a look-ahead carry adder produced internally. This is done by producing either carry generation or carry propagation. The carry propagation occurs when an output carry is produce internally, for these to occur the inputs must be 1s that is High, it is expressed as a AND gate Cg =AB. But for the carry propagation, it occurs when the input carry is rippled to become the output.

The inputs carry may be on when either or both inputs bits are 1s. It is expressed as an OR function that is Cp = A + B.

The 74LS283 make the voting result faster because carry inputs and carry output are computed simultaneously. Figure 2.7.5 show the internal structure of how these is achieved. Also the table of 2.2 shows the truth table of four bit parallel adder of 74LS283.

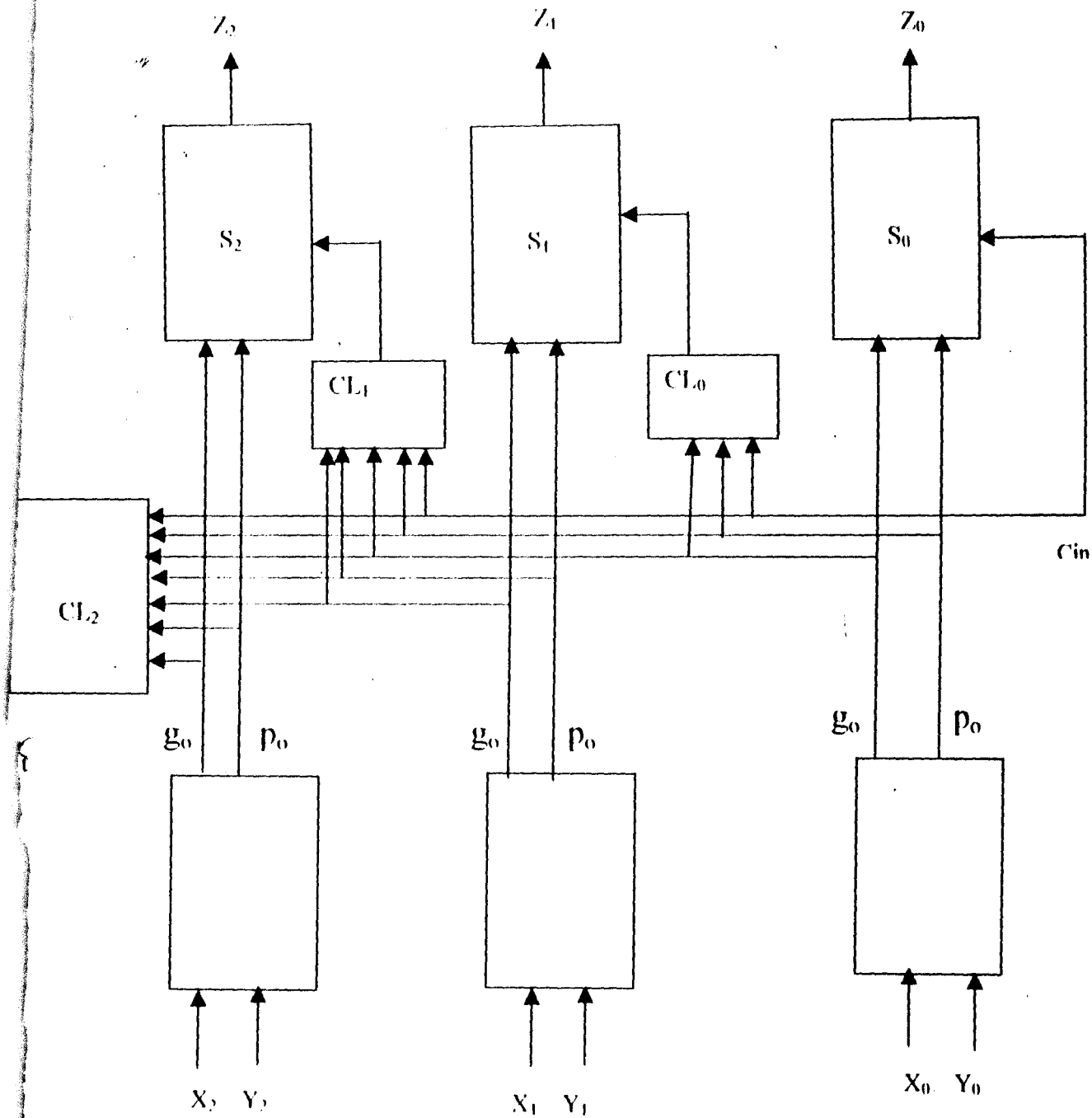

Fig. 2.7.6 Internal structure illustrating a carry look-ahead of 74LS283

Gi =XiYi

Zi =Xi ⊕ Yi ⊕

Pi = Xi ⊕ Yi

Ci = XiYi + XiCi + YiCi

=XiYi + Ci (Xi ⊕ Yi)

= Gi+ CiPi

Where Gi =propagation generation

Pi = propagation carry

Xi and Yi =input variables

Ci = carry output

/N	INPUTS				OUTPUTS					
					When $C_0 = C_2 = 0$			When $C_0 = C_2 = 1$		
	A1, A3	B1, B3	A2, A4	B2, B4	Σ1, Σ3	Σ2, Σ4	C2, C4	Σ1, Σ3	Σ2, Σ4	C2, C4
0	0	0	0	0	0	0	0	1	0	0
1	1	0	0	0	1	0	0	0	1	0
2	0	1	0	0	1	0	0	0	1	0
	1	1	0	0	0	1	0	1	1	0
	0	0	1	0	0	1	0	1	1	0
	1	0	1	0	1	1	0	0	0	1
	0	1	1	0	1	1	0	0	0	1
	1	1	1	0	0	0	1	1	0	1
	0	0	0	1	0	1	0	1	1	0
	1	0	0	1	1	1	0	0	0	1
10	0	1	0	1	1	1	0	0	0	1
11	1	1	0	1	0	0	1	1	0	1
12	0	0	1	1	0	0	1	1	0	1
13	1	0	1	1	1	0	1	0	1	1

0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Table 2.2 Truth table of 4 bit 74LS283

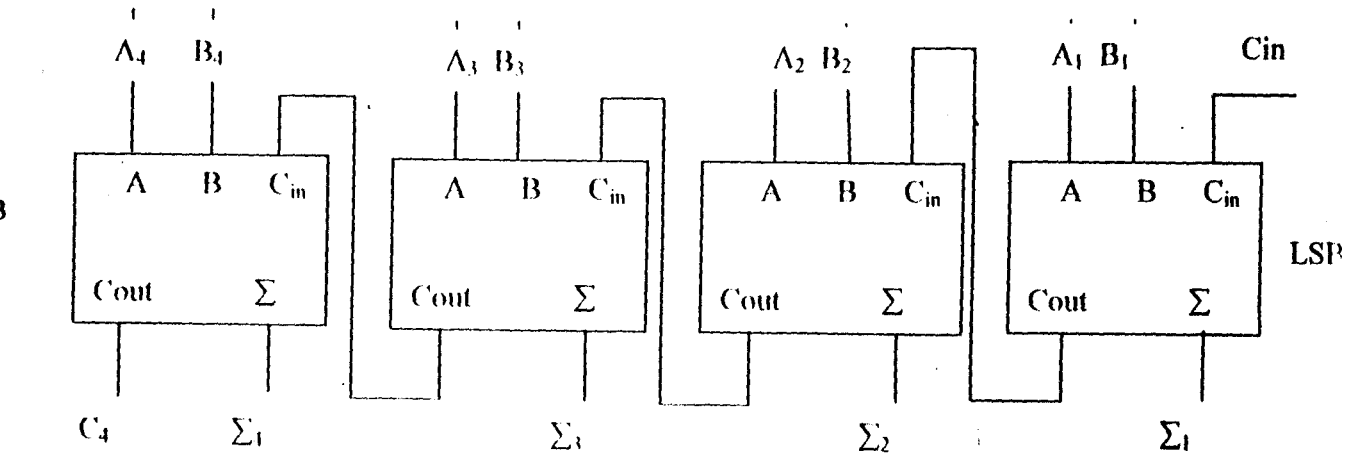

Fig 2.7.7 Block diagram of internal circuitry of 74LS283

2.3.0 DISPLAY UNIT

This unit is the most interesting part of the system because it enhances the readability of the voters as well as offering a room for accuracy of the number of voters. It composes of the binary code decimal to Seven Segment Led Display, Decoder, Transistor and the Seven Segment display unit.

2.3.1 BCD TO SEVEN SEGMENT DECODER

This is a decoder with four input and seven output lines and is formed from a combinational logic circuit. It is normally used to convert the BCD output of a decade counter into a coded output that is suitable to operate the segments of a seven segment LED display.

A 7447A (TTL) BCD to seven segment decoder was used in this project. A logic symbol of a 7447 is shown below, which is powered with a 5 V at the V_{cc}.

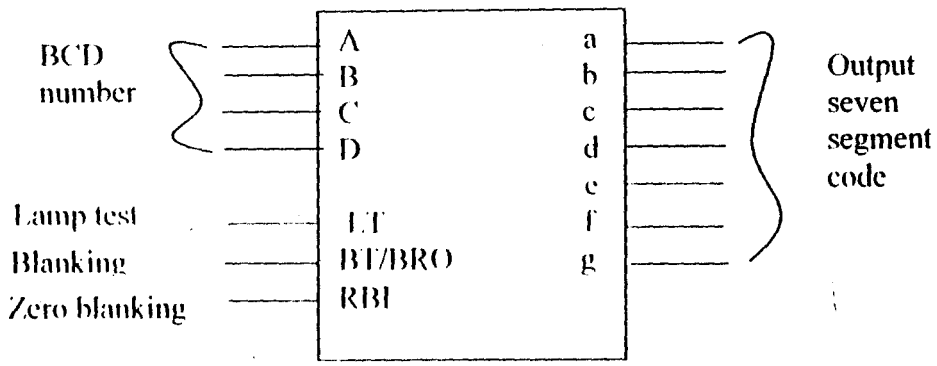

Fig 2.8 A logic symbol of 7447 (TTL)

The BCD number to be decoded is applied to the input labelled D, C, B and A. when activated with a LOW the lamp-test (LT) input activates all output (a to g). When activated with a LOW , the blanking input (BI) makes all output HIGH, turning all the attached display OFF, when activated with a LOW, the ripple-blanking input (RBI) blanks the display only if it contains a 0, when the RBI input becomes active, the BI/RBO pin temporarily becomes the ripple-blanking output (RBO) and drops to a LOW.

The seven outputs on the 7447 IC are all active LOW outputs that is the output are normally HIGH and drop to a LOW when activated.

A truth table and the connection of the 7447 to a Seven Segment LED Display is shown below

Decimal number	INPUTS						BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	1	1	1	1	1	1	0
1	H	X	L	L	L	H	H	0	1	1	0	0	0	0
2	H	X	L	L	H	L	H	1	1	0	1	1	0	1
3	H	X	L	L	H	H	H	1	1	1	1	0	0	1
4	H	X	L	H	L	L	H	0	1	1	0	0	1	1
5	H	X	L	H	L	H	H	1	0	1	1	0	1	1
6	H	X	L	H	H	L	H	0	0	1	1	1	1	1
7	H	X	L	H	H	H	H	1	1	1	0	0	0	0
8	H	X	H	L	L	L	H	1	1	1	1	1	1	1
9	H	X	H	L	L	H	H	1	1	1	0	0	1	1

H – High Level L – Low Level X – Don't Care LT – Lamp Test

BI – Blanking Input RBI – Ripple Blanking input

Table 2.3 Truth table for BCD 7447

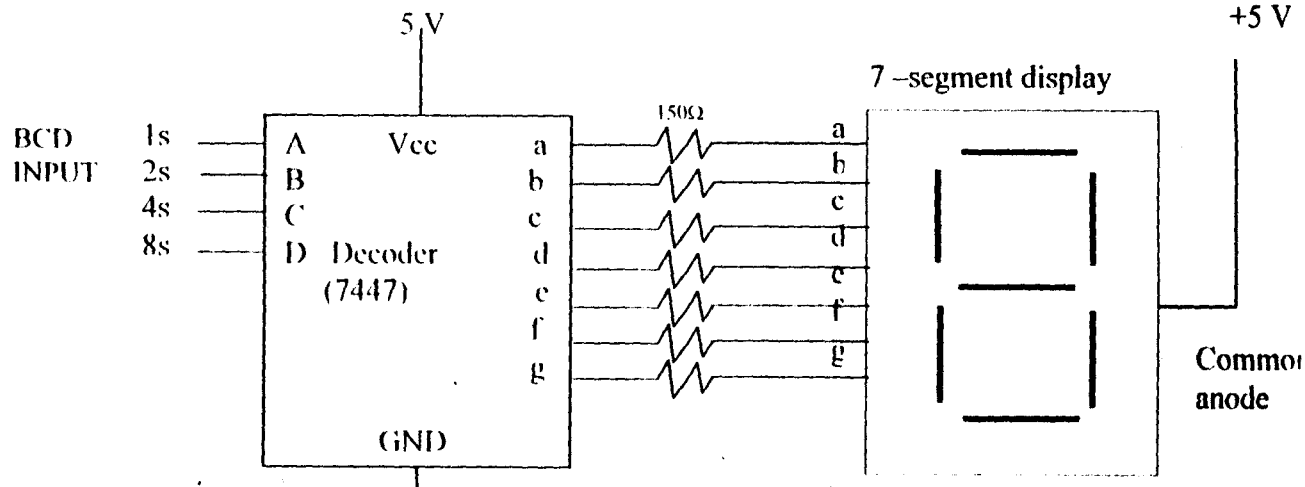

Fig. 2.81 Wiring 7447 decoder and seven segment LED display.

2.3.2 SEVEN SEGMENT DISPLAY

Seven segment displays are used to convert four bit BCD number into a visible readout. The seven segment display may be of LED (Light Emitting Diode) type or LCD (Liquid Crystal Display). But for the purpose of this project LED type was used because of its brightness, low-cost reliability and compatibility with low voltages integrated circuitry.

A typical LED seven segment display is shown in figure 2.8.1 each segment is a LED that emits light when current flows through it. There are of two type of arrangement.

(i) Common cathode

(ii) Common anode

Figure 2.8.1 is in common anode arrangement as used in this project. In which the positive side of the power supply is connected to the anode of each segment and a low voltage from the 7447 to the cathode lights the segment.

In controlling the display, a seven bit code was generated to indicate which segment should be ON or OFF as shown in table 2.3 where 0 corresponds to ON and 1 corresponds to OFF. The seven segments was configured to form the decimal character 0-9.

The segment patterns are used to display the various digits as shown in figure 2.8.2.

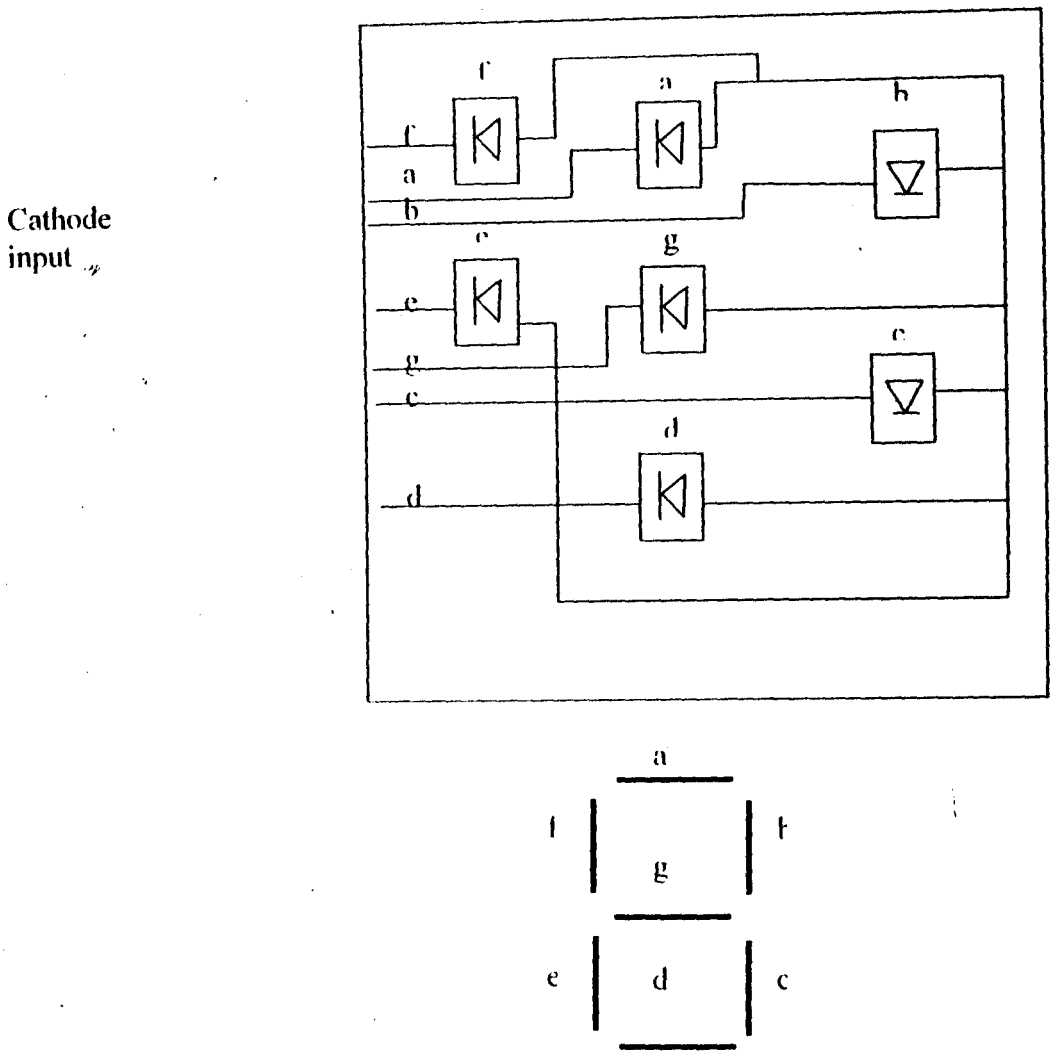

Fig. 2.9 7-Segment arrangement

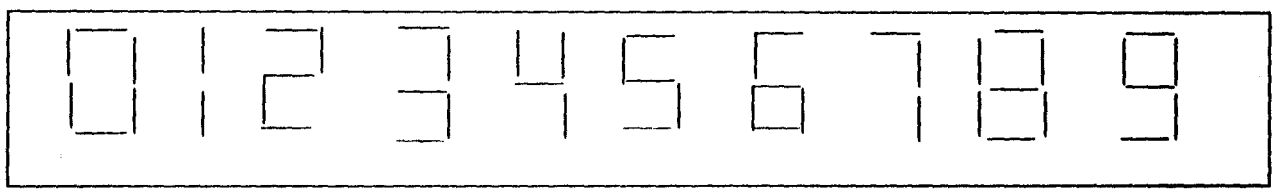

Fig 2.9.1 Active segments for each digit

DISPLAY	INPUTS				OUTPUTS						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	0	0	0

Table 2.3 Truth table for seven segment LED decoder

2.3.2 TRANSISTORS

A transistor NPN with a common emitter, where the voltage is applied between the base and the emitter and the output is taken from the collector and the emitter. Te current flows out from resistor Re. the voltage between the base and the emitter VBE is 0.7 and the voltage applied to the base is 2 V. the current required by each segment of the seven segment LED is 10 mA.

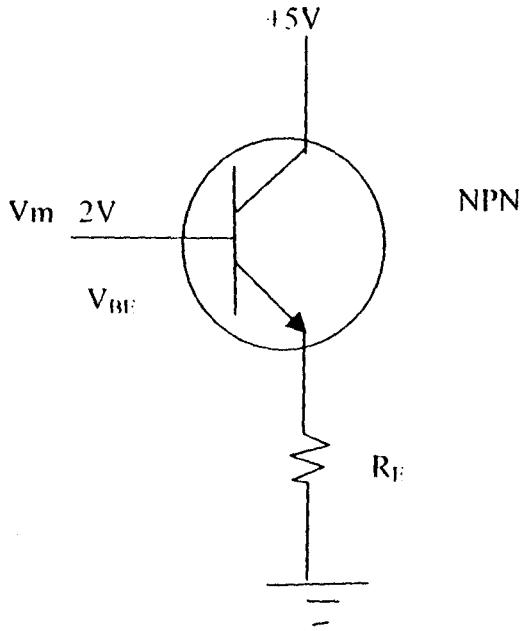

Fig. 2.10 A Transistor

$I_E = 10mA$

$V_{BE} = 0.7V$

$V_{BB} = 2V$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E}$$

$$R_E = \frac{V_{BB} - V_{BE}}{I_E}$$

$= (2 - 0.7)/10 \times 10^{-3}$

$= 130\ \Omega$

CHAPTER THREE

3.0. DESIGN AND CONSTRUCTION

This chapter deals with the construction and testing of the Digital Unanimous Vote Counter Machine which was previously analyzed and designed in the last chapter. The testing of the project was done first on a project board while the construction took place on a Vero board.

3.1.CONSTRUCTION PROCEDURE

Following the design, whose circuit diagram is shown in Appendix A, its construction took place by starting with the power unit first followed by the construction of the processing unit and lastly the display unit.

3.1.1. Power Supply Unit

The transformer, rectifier IC, regulators, filtering capacitor, light indicators (LEDS) with respective current limiting resistors were inserted into appropriate holes on the project board. A digital voltmeter was connected across each of the output terminals and ground to measure the output voltages.

Furthermore, was connection of the primary terminals of the step down transformer of the main ac supply. Following the powering of the circuit, the voltage readings indicated by the voltmeter were recorded down.

Having compared the above values with the standard one, each of the elements or components of the power circuit was then appropriately soldered to the Vero board.

3.1.2. Processing Unit.

Both 74LS83 and 74LS283 IC, for the summation of the Yes and No part were first arrange and inserted on a project board. With an input of 74LS83 that is need for the summation was connected via a resistor then the 74LS283 was inserted along side the 74LS283.

Afterwards, the unit was powered from the power supply unit, after the unit was properly tested each of its constituents was inserted in a 16pin socket that was already soldered on the Vero board.

3.1.3. Display Unit.

The 7447 decoder and seven-segment display as well as the supporting components of resistors and transistor were properly inserted and arrange on the bread board. Power was then supplied to the unit which was subsequently tested.

After the performance of the circuit was satisfactory, the 7447 was inserted into an IC socket that was soldered on the Vero board also the seven-segment display was also inserted onto another IC socket. Each of the external components, resistor and transistor was afterwards soldered to the same

3.1.4. Soldering Process.

Each time a component was soldered heat was supplied through a soldering Iron to one side of one of the component while a soldering lead was applied to the other side of the lead enough to melt the lead. At this instance, the lead melts the leg of melted solder lead was then allowed to cool,

3.1.5. Precautions

The construction would not have been effective and neat or the system could have been rendered manufuntioning if certain precaution were no taken during the construction process.

Some of these precautions are presented thus

- Care was taken to ensure that the heat supplied was not too much for the component to withstand as too much heat could damage the component.
- An IC socket was solder onto to Vero board with the main IC inserted into it rather soldering the component directly unto the board. This habit ensures that the IC pins are not damaged during the soldering and facilitates their replacement or removal in case of damages.
- It was ensure that no power was supplied to a circuit while the reading were been taken in other to reduce the power consumption.
- Proper care was taken to ensure that the correct polarities of polarized component, such as electrolytic capacitor were soldered together.
- All components were properly soldered to the Vero board to avoid shorting of component legs, shunting and opening of circuit.

3.2. TESTING

Each of the consisting units of devices been constructed was first tested on a roject board before then finally soldered to the main Vero boards.

In testing the output n\voltages of various units of the devices digital millimeter nected in parallel across the output terminals was employed.

In other to test the digital read out of the device different numbers of voters were applied to vote for Yes and No. The result of Yes and No tally with the number of voters are shown below.

Number of voters	YES	NO
5	3	2
8	2	6
10	6	4
18	10	8
20	16	4
24	12	12

Table 3.0 Result of number of voters

3.2.1 RESULTS

The results obtained during testing of different number of voters shown above in table 3.0.

CHAPTER FOUR

4.0. CONCLUSION AND RECOMMENDATION

This chapter is the concluding chapter of this report. It deals with the maintenance, conclusion and recommendation of the project design and construction.

4.1. MAINTENANCE

Maintenance is of the most important ways of which a machine can last long. So for this fact, the Digital Unanimous vote machine should be maintained by well trained Engineer. The machine comprises of mainly Integrated Circuit (IC), which is Transistor Transistor Logic (TTL) IC which need proper care and maintenance.

Also after use, the machine should be cover with a dust proof to avoid being dusty.

4.2. CONCLUSION

The aim of this project work has been to provide a alternative to counting of vote in a meeting due to its erratic way. The design and construction of Digital Unanimous vote counter has help to solving these erratic problems of voting in the meetings.

With these design, the voting exercise in the meeting has been taken to meets the challenges of the 21st century.

4.3. RECOMMENDATION

My desire has an Electrical and Computer Engineer is to fully automate the vote machine activities in various meeting were decisions are taken, debated upon thus facilitating the ease of vote counting.

For future improvement, I would recommend the following

- The use of password should incorporate in the machine.
- A gang switch should be use in places of the two way switch
- In addition the device could be interface with a computer for better display.
- Also for future design a battery may incorporated along the power supply.
- In place of the 74LS83 and 74LS283 an arithmetic logic unit could be used.