FOUR CAMERA VIDEO SURVEILLANCE SYSTEM WITH MULTIPLEXED SWITCHING

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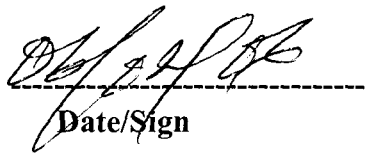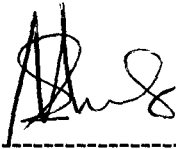
NOVEMBER, 2005

CERTIFICATION

This is to certify that this project work was carried out by Ifeanyichukwu

Egeolu. MAT. No. 99/8150EE, of the department of electrical and

Computer engineering, Federal university of Technology Minna,

Niger state, Nigeria and was duly supervised BY Engr. Emmanuel Eronu.

ENGR M.D Abdullah
(H.O.D Elect. / Cpt.)

Date/Sign

ENGR E. Eronu
(Supervisor)

5 - 12 - 2005

Date/Sign

External Supervisor

Date/Sign

Student
IFEANYICHUKWU EGEOLU

06 - 12 - 2005

Date/Sign

DEDICATION

I dedicate this Project work in Blessed Memory of my father, LATE CELESTINE
NWADEDE EGEOLU. Dad, though you are no more, the legacies you left behind lives
on. May your soul continue to rest in peace till we meet at the bosom of our lord Jesus
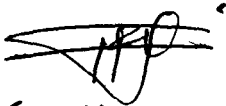Christ

Adieu| Adieu|| Adieu|||

DECLARATION

I declare that this project work was carried out by me and was duly supervised by

Engr. Emmanuel Eronu

06-12-2005

Date/Sign

ACKNOLEDGEMENT

First and foremost, I give God all the praise, honor and adoration for sparing my life and seeing me through.

I also thank God for my mother, Mrs. Juliana Egeolu for her love, attention and supports for me.

I appreciate the kind gesture and love extended to me by Pastor and Mrs. Joshua Jeremiah in the course of typesetting this project write-up. I will also not forget the contributions of Moses, Barnabas, Harrison, Segun and Mr. Pius to make the typesetting of this project a reality. May God continue to bless and protect them. I also wish to thank Mr. Chris for his valuable contribution. I appreciate all those who contributed to the success of this project work and whose names may not have been mentioned here.

I express my gratitude to my lecturers; they indeed imparted unto us knowledge that cannot be quantified. I appreciate my supervisor, Engr. Emmanuel Eronu for his attention, advice and understanding. May God continue to water you all?

Finally, I ascribe all the glory and honor to God the giver of life who made this project possible.

ABSTRACT

This project work aims at implementing a low cost approach to distributing video signals over a common transmission link or sending video pictures from numerous input sources say cameras unto a common output say video cassette recorder, monitor or television set. In other words, this project seeks to provide visual monitoring using multiplexed transmission of video signals.

The use of video for surveillance purposes is known as video surveillance. The term multiplexer refers to an electronic device that time multiplexer's video pictures from numerous input sources unto a single output.

The major components used in the implementation of this project include;

1. 74HC4052 Dual 4-Channel Multiplexer

2. CD4518 Dual binary up counter

3. SN7445 BCD-To-Decimal Decoder/Driver

4. NE555 Timer Oscillator

5. LM337 and LM317 Three –Terminal/Adjustable positive and Negative voltage regulators respectively.

This project work makes use of four video input channels and two output channels. One of the output channels is manually controlled while the other is controlled through an automatic means. This project work implements a wired scheme as against a wireless scheme.

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Chapter One Introduction

1.0 Introduction to Video Surveillance

The word surveillance simply means keeping close watch. Close watch can be kept on an event such as a sporting event, action, persons suspected of wrong doing and so on. The term video may assume the following meanings:

1. Related to or used in the process of recording and showing pictures on television.

2. To record a television programme, film or a real event on a tape

3. The process of recording and showing television programmes, films, real events and so on using video cassette recorder and so on.

The use of video for surveillance purposes is known as video surveillance. It can ruin a perfectly good day. You drive up to your self storage facility on an otherwise glorious morning, and there are the tell-tale signs left by an intruder; vanderlism, open doors, renter's property strewn about. It is your worst nightmare, but there is one minor consolation; you have a video-surveillance system, which means there is a chance of catching the responsible party, if...

And there is the problem. There are some big "ifs," especially when you are operating a standard analog video system. You might catch this guy if the quality of the tape is still good enough to make a positive indentification.And if you remembered to change the VHS tapes, as must be done every day. And if you are willing to spend hours sifting through miles of tape to find the scene you need. That is a lot of "ifs". The truth of the matter is, the chances of catching the jerk who messed up your beautiful day are greatly improved with the use of a digital video surveillance system. A digital system essentially uses no magnetic video tape. The video camera converts light directly into

electronic signals which are stored on a hard drive. This may not seem like a major advancement, but in the short history of video surveillance, this is like the invention of the transistor-very big.

1.1 Introduction to Multiplexers

The term multiplexer was given to an electronic device that time multiplexes video pictures from numerous cameras unto one VCR.This means that one field or frame from one camera was switched to the VCR,than immediately following that picture was another field or frame from another camera and so on from each camera, then it started over again. This technique maintains full resolution as does normal video switchers but reduces the time between recorded images so the 2-3 second dead time between normal camera switching was reduced to 17ms (milliseconds) times the number of cameras.

1.1.1   Multiplexer Math

One odd field and one even field (2 fields) make up one frame of video. This is important to multiplexers since they are basically a time base multiplexing device. In a true real time recording mode the above standard of recording sixty (60) pictures or fields per second is adhered to but when we switch to virtual real time or time lapse video recording, every thing changes. In the CCTV world there really does not exist a standard to how many pictures per second are recorded in virtual real time or any time lapse mode. Normally in virtual real time you have (20) twenty pictures per second. In a 24hour time lapse mode you will have five (5) pictures per second for a single density VCR.When you go to double or triple density VCR this number is increased.

When setting up the multiplexer there exists menu or dipswitches to tell the multiplexer this information. If this information is not set up correctly the multiplexer will switch between its input cameras either too slow or too fast resulting in lost video cameras recorded on the VCR or at best reduces the efficiency of the multiplexer. When the VCR changes speed and the multiplexer does not know this fact the above problem exists. To eliminate this entire problem some multiplexes use a camera switcher pulse. This pulse tells the multiplexer electronically when it has recorded the last video image on tape. The multiplexer then can switch to the next input camera, process it and have it ready for output to the VCR. The advantage of using this pulse is that the multiplexer is guaranteed to stay "in sync "with the VCR even if the VCR changes recording speed. Another big advantage you do not have to learn multiplexer math and rest easy your system will record images no matter what. When the menu does not have a particular model of VCR in its menu that is designated to be used or that which one plans to use, then the manual setup in the multiplexer must be used to define the timing. Basically you tell the multiplexer how many pictures per second your VCR is recording depending on your recording speed. Again this information is in the VCR manual. The multiplexer will then compute how often to switch its cameras.

The most important thing that is normally forgotten about multiplexers is that they still are basically video switchers. When many cameras are connected and the time lapse recording is too slow, the time between recording a single image from a particular camera may be too long to catch any event. Basically, the number of camera inputs is taken and divided by the recording pictures per seconds.

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No. of cameras/record pictures per second = update rate. This implies that if a 16 camera system records at a 168hour time lapse mode then there will be 17.40 seconds from recording a new image from any one camera input. This of course would have little use in any application since someone could walk by and never be recorded. If we reduce the recording to 24hr. time lapse then we would have a new image every 3.2 seconds. This would be more acceptable but not very applicable in high traffic areas. If we went to 24hr. virtual real time at 20 pictures per second then we would have new image every 8 seconds. This is more like it and will be useful in most applications.

1.1.2   Multiplexer Types

- Simplex

The simplex multiplexer is basically the lowest cost since it has the least amount of features. A simplex multiplexer has the ability to time base multiplex to the VCR and all the timing setups required. The main thing a simplex multiplexer does not have is the ability to record and show a multiscreen display at the same time whether it is 4,8,16 or 32 camera screen. Normally simplex multiplexers have no capability for multiscreen display at all. In this project, the use of simplex multiplexer is employed

- Duplex

A full duplex multiplexer has the ability to display the multiscreen and record to the VCR the multiplexed data. Some duplex multiplexers can play back from one VCR while recording on another but you give up the multisrceen viewing at this time.

- Full duplex

A full duplex multiplexer has the ability to record the multiplexed output to one VCR, playback from another, and view the multiscreen at the same time.

- Triplex

A triplex multiplexer has all the features of the full duplex but the multiscreen output can be substituted for a third VCR if desired.

1.2 Objective

The objective for this project work is to provide visual monitoring using multiplexed transmission of video signals. This project work is geared towards a low cost approach to distributing video signals over a common transmission link. It can be used as a means of time multiplexing or sending video pictures from numerous sources say cameras unto one or common output say video cassette recorder, monitor or television

This project work aims at actualizing two modes of operation that is manual and automatic. In other words, this project incorporates the use of two video outputs; one of the two is controlled manually while the other is automatically controlled. The scan rate of the video picture input going into one of the output nodes is determined manually while the scan rate of the video picture into the second output node is determined automatically via a fixed or predetermined scan rate. However, one can choose to make use of a single output node to view video pictures from several input sources.

This project work finds application in commercial establishments such as banks, stores, airports and other sensitive places or areas of high security consciousness. This project work can also be applied to recording studies, halls, sporting arenas, video routing, and so on

1.3 Scope

The design and construction of this project work, four (4) camera video Surveillance system with multiplexed switching is limited to four (4) camera video input sources and two video output units. The scan rate of the video picture going to one of the output units is manually controlled or determined while the scan rate or frequency of the video input to the second video output is automatically controlled or determined.Summarily,video pictures from the four camera input sources is time multiplexed unto one output unit.

However, this project can be expanded to inculcate numerous camera video inputs as desired, unto a single output unit. The design and construction of this project implements wired video surveillance system and not wireless.Nevertheless, the project can be modified to operate in a wireless mode. Also, this project seeks to make use of VCD video input sources instead of camera video input sources, for demonstration purposes. However, camera source can be effectively used.

Chapter Two Review of the Literature

2.0 Introduction

Mention video surveillance and most people think of video cameras mounted in the corners of train stations or private detectives video taping a messy case. The truth is that the history of video surveillance is much more complex and goes back much farther than most people realize.

If you consider video in the simplest term, video surveillance began with simple closed circuit television monitoring. As early as 1965, there were press reports in the United States suggesting police use of surveillance cameras in public places. In 1969, police cameras were installed in the New York City municipal Building near city Hall. The practice soon spread to other cities, with closed circuit television (CCTV) watched by officers at all times.

2.1 Analog beginnings spur video surveillance

When video cassette recorders hit the market, video surveillance really hit its stride. Analog technology using taped video cassette recordings meant surveillance could be preserved on tape as evidence. The seventies saw around the world in the use of video surveillance in everything from law enforcement to traffic control and divorce proceedings.

England installed video surveillance systems in four major underground Train Stations in 1975 and began monitoring traffic flow on major highway arteries about the same time. In the United States, the use of video surveillance was not quite as prevalent

until the 1980's for public areas, but store owners and banks quickly understood the value of it.

Businesses that were prone to theft, including banks, mini-parts and gas stations, began mounting video surveillance systems as deterrent and in hopes of apprehending thieves, particularly in high crime areas.

The insurance industry also found video surveillance compelling—worker's compensation Fraud, bogus accident claims and variety of other cases began to turn in the industry's favour when they could provide tapes of supposedly, disabled workers doing the limbo at a family reunion.

For the private citizen, analog technology was primarily used in the 1970's and 1980's for capturing the worst side of human nature ---cheating spouses and poor parenting. Private detectives were able to provide more graphic and compelling evidence of affairs and parental stupidity with films than with still shots, and video tapes became frequent evidence in family court.

The draw back in many cases was that after a while, owners and employees become complacent and not change the tapes daily or the tapes would wear out after months of being re-used. There was also the problem of recording at night or in low light. While the concept was good, the technology had not yet peaked. The next step was the Coupled Device Camera (CCD), which used microchip computer technology. This new cameras broaded the practical applications of video surveillance by allowing low light and night recording possible.

In the 1990's advancement in the history of video surveillance made great strides in practicality multiplexing. When digital multiplexer units became affordable, it

revolutionized the surveillance industry enabling recording on several cameras at once (more than a dozen at time in most cases). Digital multiplexing features like time – laps and motion – only recording which saved a great deal of wasted video tape. By the mid-1990's, ATM's across the United States and in most parts of the word have video cameras to record all transactions. After the attack in February of 1993, The New York Department, FBI and CIA all installed surveillance cameras throughout the area. Soon many countries are using either CCTV or video tapes surveillance to cover major sporting events that could be potential hot spots such as the world soccer games at giant stadium in 1994.

2.2 Multiplexer History

The early multiplexers were basically video switchers that could mark each camera with a unique number in a vertical interval. This required the cameras to be genlocked or v-phase so the VCR would see a continuously composite sync signal so it would not loose servo lock on the switched incoming video signals. The playback mechanism merely switched to the correct camera only during its active period on the tape while switching to a flat field for the rest of the use of the time. This caused severe flicker but produced a viewable single camera image and was effective.

Later digital memory was used to save the active camera until a new picture was displayed. Early genlocking or v-phasing was poor and cameras drifted causing the VCR to record garbage, thereby resulting in poor playback regardless of digital memory or not. Next a two field digital memory was used to time base correct the incoming signal to guarantee continuous composite video to the VCR. The main benefit of this technology

was that this device guarantees continuous composite sync to the VCR regardless of the video quality. A side benefit was that non genlocked or any camera could be used. This method is the preferred method used among multiplexer manufacturers. The problem of this approach is that encoder and decoder is rather costly and is usually packaged together since they are basically the same internal hardware.

Since new cameras have quality genlocking system and / or stable line locked vertical intervals, a reversion to the old technology is feasible. If time base correcting is not required, a low cost analog only encoder can be used that merely marks each vertical interval with the camera number. The decoder would then contain the digital field memories for playback. This system would be viable for retailers that have small locations and one common location for review. The many locations will have the low cost encoder and the few common locations would have the high cost decoder.

2.3 9/11 redefine video surveillance for the future

Nothing changed the concept of the public's awareness of video surveillance as much as the tragic events of September 11, 2001 when the World Trade Center was attacked by terrorists. Where once people saw video surveillance as an issue that might never affect them, it was now an issue of immediate and lasting importance. Software developers began refining programs that would enhance video surveillance, including facial recognition programs that could compare various key facial feature points in order to match recorded faces to known photographs of terrorists or crimininals while the earlier versions weren't always reliable, the later versions became more refined and were

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phased into use by law enforcement in some areas. In may of 2002, the united states

parks service installed face recognition software on the stature of liberty and Ellis Island.

That same year, the Sidney international Airport in Australia installed smart

Guide, an automated border crossing system used for all airline crew members. Using

photo biometrics, the video surveillance systems scans the crew members' face and

compares it to the passport photo and confirms the match in less than ten seconds.

In December of 2003, Royal Palm Middle School in Phoenix, Arizona installed

face recognition video surveillance as a pilot program for tracking missing children and

registered sex offenders. It has split the community, but is supported by many in favor of

it as a potential way to tracking abductors and child molesters.

2.4 The Internet revolution in video Surveillance

The internet has enabled video surveillance to be instituted virtually anywhere

and be watched from anywhere in the world. With satellites bouncing signals around the

globe, one can now watch anyone anywhere from the laptop. The eye in the sky is a

reality with digital streaming video. Sadly, the least common denominator in streaming

video is the peck-a-boo industry of porn sites that have proliferated on the web, but these

real time streaming videos use the same technology as many genuine surveillance

operations.

Streaming videos is set up as a remote system so that you can monitor your site from

anywhere in the world with internet access because the images are video archived on a

remote web server. The quality is outstanding with high compression (1800:1 in some

cases) for storage and features like motion-activation and email alerting when there is activity if you wish. The Internet has truly revolutionized video surveillance by removing all boundaries for viewing anywhere in the world.

2.5 What does the future hold for video surveillance?

The newest trendy, must have fun gadget for consumers, these days is the picture phone that can instantly send snapshots and streaming video to family and friends with just a click. What those fun television ads don't say is that those telephones can just as easily be used for video surveillance. Nearly everyone has a cell phone in their hands these days, so someone standing on a street corner is so unremarkable that virtually anyone could be filming you without your knowledge.

Rather than mounting obtrusive cameras, future law enforcement agencies may begin using these phones as integrated devices, combining video surveillance with public phones in one package for 24/7 public watch dogging. Police officers and federal agents may eventually be issued phones with streaming video so that they can immediately send pictures of suspects they are trailing back to a database for matching against a face recognition program. When new Amber alerts are issued, video clips could be sent to all law officers quickly and efficiently.

It is clear that with digital technology and streaming video, we have moved into the era of being able to conduct comprehensive video surveillance and store the resulting evidence indefinitely. We can reach around the world or across the street with surveillance equipment, but we are still making advances as the new video cell phones

clearly illustrate. The future is sure to see even greater strides that will eventually become

part of the history of video surveillance.

Chapter Three Material and methods

3.0 Overview

The major components used in the implementation of this project include:

1. 74HC4052 Dual 4-channel Multiplexer.

2. CD4518 Dual binary up counter

3. SN7445 BCD-To-Decimal Decoder/ Driver

4. NE555 Timer oscillator

5. LM337 and LM317 Three-Terminal Adjustable Positive and Negative voltage

   regulators respectively.

3.1 Multiplexer

A multiplexer is a device that allows digital / analogue information or data from

several sources to be routed unto a single line for transmission over that line to a common

destination.

There are two basic types of multiplexers. These are:

1. The Analog Multiplexer

2. The Digital Multiplexer

The Analog multiplexer can accept analogue/ digital from several sources and route them

unto a single line for transmission over that line to a common destination.

The Digital multiplexer does the same function as the Analog multiplexer: but the digital

multiplexer accepts only digital data and not analog data.

In addition, the term multiplexer was given to an electronic device that time multiplexes

video pictures from numerous cameras unto one VCR.

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3.1.1 74HC4052 Dual 4-channel Multiplexer

The 74HC4052 is a high speed si-gate CMOS device and is pin compatible with the HEF4052B. The 74HC4052 is a dual 4-channel analog multiplexer with common select logic. Each multiplexer has four independents inputs / outputs (pins nYO to nY3 and a common input/ output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin E). When pin E=low, one of the four switches is selected (low impedance ON-state) with S0 and S1. When pin E=HIGH, all switches are in the high-impedance OFF-state, independents of pins S0 and S1.

VCC and GND are the supply voltage pins for the digital control inputs (pins S0, S1 and E). The VCC to GND ranges are 2.0v to 10.0v for 74HC4052. The analog inputs / outputs (pins nY0 to nY3 and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC-VEE may not exceed 10.0V. For operation as a digital multiplexer / demultiplexer, VEE is connected to GND (typically ground).

Table 3.1.1 Function Table

INPUT(1)

E	S1	So	CHANNEL BETWEEN
L	L	L	nYO and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ

H=HIGH Voltage Level

L=low voltage Level

X=don't care

Table 3.1.2 Quick Reference Data

VEE=GND=OV; Tamb=25 °c; tr =tf= 6ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL 74HC4052	UNIT
tpZH/ tpZL	turn-on time E or Sn to Vos	C_L=15 PF; R_L=1kΩ VCC=5V	28	ns
tpHZ / tpLZ	turn-OFF time E or Sn to Vos	C_L=15 PF; R_L=1k VCC=5V	21	ns
CI	Input capacitance		3.5	PF
Cp_D	Power dissipation capacitance per / switch	Notes 1 and 2	57	PF
Cs	Maximum switch capacitance	Independent (Y)	5	PF
		Common (Z)	12	PF

1. Cp_D is used to determine the dynamic power dissipation (PD μW).

$$PD=C_{PD} X Vcc^2 X Fi X N+\sum [CC_L +C_S) X Vcc^2 X Fo]$$ Where:

Fi = input frequency in MHz;

Fo = output frequency in MHz

C_L = output load capacitance in PF;

Cs = Maximum switch capacitance in PF

Vcc = supply voltage in volts;

N = number of input switching;

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$\sum [(C_L + Cs) \times Vcc^2 \times Fo] = $ sum of the output.

2. For 74HC4052 the condition is $V_1 = $GND to Vcc.

Table 3.1.3 Pinning

| PIN	SYMBOL	DESCRIPTION
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	E	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (OV)
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	Vcc	positive supply voltage
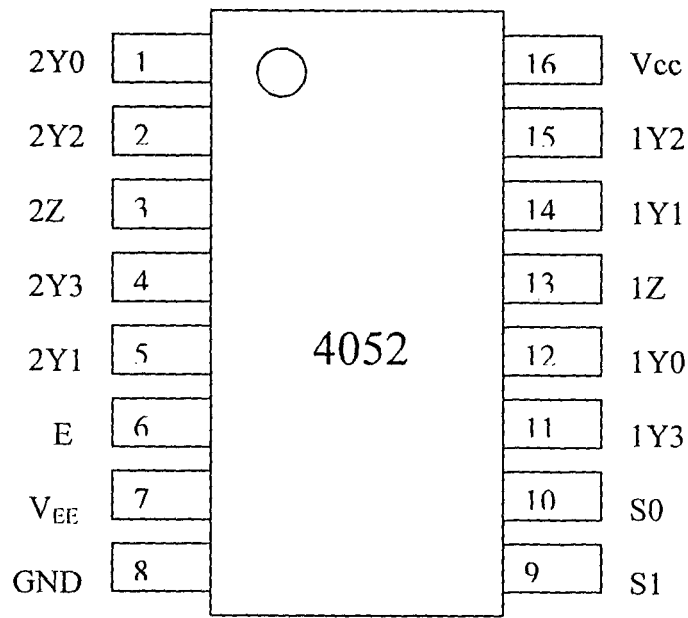
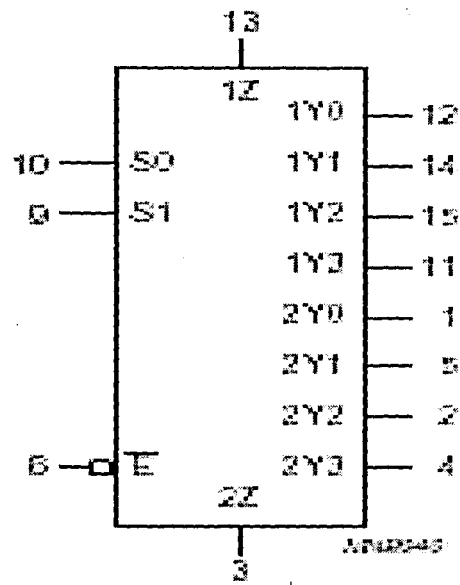Figure 3.1.1 Pin configuration DIP16, SO16.
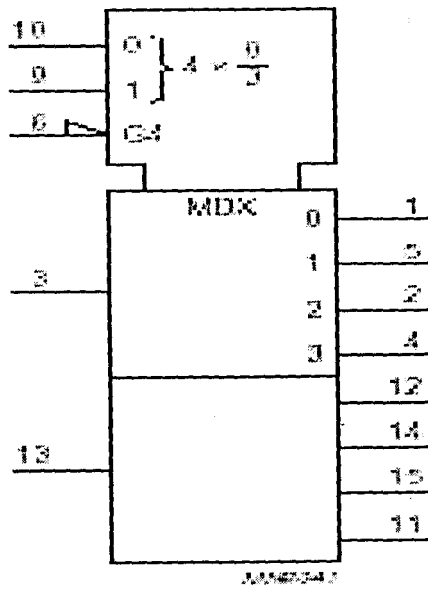

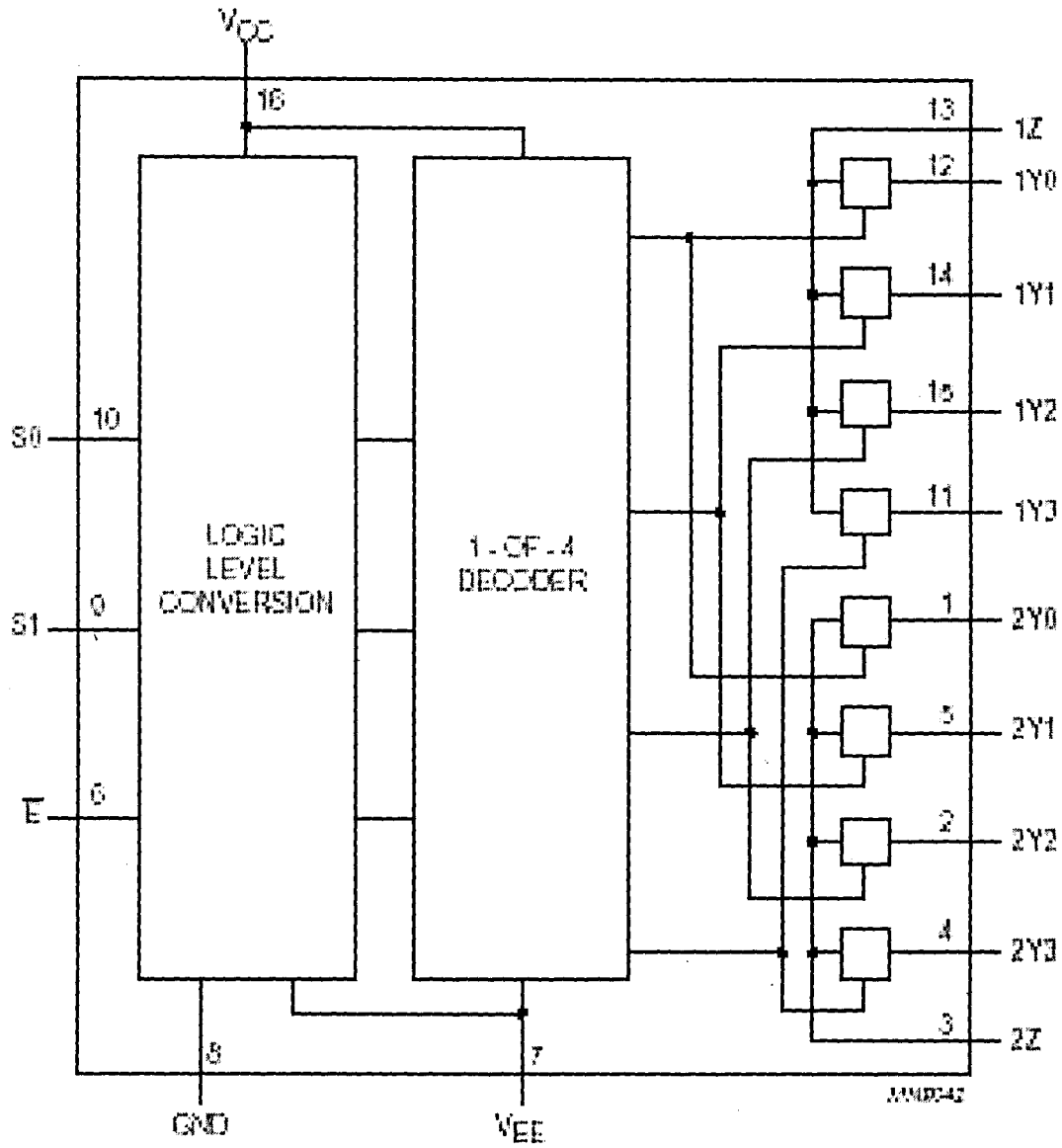Figure 3.1.2 Logic Symbol

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Figure 3.1.3 IEC Logic symbol

Figure 3.1.4 Functional Diagram

Table 3.1.4 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	74HC4052			74HCT4052			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage	see Figs 7 and 8							
		V_{CC} – GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V_{CC} – V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	–	V_{CC}	GND	–	V_{CC}	V
V_S	switch voltage		V_{EE}	–	V_{CC}	V_{EE}	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	–	+125	–40	–	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	6.0	1000	–	6.0	500	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	6.0	400	–	6.0	500	ns
		V_{CC} = 10.0 V	–	6.0	250	–	6.0	500	ns

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3.2 Counters

A counter is a device that counts events or periods of time or put events into sequence. Other functions of counters include dividing frequency, addressing, and serving as memory units.

Flip-flops are wired together to form circuits that count. Because of the wide use of counters, manufactures also make self- contained counters in IC form. Many counters are available in all TTC and CMOS families. The number of flip-flops used and the way in which they are connected determine the number of states (called the modulus) and also the specific sequence of the states that the counter goes through during each complete cycle.

Counters are classified into two broad categories according to the way they are clocked: Asynchronous and synchronous. In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip- flop.

In synchronous counters, the clock input is connected to all of the flips so that they are clocked simultaneously, within each of these two categories, counters are classified primarily by the type of sequence, the number of states or the number of flip- flops in the counter.

3.2.1 Synchronous counters

The term synchronous refers to events that have fixed time relationship with each other. With respect to counter operation, synchronous means that all the flip-flops in the counters are clocked at the same time by a common clock pulse.

A synchronous counter up counter is a counter that counts upward (0, 1, 2, 3, 4...). A counter that counts from higher to lower numbers is called a down counter.

This project makes use of a synchronous counter.
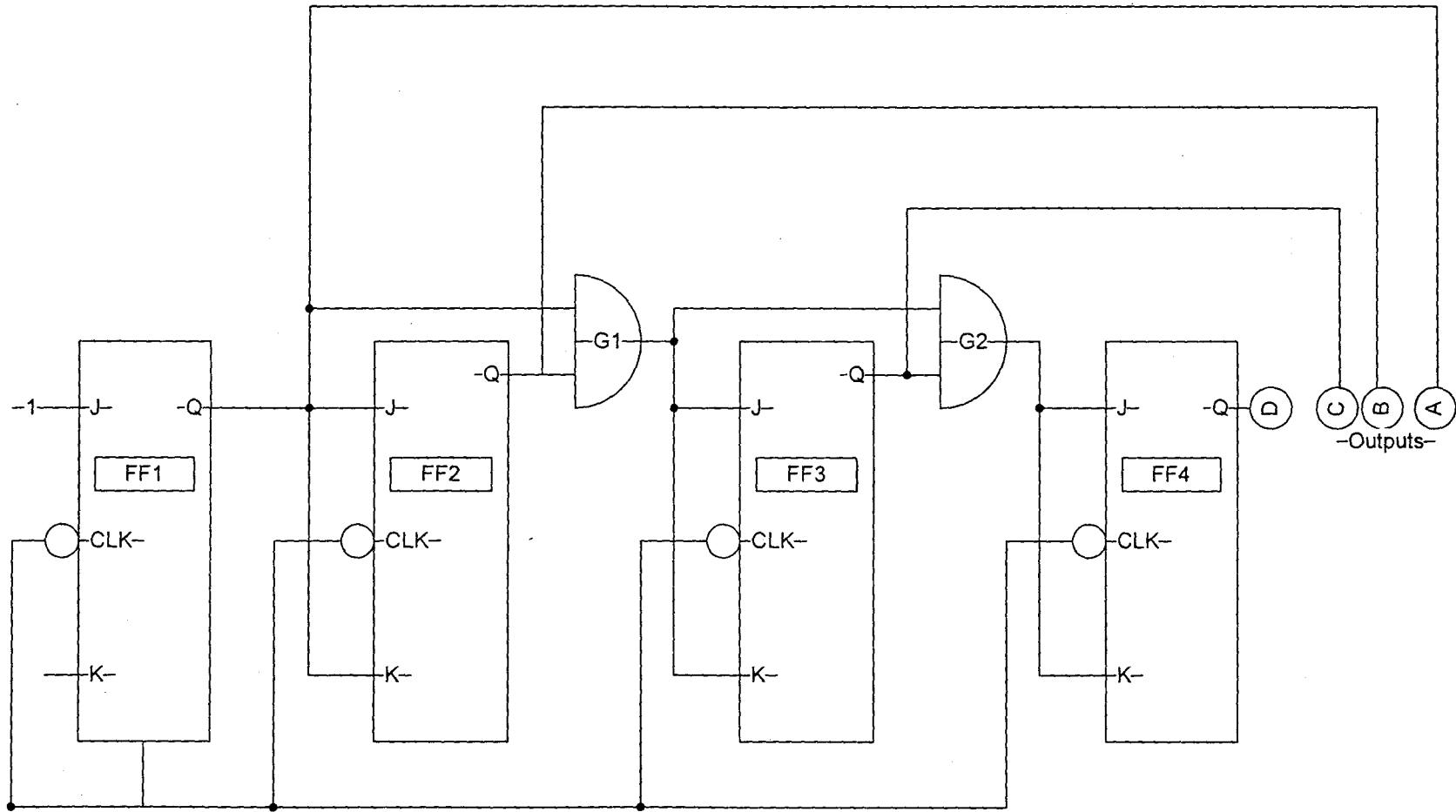
−Figure 3.2.1 A 4-Bit Synchronous Counter−

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Table 3.3.1 Counting Sequence

Row	Number of clock pulses	BINARY COUNTING SEQUENCE				DECIMAL COUNT
		D	C	B	A	
1	0	0	0	0	0	0
2	1	0	0	0	1	1
3	2	0	0	1	0	2
4	3	0	0	1	1	3
5	4	0	1	0	0	4
6	5	0	1	0	1	5
7	6	0	1	1	0	6
8	7	0	1	1	1	7
9	8	1	0	0	0	8
10	9	1	0	0	1	9
11	10	1	0	1	0	10
12	11	1	0	1	1	11
13	12	1	1	0	0	12
14	13	1	1	0	1	13
15	14	1	1	1	0	14
16	15	1	1	1	1	15

The counting sequence of this four bit counter can be explained as follows; with

reference to table 3.2.1

Pulse 1- row 2 ;

Circuit action: each flip flop is pulsed by the clock. Only FF1 can toggle because it is

the only one with 1s applied to both J and K inputs. FF1 goes from 0 to 1

Output result: 0001(decimal1)

Pulse 2 – row 3;

Circuit action: Each flip-flop is pulsed. Two flip-flops toggles because they have 1s

applied to both J and K inputs.

FF1 and FF2 both toggle.

FF1 goes from 1 to 0

FF2 goes from 0 to 1

Output result: 0010 (decimals)

Pulse3 –row 4;

Circuit action: Each flip-flop is pulsed. Only one flip-flop toggles.

FF1 toggles from 0 to 1

Output results: 0011(decimals)

Pulse 4 – row 5

Circuit action: Each flip-flop is pulsed. Three flip-flops toggle to opposite state.

FF1 goes from 1 to 0

FF2 goes from 1 to 0

FF3 goes from 0 to 1

Output result: 0100 (decimal 4)

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3.2.2 CD4518 Dual binary up counter

CD4518 Dual binary up counter consists of two indentical, internally synchronous 4-stage counters. The counter stages are D-type flip-flips having interchangeable clocks and enable lines for incrementing on either the positive –going or negative –going transition. For single unit operation the ENABLE input is maintained high and the counter advances on each positive –going transition of the clock. The counters are cleared by high levels on their RESET lines. The counter can be cascaded in a ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low. The CD4528B type is supplied in 16-led hermetic dual-in-line ceramic packages (F3A suffix), 16-lead in-line plastic packages (E suffix), 16- lead outline packages (M,M96, and NSR suffixes), and 16 lead thin shrink small outline packages (PW and PWR suffixes).

Features of the CD4518 Dual binary up counter are:

1. Medium- speed operation-6MH$_z$ typical clock frequency at 10 volts

2. Positive or negative-edge triggering

3. Synchronous Internal carry propagation

4. 100% tested for quiescent current at 20 volts

5. Maximum input current of 1µA at 18v over full package-temperature range; 100nA at 18v and 25°c.

6. Noise margin (over full package temperature range):

1v at V$_{DD}$ =5V, 2v at V$_{DD}$= 10v, 2.5v at V$_{DD}$= 15v

7. 5v,10v and 15v parametric ratings

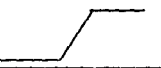8. Standardized symmetrical output characteristics

28
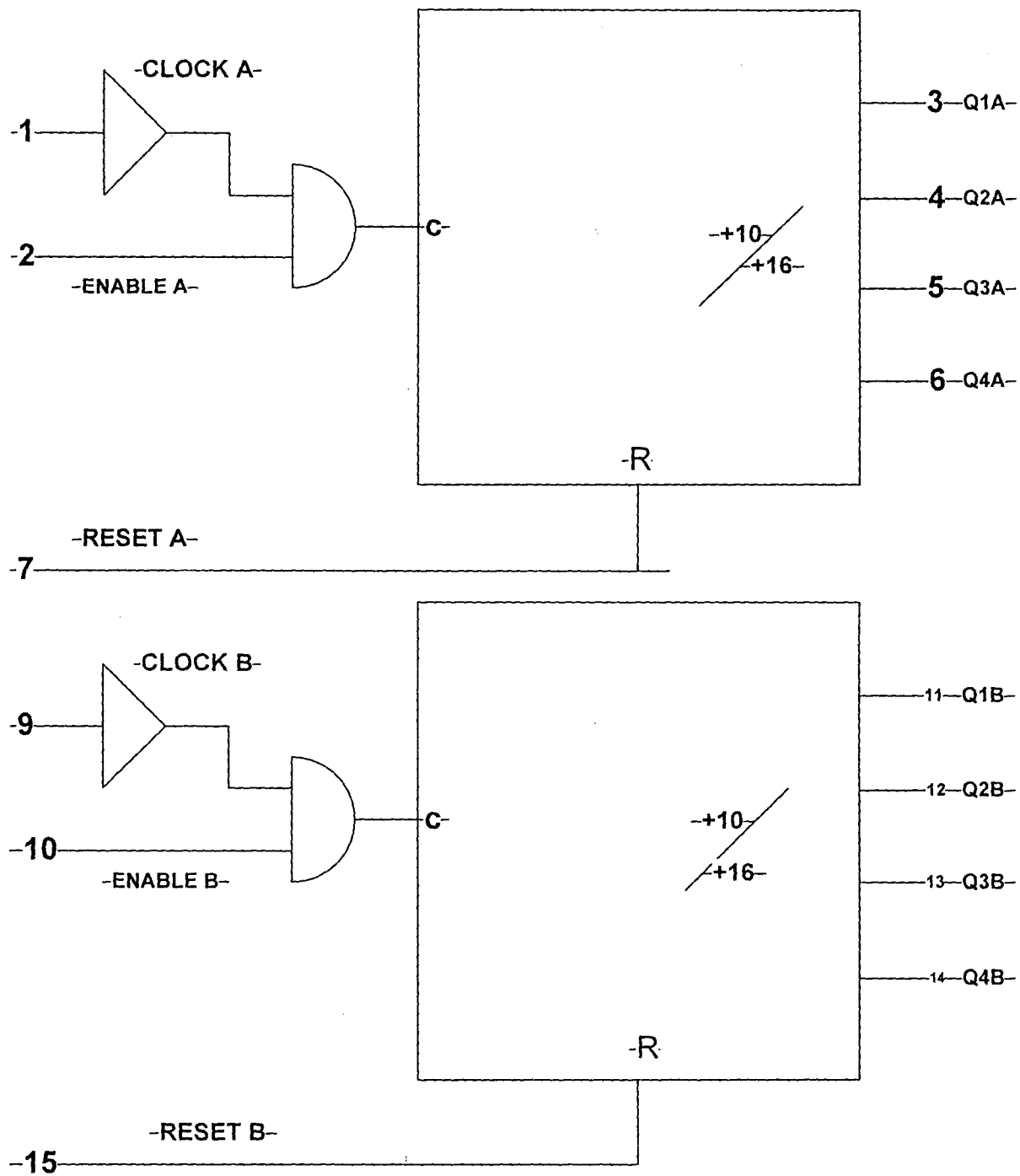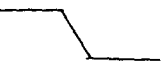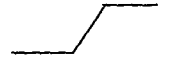
DIAGRAMS FIGURE 3.2.2

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Applications:

1. Multistage synchronous counting

2. Multistage ripple counting

3. Frequency Dividers

Table 3.2.2 Truth Table

CLOCK	ENABLE	RESET	ACTION
⟋	1	0	Increment counter
0	⟍	0	Increment counter
⟍	X	0	No change
X	⟋	0	No change
⟋	0	0	No change
1	⟍	0	No change
X	X	1	Q1 thru Q4 = 0

3.3 Decoder

A decoder is a device that detects the presence of a a specified combination of bits (code) on its inputs and indicates the presence of that code by a specific output level. In its general form a decoder has n input lines to handle n bits and from one to 2^n output lines to indicate the presence of one or more n-bit combinations.

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3.3.1 SN7445 BCD-TO- Decimal Decoder / Driver

These BCD-to- decimal decoder/ driver consists of eight inverters and ten four-input NAND gates. Full decoding of valid BCD inputs logic ensures that all output remain off for all invalid binary inputs conditions. These decoder features TTC Inputs and high performance, n-p-n output transistors designed for use as indicator / relay drivers or as open- collector logic-circuit drivers. Each of the high-break- down output transistor (30V) will sink up to 80mA of current. Inputs and outputs are entirely compatible for use with TTC logic circuits and the outputs are compatible for interfacing with MOS integrated circuits. Power dissipation is basically 215mW.

Features of the SN7445 BCD-To-Decimal Decoder

1. Full decoding of input logic

2. 80mA sink-current capability

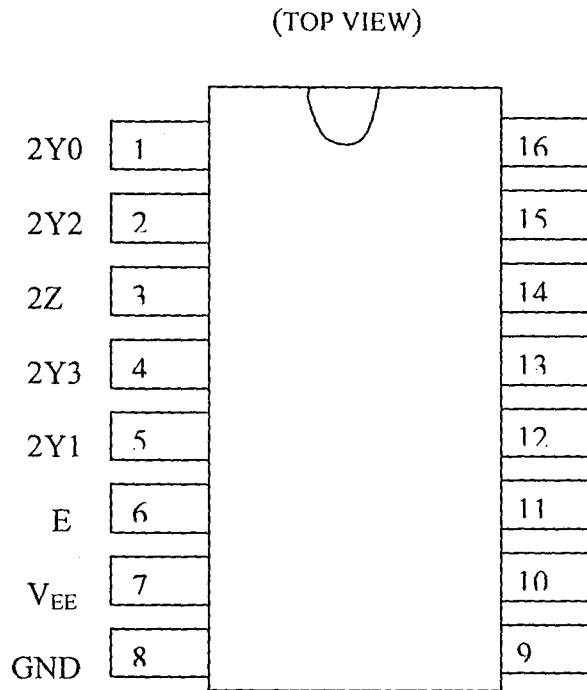3. All outputs are OFF for invalid BCD input conditions
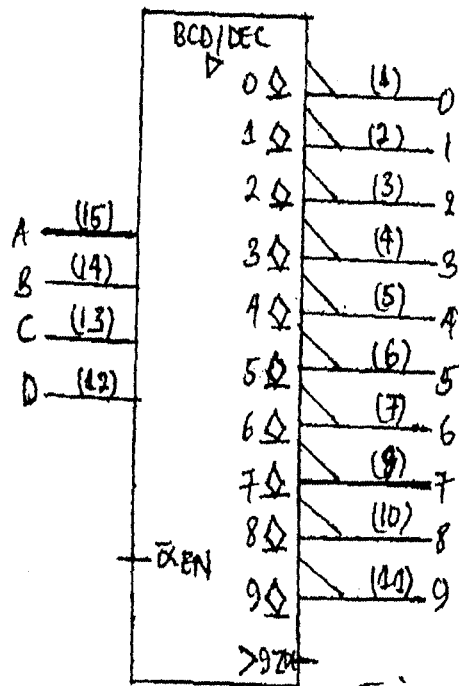
Figure 3.3.1 Pin diagram

Figure 3.3.2 Logic symbol

Absolute maximum ratings over operating free-air temperature range

Supply voltage V_{CC},

Input voltage

Maximum current current into any output (OFF State) --------------- 1mA operating free-air temperature range: SN7445 circuits ---

--- 0^0 C to 70^0 C

Storage temperature range---65^0 C to 150^0 C

Table 3.3.1 Functional Table

NO	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	H	H	H	H	H	
1	L	L	L	H	H	L	H	H	H	H	H	H	H	
2	L	L	H	L	H	H	L	H	H	H	H	H	H	
3	L	L	H	H	H	H	H	L	H	H	H	H	H	
4	L	H	L	L	H	H	H	H	L	H	H	H	H	
5	L	H	L	H	H	H	H	H	L	H	H	H	H	
6	L	H	H	L	H	H	H	H	H	L	H	H	H	
7	L	H	H	H	H	H	H	H	H	H	L	H	H	
8	H	L	L	L	H	H	H	H	H	H	H	L	H	
9	H	L	L	H	H	H	H	H	H	H	H	H	L	
	H	L	H	L	H	H	H	H	H	H	H	H	H	
	H	L	H	H	H	H	H	H	H	H	H	H	H	
	H	H	L	L	H	H	H	H	H	H	H	H	H	
	H	H	L	H	H	H	H	H	H	H	H	H	H	
	H	H	H	H	H	H	H	H	H	H	H	H	H	

3.4 Oscillator

An oscillator is a circuit that creates an AC signal, that is, it converts DC to AC. The only input to the oscillator is a DC power supply and the output is AC. Oscillators can be designed to produce many kinds of waveform such as sine, rectangular, triangular or saw tooth. The range of frequencies that oscillators can generate is from less than 1Hz to well over 10GHz. Depending on the waveform and frequency requirement, oscillators is designed in different ways. Most oscillators are designed in different ways. Most oscillators are amplifiers with feedback. If the feedback is positive, the amplifier may oscillate (produce alternating current).

Applications of oscillators

Examples of oscillator applications include.

1. Many digital devices such as computers, calculators and watches use oscillators to generate rectangular waveforms that time and co-ordinate the various logic circuits.

2. Signal generators use oscillators to produce the frequencies and waveforms required for testing, calibrating, or troubleshooting other electronic systems

3. Touch-tone telephones, musical instruments and remote control-transmitters can use them to produce the various frequencies needed

4. Radio and television transmitters use oscillators to develop the basic signals sent to the receivers.

With respect to this project, the oscillator of interest is the free running or astable mode 555 timer oscillator.

3.4.1 The 555 Timer

The NE555 IC timer has become very popular with circuit designers because of its low-cost and versatility. It is available in the 14-pin dual in-line package and the 8-pin mini DIP. The 555 provides stable time delays or free running oscillation. The time delay mode is RC-controlled by two external components. Timing from microseconds to hours is possible. The oscillator mode requires three or more external components, depending on the desired output waveform. Frequencies from less than 1Hz to 500 KHz with duty cycles from 1 to 99 percent can be attained.

The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

Features of the NE555 Timer

1. Turn-off time less than $2\mu s$

2. Maximum operating frequency greater than 500 KHz

3. Timing from microseconds to hours

4. Operates in both astable and mono stable modes.

5. High output current

6. Adjustable duty cycle

7. TTTC compatible

8. Temperature stability of 0.005% per 0^{0} C.

Applications

1. Precision timing

2. Pulse generation

3. Sequential timing

4. Time delay generation

5. Pulse width modulation.

555 timer configuration for the free – running or astable mode (oscillator):

Figure 3.41 shows the timer configured for the running or astable mode. The trigger (pin2) is tied to the threshold (pin6). When the circuit is turned on, timing capacitor C is discharged. It begins changing through the series combination of R_A and R_B. When the capacitor voltage reaches 2/3 Vcc, the output drops low and the discharged transistor comes on. The capacitor now discharges through R_B. When the capacitor reaches 1/3 Vcc, the output switches high and the discharged transistor is turned off.The capacitor now begins charging through R_A and R_B again. The cycle will repeat continuously with the capacitor charging and discharging and the output switches high and low.

The charge path for the astable circuit is through two resistors and the time that the output will be held high is given by $t_{high} = 0.69(R_A + R_B) C$

The discharge path is through only one resistor (R_B), so the time that the output is held low is shorter $t_{low} = 0.69 (R_B.)C$.

The output waveform is non symmetrical. The total period can be found by adding t_{high} to t_{low}.The output frequency will be equal to the reciprocal of the total period.Or the output frequency can be found with

$F_O = 1/0.693(R_A + 2R_B) \times 10\mu$

The output of the 555 timer is digital, it is either high or low. When it is high, it is close to Vcc, and when it is low it is near ground potential.Pin6 in figure 3.42 is normally connected to a capacitor which is part of an external RC timing network. When the capacitor voltage exceeds $2/3V_{CC}$ the threshold comparator resets the free flip flop to a low state. This turns on the discharge transistor which can be used to discharge the

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external capacitor in preparation for another timing cycle.Pin4, the reset gives direct access to the flip-flop. This pin overrides the other timer functions and pins. It is a digital input and when it is taken low (to ground potential), it resets the flip-flop, turns the discharge transistor, an d drives output pin3 low. Reset may be used to halt a timing cycle. The reset function is ordinarily not needed so pin4 is typically tied to V_{CC}. Once the 555 is triggered and the timing capacitor is charging, additional triggering (pin2) will not begin a new timing circle.

Table 3.4.1.1 DC AND AC ELECTRICAL CHARACTRISTICS

$T_{amb} = 25$ C, $V_{CC} = +5$ V to $+15$ V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SA555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	$V_{CC}=5$ V, $R_L=\infty$		3	5		3	6	mA
		$V_{CC}=15$ V, $R_L=\infty$		10	12		10	15	mA
t_i	Timing error (monostable) Initial accuracy[2]	$R_A = 2$ kΩ to 100 kΩ C=0.1 uF		0.5	2.0		1.0	3.0	%
$\Delta t_i/\Delta T$	Drift with temperature			30	100		50	150	ppm/C
$\Delta t_i/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
t_A	Timing error (astable) Initial accuracy[2]	$R_A, R_B = 1$ kΩ to 100 kΩ C = 0.1 uF $V_{CC} = 15$ V		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature				500			500	ppm/C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	$V_{CC}=15$ V	9.6	10.0	10.4	9.0	10.0	11.0	V
		$V_{CC}=5$ V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	$V_{CC}=15$ V	9.4	10.0	10.6	8.8	10.0	11.2	V
		$V_{CC}=5$ V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	uA
V_{TRIG}	Trigger voltage	$V_{CC}=15$ V	4.8	5.0	5.2	4.5	5.0	5.6	V
		$V_{CC}=5$ V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	$V_{TRIG}=0$ V		0.5	0.9		0.5	2.0	uA
V_{RESET}	Reset voltage[4]	$V_{CC}=15$ V, $V_{TH}=10.5$ V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	$V_{RESET}=0.4$ V		0.1	0.4		0.1	0.4	mA
	Reset current	$V_{RESET}=0$ V		0.4	1.0		0.4	1.5	mA
V_{OL}	LOW-level output voltage	$V_{CC}=15$ V $I_{SINK}=10$ mA		0.1	0.15		0.1	0.25	V
		$I_{SINK}=50$ mA		0.4	0.5		0.4	0.75	V
		$I_{SINK}=100$ mA		2.0	2.2		2.0	2.5	V
		$I_{SINK}=200$ mA		2.5			2.5		V
		$V_{CC}=5$ V $I_{SINK}=8$ mA		0.1	0.25		0.3	0.4	V
		$I_{SINK}=5$ mA		0.05	0.2		0.25	0.35	V
V_{OH}	HIGH-level output voltage	$V_{CC}=15$ V $I_{SOURCE}=200$ mA		12.5			12.5		V
		$I_{SOURCE}=100$ mA	13.0	13.3		12.75	13.3		V
		$V_{CC}=5$ V $I_{SOURCE}=100$ mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	$V_{RESET}=V_{CC}$		0.5	2.0		0.5	2.0	us
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:
1. Supply current when output high typically 1 mA less.
2. Tested at $V_{CC} = 5$ V and $V_{CC} = 15$ V.
3. This will determine the max value of $R_A + R_B$, for 15 V operation the max total R = 10 MΩ, and for 5 V operation, the max. total R = 3.4 MΩ
4. Specified with trigger input HIGH.
5. Time measured from a positive-going input pulse from 0 to $0.8 \cdot V_{CC}$ into the threshold to the drop from HIGH to LOW of the output. Trigger is tied to threshold.
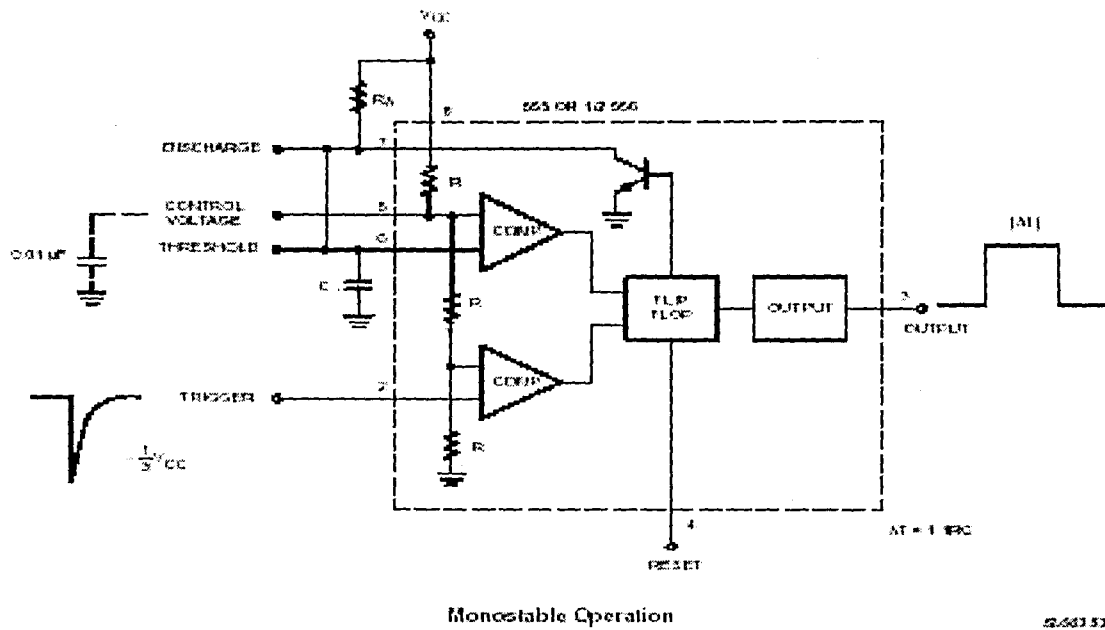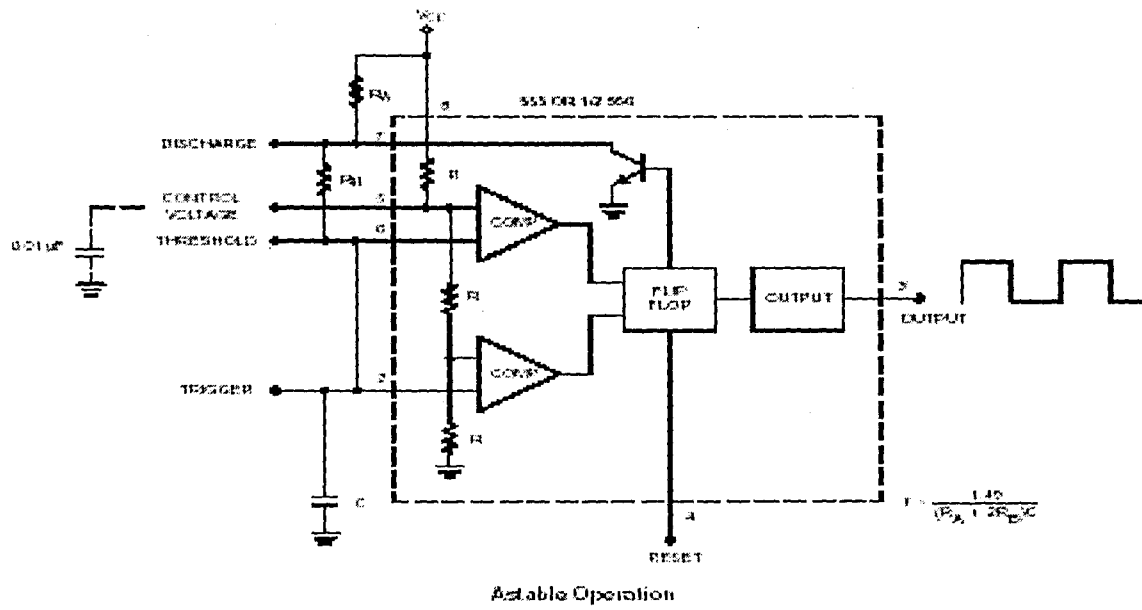
Astable Operation

Monostable Operation

Figure 3.4.1 Typical Applications of Multivibrators

3.5 Regulators

A regulator is a device used to adjust voltage supply which has been stepped down by a transformer to the level desired for a particular circuit operation.

3.5.1 Three-Terminal adjustable output positive voltage regulator-LM317

The LM317 is an adjustable 3-terminal positive regulator capable of supplying in excess of 1.5A over an output voltage range of 1.2V to 37 V.This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage.Further, it employs internal current limiting, thermal shut down and safe area compensation, making it essentially blow-out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator or voltage regulator.

Features:

1. Output current in excess of 1.5A

2. Output adjustable between 1.2V and 37V

3. Internal Thermal overload protection

4. Internal short circuit current limiting constant with temperature

5. Output transistor safe-area compensation

6. Floating operation for High voltage Applications

7. Eliminating stocking many fixed voltages

Table 3.5.1 Maximum Ratings

| Rating	Symbol	Value	Unit
Input-output-Voltage differential	V1—Vo	40	Vdc
Power Dissipation Case 221A $TA= = 25^0 C$	PD	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	OJA	65	$^0C/W$
Thermal Resistance, Junction-to-Case	OJC		$^0C/W$
Case 936 ($D^2 PAK$)	PD	5.0	W
$TA= +25^0 C$			
Thermal Resistance, Junction-to-Ambient		Internally Limited	
Thermal Resistance, junction-to-case.	OJC	5.0	$^0C/W$
Operating junction Temperature range	Tj	-40 to+125	^0C
Storage Temperature Range	Tstg	-65+150	^0C
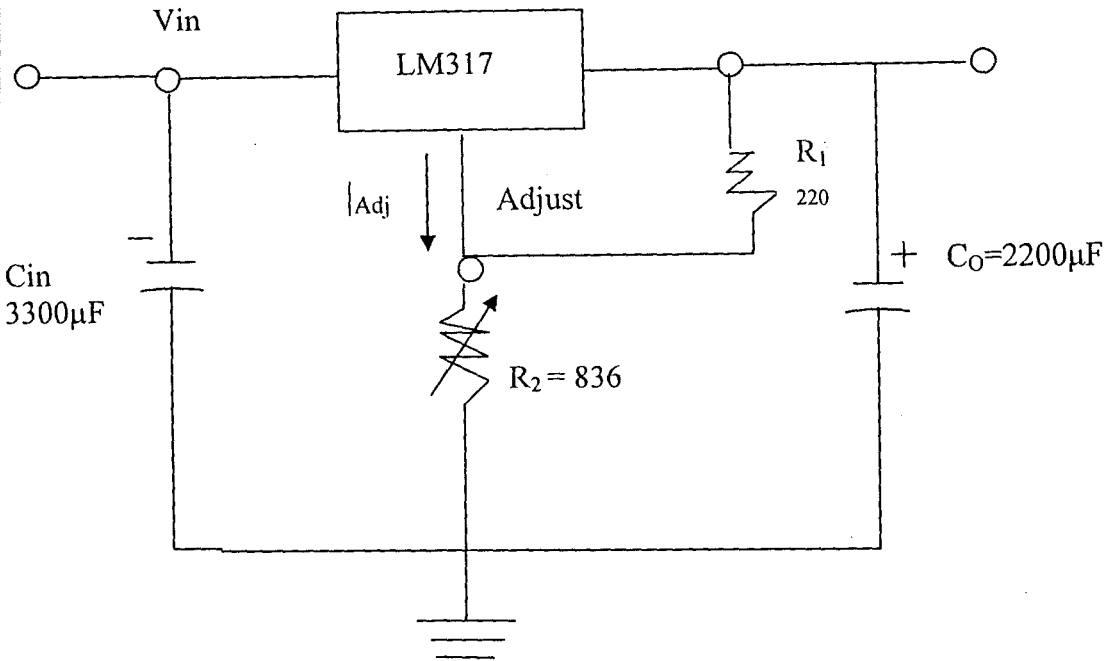
Figure 3.5.1 Standard Application

C_{IN} is required if regulator is located an appreciate distance from power supply filter

C_0 is not needed for stability; however, it does improve transient response.

Basic circuit operation of LM317

The LM317 is a 3-terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 reference (V_{ref}) between it's output and adjustment terminals. This reference voltage is converted to a programming current by R_1 and these constant current flows through R_2 ground.

The regulated output voltage is given by: $V_{out} = V_{ref} \{1 + R_2/R_1) + I_{Adj}R_2\}$ Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317 was designed to control I_{adj} to less than 100µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirements for a minimum load- current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance and operation at high voltages with respect to ground is possible.
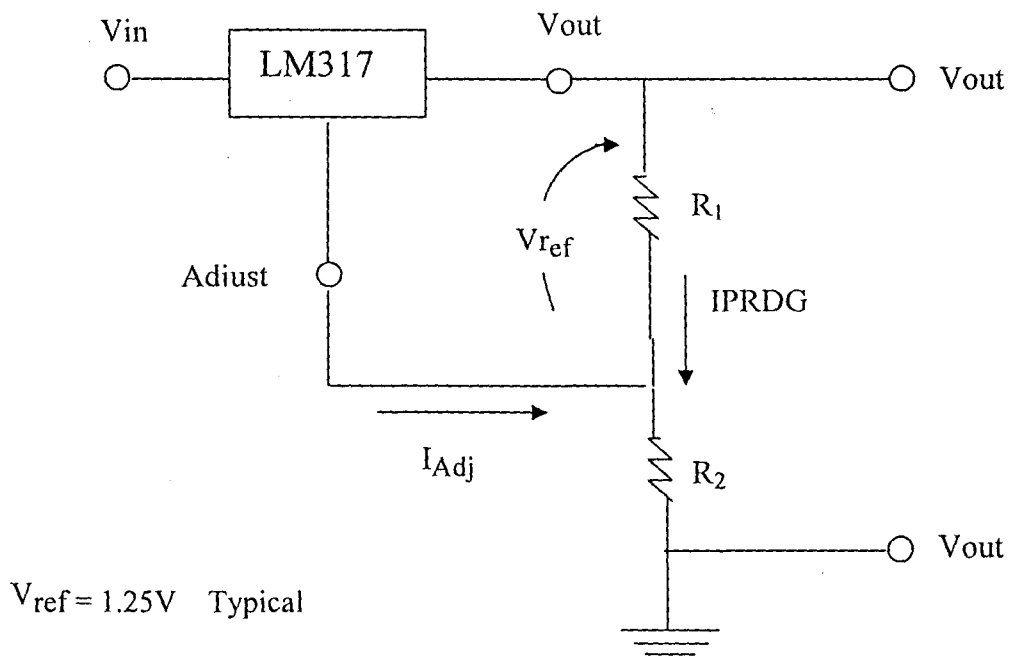
Figure 3.5.2 Basic Circuit Configuration

$V_{ref} = 1.25V$ Typical

Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) is connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 is returned near the load ground to provide remote ground, sensing and improve load regulation.

3.5.2 Three-Terminal Adjustable Output Negative Voltage Regulator – LM337

The LM337 is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 1.5A over an output voltage range of -1.2V to -37V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal short down and save area compensation making it essentially blow-out proof.

The LM337 serves as a wide variety of application including local on card regulation. This device can be also used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator. In this project, the LM337 serves as a precision current regulator or voltage or voltage regulator.

Features of LM337:

1. Output current in excess of 1.5A

2. Output adjustable between -1.2V and -3.7V

3. Internal thermal overload protection

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4. Internal short circuit current limiting constant with temperature

5. Output transistor safe-area compensation

6. Floating operation for High voltage Applications

7. Eliminate stocking many fixed voltages

8. Available in surface Mount D^2 PAK and standard 3-lead Transistor package.

Basic circuit operation of LM337

The LM337 is a 3-terminal floating regulator. In operation, the LM337 develops and maintains a nominal -1.25 reference (V_{ref}) between it's output and adjustment terminals. This reference voltage is converted to a programming current by R_1 and these constant current flows through R_2 ground.

The regulated output voltage is given by: $V_{ref} = V_{ref} \{1 + R_2/R_1) + I_{Adj}R_2\}$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337 was designed to control I_{adj} to less than 100µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirements for a minimum load- current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) is connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground, sensing and improve load regulation.

Chapter 4: Project Construction

4.0 Introduction

This project work is designed around two multiplexes (CD4052BE), two CMOS

Synchronous up Counters, an NE555 square wave Oscillator, and two SN7445 BCD-

Decimal Decoders/Drivers.

The whole work can be subdivided into five subsections. These subtions are:

1. Video Switching/Multiplexing System

2. The 2-bit binary address Generator

3. An 0.5HZ adjustable scan rate generator

4. Dual 1-of-4 Led Drivers

5. Power suppliers

4.1 Video Switching/ Multiplexing

The input stage of the video switch is built around 2 dual 1-of-4

multiplexers/demultiplexers. Four (4) video inputs from four surveillance cameras are

connected to each of the four inputs on the half-sections of the two analog multiplexer.

(Only half the circuit in each chip is used). The video inputs are terminated into a

standard 82 ohms input impedance as demanded for a video signal. Each video input is

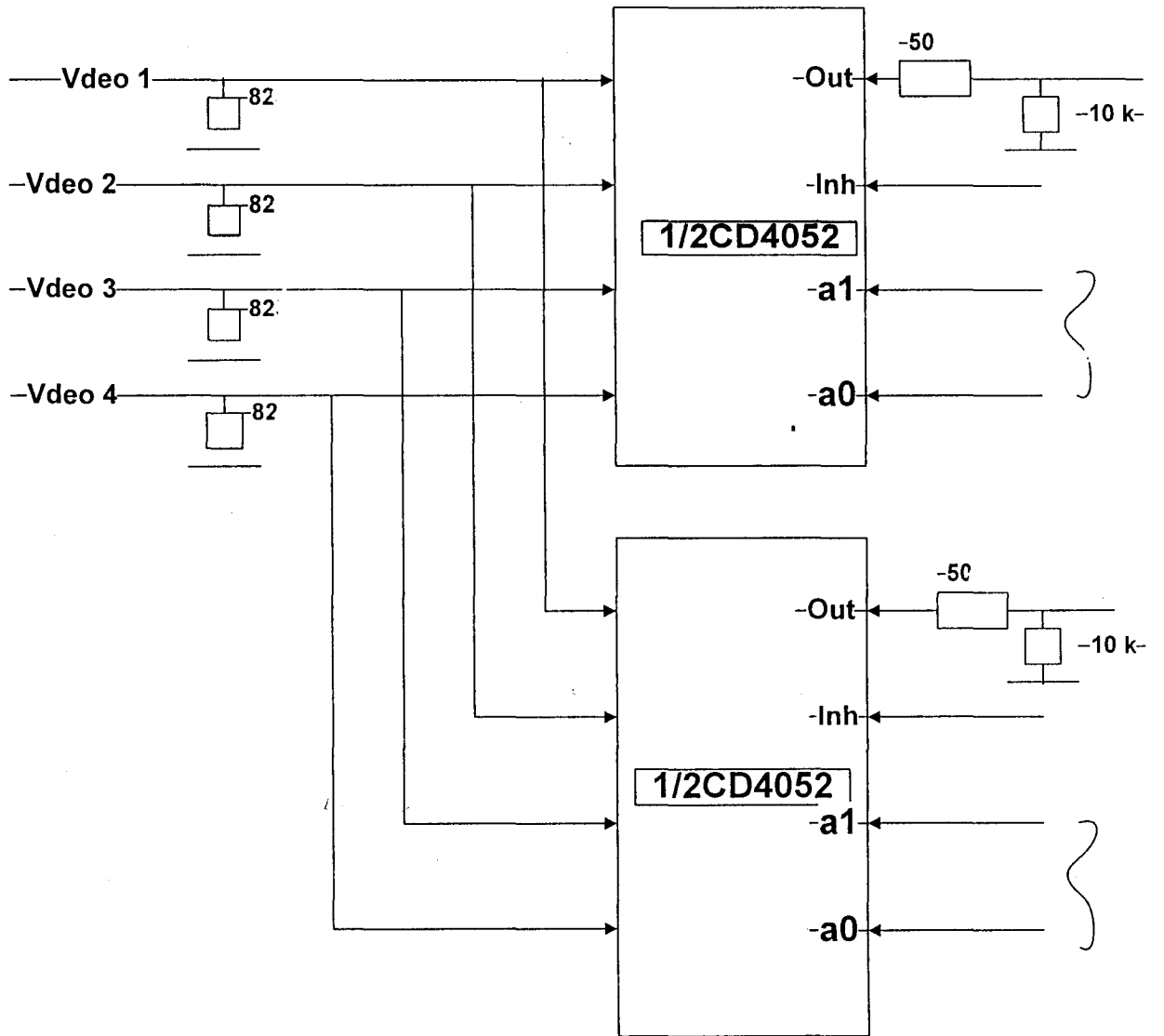routed through the multiplexers separately as depicted in figure 4.. 1

Figure 4.1(a) (multiplexed switching)

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One multiplexer is driven by a CD4518 clocked by the scan rate generator and the other multiplexer is driven by the second pair of the CD4518 clocked manually. This arrangement yields a switching system with two outputs; an auto select output and a manual user selectable video output. This scheme is adopted so that a particular camera can be specifically monitored while still keeping a running display of the outputs of the four cameras.

The inhibits inputs of the CD4052BE multipliers are tied low to enable multiplexer action and the two devices are run off ±7.5V.

The video inputs are selected sequentially by the 2 bit addresses generated by the up counters. The multiplexers are terminated into 50 ohms output impedance as is also needed for video applications.
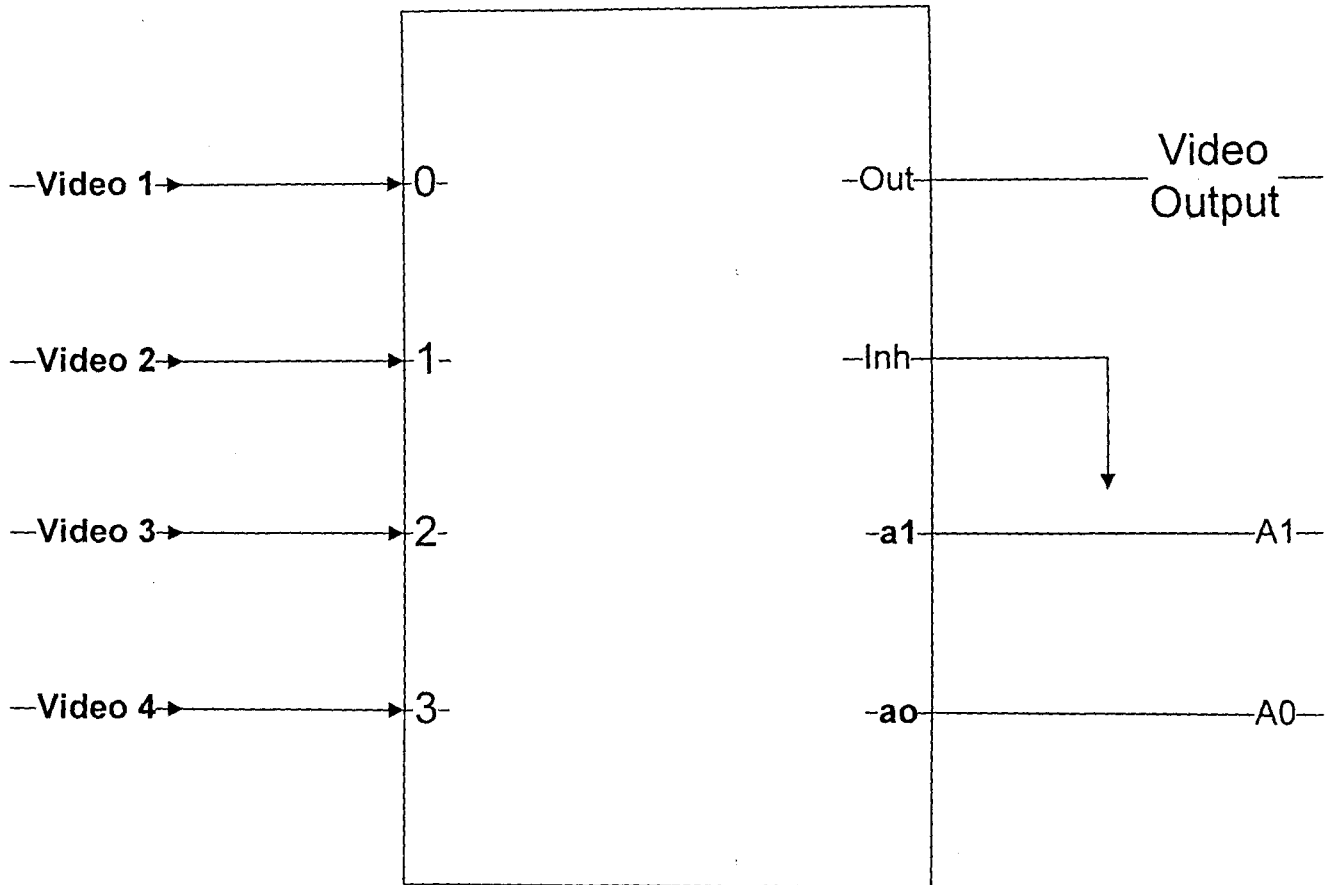
Figure 4.1(b).Multiplexer Switching

Table 4.1 Truth Table.

Table 4.1

address	lines	Selected video output
a_1	a_0	
0	0	Video 1
0	1	Video 2
1	0	Video 3
1	1	Video 4

Sequential feeding of the different address combinations connects different inputs to the output.

4.2 Binary Address generators

Binary address generator is built around a CD4518 dual 4-bit Synchronous up counter. One half of the counter has its clocking circuitry driven by the output of the NE555 scan rate clock/generator. The output of the counters are 4 bits : (0000 ~ 1111), though only the first four bits combinations are used(0000~0011).

One multiplexers is addressed by the counter driven by the scan rate generator, while the other multiplexer is addressed by the manually clocked counter. Both counters are reset on the 3-4 count, to 00, to repeat the 0-3 count loop.

Table 4.2 Binary counting sequence

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Reset to 0000 →

4.3 Scan rate generator

The scan generator is designed around the generic 555 timer.

$$F = \frac{1}{0.693 \, (RA + 2RB) \times C}$$

$R_B = 47$kilo ohms for case 1 and
$R_B = 104,000$ for case 2

To allow for display of different number of frames per second. The frequency generated by the 555 is designed to be variable by the inclusion of a 100 kΩ variable resistor in the R_B component of the calculation of the frequencies.

With the value given above, twp extreme values of F are calculated from

$1/0.693 \times (10000 + 94000) \times 10\mu$ Hetz

The first calculaton is done with the variable resistor at set at 0Ω resistance, in this case, frequency (F) is calculated as: $F = 1/ 0.693 \, (10000 + 94000) \times 10\mu$ (Hetz)

$$F = 1.5H_Z$$

The other frequency B if generated with the variable resistor set to maximum resistance that is 100kΩ. In this case, frequency is calculated as:

$F = 1/ 0.693(10000 + 2 \times 104k) \times 10\mu;$ $F = 0.66H_Z$

As can be deduced from the calculations, varying the values of the 100kΩ variable resistance varies the generated frequency, and hence the rate at which the auto-scan multiplexer is addressed.

4.4 Led Drivers / BCD-Deecimal Decorders

To give a visual indication of the selected video source, the outputs of the two counters are separately fed into the inputs of two SN7445 BCD-to-Decimal recorders/drivers.

These drivers provide full decoding full decoding of the 4-bits input logic, 80-mA sink-current capability, and an all output off for invalid BCD input conditions.

The two 2-bit address inputs from the counters are separately into the SN7445 BCD-decimal decoder / drivers.

These drivers provide full decoding of the 4-bit input logic; 80mA sink current capability, and an all output off for invalid BCD input conditions. The two (2) bit address inputs from the counters are separately fed into the SN7445. The activated output is a function of the logic combination fed into the decorder. The truth table is given as shown in table 4.4.

Table 4.4. Truth Table

	Inputs				Outputs									
NO	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0
	1	0	1	0	All Outputs are at a logical 1, i.e. no output is activated									
	1	0	1	1										
	1	1	0	0										
	1	1	1	0										
	1	1	1	1										

Inputs C and D on the two decoders are tied to logic 0, so that the binary combination presented to the decoders range from 0000 to 0011, before rolling back to zero to repeat the input sequence.

4.5 Power Supply

The power supply is built around two adjustable positive / negative regulators; the LM317T and the LM337T. The former is a 1.5 ampere, 1.2-37V, 3-pin adjustable positive regulator, while the latter, the 337 embodies the total specifications of the 317, except that the ratings are in the negatives, rather than positive.

The two regulators are adjusted by preset trimmer resistors to generate precise ±6v needed to power the circuit. The inputs are from a dual output rectifier system with heavy filtering of the output voltage.

POWER SUPPLY

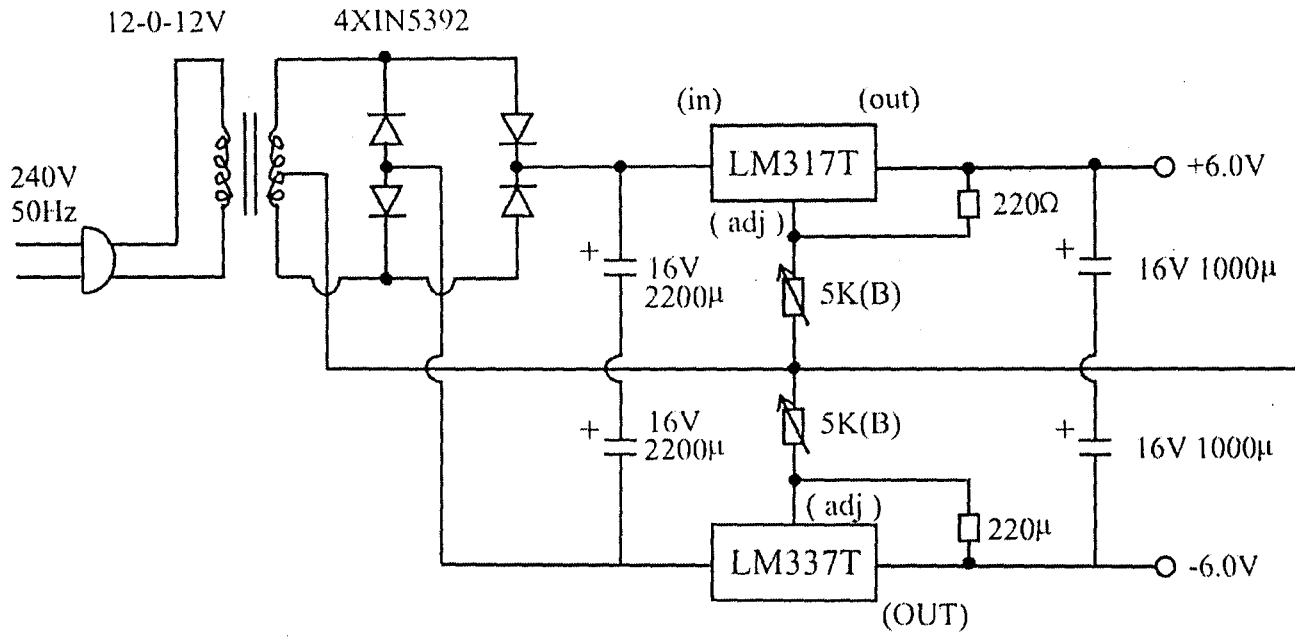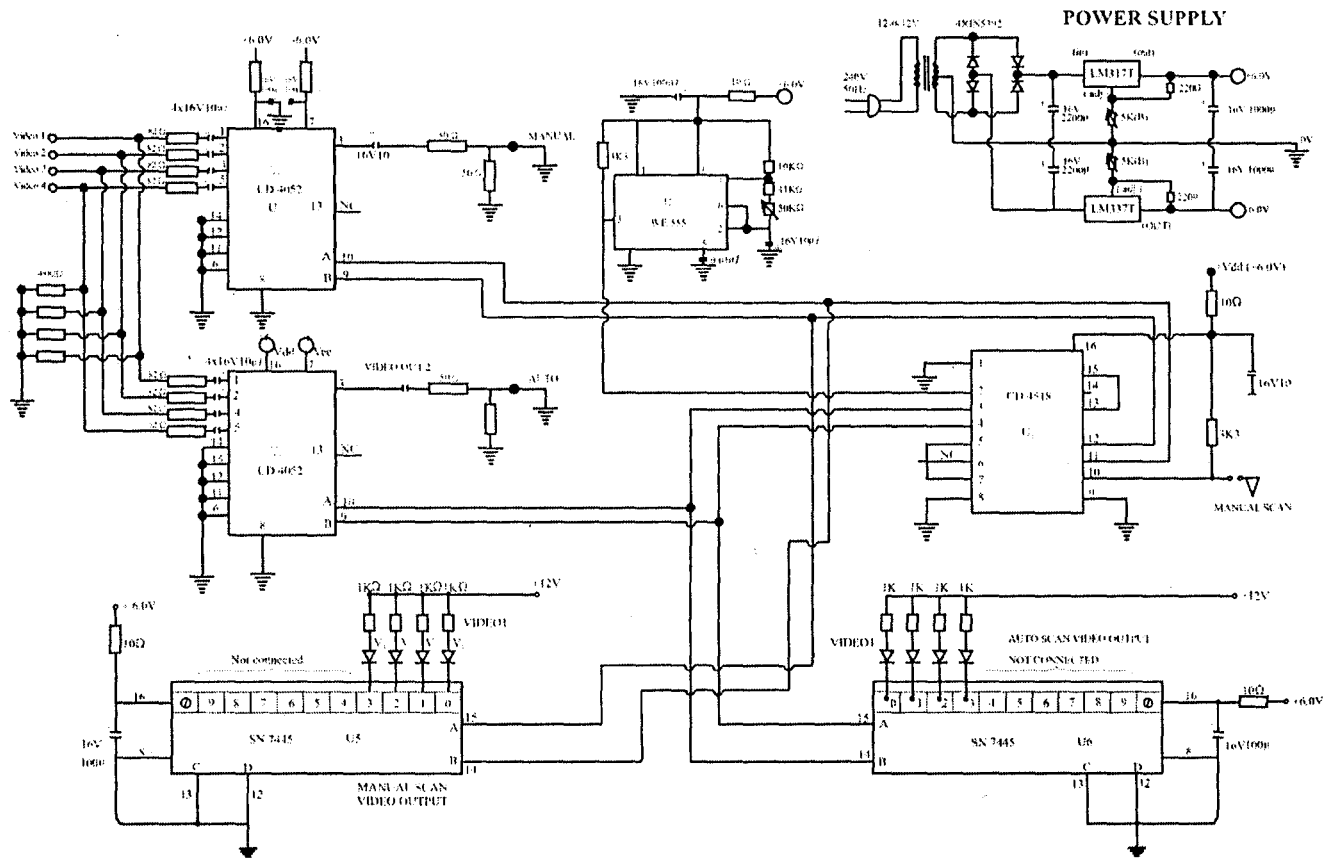Figure 4.5 . Power Supply Circuit

VIDEO SWITCH CIRCUIT DIAGRAM

Figure 4.6: Video Switch Circuit Diagram.

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Chapter Five

5.0 Conclusions

The project, four camera video surveillance with multiplexed switching have been successfully designed and contructed. The project have also been tested and confirmed to work according to specifications or stated objective. The project makes use of four input channels and two output channels that is automatic and manual. The multiplexer a[application in this project have been fully explored and the workability and fuctionity demonstrated and confirmed okay. For the sake of emphasis, this project is subdivided into five subsections, that is:

1. Video switching / Multiplexing System

2. Two Bit binary address generator

3. An 0.5Hz adjustable scan generator

4. Dual 1-of-4 Led drivers / Decorders

5. Power Supplies

Limitations

Though a feasible design, this project work has its own inherent limitations. These are:

1. Two television monitors are needed for actualization of the two modes of operation: Manual / Automatic.

2. The switching System is connected to the four video sources by wires.

3. There is no log of previous scans, that is no history that can be referred

5.1 Recommendations

To overcome the first limitations, a scheme that displays the four video frames at the same time on the same screen should be implemented. This demands the use of a Duplex or Triplex multiplexer.

The second limitations can be overcome by employing a wireless scheme whereby each video source is sent to the switch as a modulated RF signal. This permits remote monitoring of events without the encumbrance of wiring. Limitation three can be eliminated by storing previous scan fames in non- volatile memory. This can be stored on video tape machine or digital recorder.

5.2 References

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