DESIGN AND CONSTRUCTION OF AN ELECTRONIC DOOR LOCK

BY

AKINNIRAN MOHAMMED

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DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

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NIGER STATE NIGERIA

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PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE ELECTRICAL/COMPUTER DEPARTMENT OF THE FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA-NIGER STATE, NIGERIA.

NOVEMBER 2004.

DECLARATION

I hereby declare that this project (electronic door lock) was constructed by me under the supervision of Mr. A. U. Usman; a lecturer in the department of electrical/computer engineering, Federal university of technology, Minna.

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MR. A.U. USMAN **Date**
Project supervisor

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AKINNIRAN MOHAMMED **Date**
Student

CERTIFICATION

This is to certify that this project **ELECTRONIC DOOR LOCK** was designed and constructed by Akinniran Mohammed for the partial fulfillment of the award of Bachelor degree in electrical/computer engineering.

MR. A.U. USMAN
Project Supervisor

7/12/04
Date

ENGR. M.D. ABDULLAHI
H.O.D

31/01/2005
Date

External Examiner

Date

AKINNIRAN MOHAMMED
Student

7/12/04
Date

DEDICATION

This project is dedicated to the Almighty Allah who saw me through my course of study and especially through this project work.

ACKNOWLEDGEMENT

Praise be to Almighty Allah for seeing me this far and for the good things He has been doing and He is still planning to do in my life. I say a big thanks to the Almighty Allah for His immense grace on me and for His protection and guidance throughout my academic pursuit.

Also, I cannot but say thanks to my daddy and mummy, Alhaji and Alhaja M.O. Aknniran, for their spiritual, moral, and financial support. And to my brothers and sisters, I say thanks for they are always there for me.

I express my profound gratitude to Mr. A. U. Usman who supervised my project work and gave me professional advice and technical guidance on my project work. He also made time available to meticulously scrutinize this project work despite his tight academic schedule.

I which to also thank the H.O.D, Engr. M.D. Abdullahi and all other staffs in the department for their guidance in the different academic works they taught me and made electrical engineering an interesting field of study.

I thank all my colleagues and friends who either consciously or unconsciously encouraged me in the course of my career and in the accomplishment of this project.

May the Almighty Allah reward you all (Amen).

ABSTRACT

An electronic lock is used to open or close a lock depending on electronic logic applied to the motor terminal as described here. To open a lock, four digits stored in a memory latch must be entered in the correct sequence by first pressing the reset push button switch and using the two other push button switches. If any of the digits is entered wrongly, the circuit will not open after inputting the four decimal digits. If you continue to press and release the two other push button switches to enter another set of four decimal values without first pressing and releasing the first push button switch, the lock will not open if the right code is now entered. The sequence of decimal numbers stored in a memory latch can be changed as frequently and easily as possible, providing a higher security level to this electronic lock device. The change of the decimal number stored in the memory latch (4076B) can only be effected when the door is opened and a fourth push button switch is pressed and released.

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CHAPTER ONE

1.0.0 GENERAL INTRODUCTION

1.1.0 INTRODUCTION

The goal of every nation is to develop into a most prosperous nation. If any nation is to undergo developmental process, its security must be given the topmost priority it deserves. Security as a basic subject has a global impact on any nation, lack of it goes a long way to tell its effect on us whether it would be on humanity or otherwise. It affects all areas of life and without it life becomes unbearable. Humanity owes its present relatively comfortable standard of life and expectation of further advancement to security. With the advancement in technology, the problem of security consciousness has increased. The process of security changes have been going on for million of years and will continue due to the advancement in technology. In recent times, the use of key operated locks for doors have been unreliable with the various nefarious activities of the intruders which include taking impression of key, picking of keyholes with picking tools or by the use of the so called master key. In addition, lost (misplacement) and the theft of key are problems associated with key operated locks.

The most modern keyless locks have different problems associated with them. For the card operated lock, the cost of the lock and the cost of printing of the card used, makes it unaffordable to everybody. Also the lost of the card or the breakage of the card will deny the owner access from entering the building. For the remote control lock, the

cost of the lock is a problem while the misplacement of the control unit of the lock denies the owner access to the building.

It is against this background of the reliability of the key operated locks and the problems associated with the keyless locks that the electronic door lock was designed to solve the stated problems. Apart from the ability of the lock to solve these stated problems, it has the property of being cheap and the ability of changing the password easily and frequently at no cost. The ability to change the password improves the security of this lock.

The device is a digital circuit made up of different CMOS ICs. This device make use of CMOS ICs because of its wide operating voltage range (+3Vd.c to +18Vd.c) of this IC technology, its reduced power consumption. The device consists of the following IC chips namely the up/down counter (4029B) which provides the number to be stored in the memory or required to open the lock, two types of memory ICs were made use of namely the 4-bit registers (4076B) and the D-latch (4013B) and these are used to store information (binary code) by latching the information and holding it for as long as necessary; the oscillator (4060B) output is required to clock the up/down counter to count, a Johnson decade counter (4017B) required to control the operation of some other ICs which open or closes the lock. The comparator unit comprising of the exclusive-OR gate (4070B) required to compare the inputted decimal numbers with the stored values and activate the required circuitry to open or close the lock, the seven segment display which shows the decimal number being inputted via the BCD-to-7-seggment decoder (4511B) and other devices that are not integrated circuits such as the light emitting diode which serves as indicator for different purposes, the push button switches required to

send pulse as and when required (by the closing of its electrical contacts) to some ICs, the motor which rotates the knob connected to its armature depending on the polarity of its terminals to close or open the lock and the transistor (2SD400) used for switching purpose.

1.2.0 LITERATURE REVIEW

Lock is a device that secures such things as a door of a house or cabinet, brief case or other luggages and the action of an ignition system by means of a bolt or a latch that can be released by a mechanical, hydraulic or electric/electronic actuator. It is a device widely used to protect property/information from thieves and intruders. A lock is operated by a key, in the case of the combination by the dealing the correct sequence of position, electronic lock responding to an electronic logic to open it, remote control lock by using its remote control unit and the card operated lock by using the right card.

Mechanical locks were developed by the Egyptians about 2000 B.C. These locks were made of wood and contained pegs that fell by the gravity into the corresponding holes in the lock bolt. This is the first known lock found in the ruins of the Near Eastern palace of Khorsabad near ancient Ninevah. It is the forerunner of the modern pin tumbler lock. The Greek used a simple lock in which a notch was moved by a large-sickled shape key. The Romans developed warded locks, the first metal locks. In Europe skilled locksmiths devised ingenious variations of locks and adorned them with elaborate decorations.

The principle of combination lock probably originated in china, it appeared in southern Germany in the 16th century and resurfaced in England in the following century. The familiar combination lock works without any physical key but with dealing the

correct sequence. The combination lock mechanism consists of three or more slotted rings connected to a graduated dial. In order to open the combination lock, the correct series of position is dialed. By this process the slots are aligned, allowing the bolt to be released.

The security provided by the modern locks began in the 18th century, when the pin tumbler lock was invented by Linus Yale and Linus Yale Jnr. The senior Yale patented (1851) a lock with a radial pin tumblers, his son patented improvement and began manufacturing the lock. Great modern advances made in lock security involve the use of multiple tumbler and this form the basis of most locks made.

The advancement in the technology made machine tools and manufacturing methods become more sophisticated, locks were produced with closer part tolerance resulting in better security. Locks were later combined with burglar alarm systems that automatically fires a steel relocking bolt into the door jam when a foreign key was inserted. In 1883 George Lush Pearson applied for a patent for his invention which would alarm by means of electric communication. This was initially a revolving lamp in the exterior of the protected premises or the use of bells. It was not however until 1923 the intruder alarm became generally available, since that time lock equipment have been designed which uses the principles of ultrasonic, microwave, infrared light, television current monitored wiring, magnetic recorders, pressure pads, vibration sensors, capacity sensors, microphone, many type of switches and electronic security system.

Today new security technologies threaten the dominance of the metal lock and key. The key card developed in the early 1980's for use in the hostels, is a small credit card that holds coded information that is magnetically imprinted allowing a guest to enter

the rented room. The code is changed when the person checks out. The keyless locks are the most recent of the modern locks. They include remote control lock, card operated lock and the electronic lock which this project write up is all about.

1.3.0 PROJECT LAYOUT

This project write up is divided into four chapters for easy comprehension of what the project is all about.

Chapter one consist of the introduction which present a brief insight to the main concepts behind the work, the aim and objective of carrying out this project, the literature review showing previous or related works that have been done on this project and the project outline showing the division of the project work into chapters.

Chapter two consists of the system analysis and the design which gives a clear description of the step by step design of the project work with the aid of truth tables and pin assignment diagram which aid better understanding of the project.

Chapter three consist of the working operation which shows the principle on which this lock works on and how to use it, the construction aspect, the testing and result/inference. In this chapter all the technique used in combining the different IC components and the passive component to the realization of the circuit diagram of the project work was discussed. Testing procedures as well as result and inference deduced from the test performed were also discussed in this chapter.

Chapter four, the last chapter consists of the recommendation which provide suggestions for the improvement of this design work and conclusion which shows what have been achieved from doing the project work.

CHAPTER TWO

2.0.0 SYSTEM DESIGN AND ANALYSIS

2.1.0 GENERAL OVERVIEW

In this project design, complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) were chosen for all the ICs used because of its wide operating voltage of between +3Vd.c to+18Vd.c, its reduced power consumption and its low price value. Also CMOS devices do not need the voltage to be closely regulated as its transistor-transistor logic (TTL) counterpart.

The circuit is a digital circuit as against an analogue circuit, since digital circuits are used as switching circuits where exact values of voltages and currents are not important, only the range (HIGH or LOW) in which they fall. Information storage is also easy. This is accomplished by special switching circuits that can latch onto information and hold it for as long as necessary.

The low power consumption of this device makes it to be powered from a battery since it does not make unusual demand on power supplies because of its minimal requirement for supply current (only a few microampere on quiescent state). This battery is required in case of power outage making it reliable.

In order to analyse the entire circuit, it was broken down into eight broad subsystems namely, power supply unit, the input unit, the digit indicator unit, the password enable unit, the control unit, the memory unit, the comparator unit, and the output unit. Each of these subsystems was further divided into modules to ease design and enhance simplicity.

The block diagram for the electronic door lock is shown in fig.2.0 below

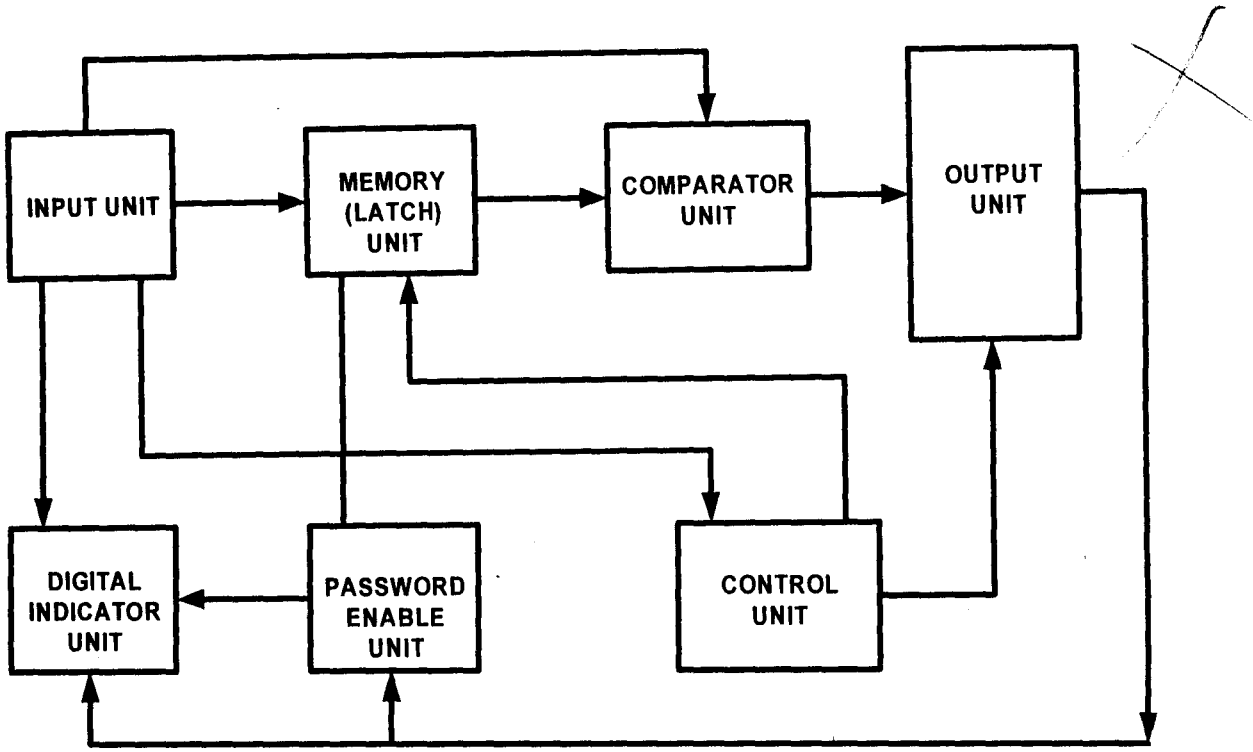


Fig. 2.0 Block diagram for the electronic door lock

2.2.0 POWER SUPPLY UNITT

All electronic circuits rely for their operation on the availability of power supply; the electronic door lock is no exception.

The necessary power supply for most electronic circuit is direct current (d.c) and this may be drawn from battery or obtained from alternating current (a.c) mains.

The power supply of this device is essentially an a.c to d.c converter, together with a 9V battery in case of power failure. The electronic door lock requires a voltage between +3Vd.c to +18Vd.c for its operations since the ICs used in this device are CMOS ICs.

The circuit diagram of the power supply unit is shown in fig 2.1 below

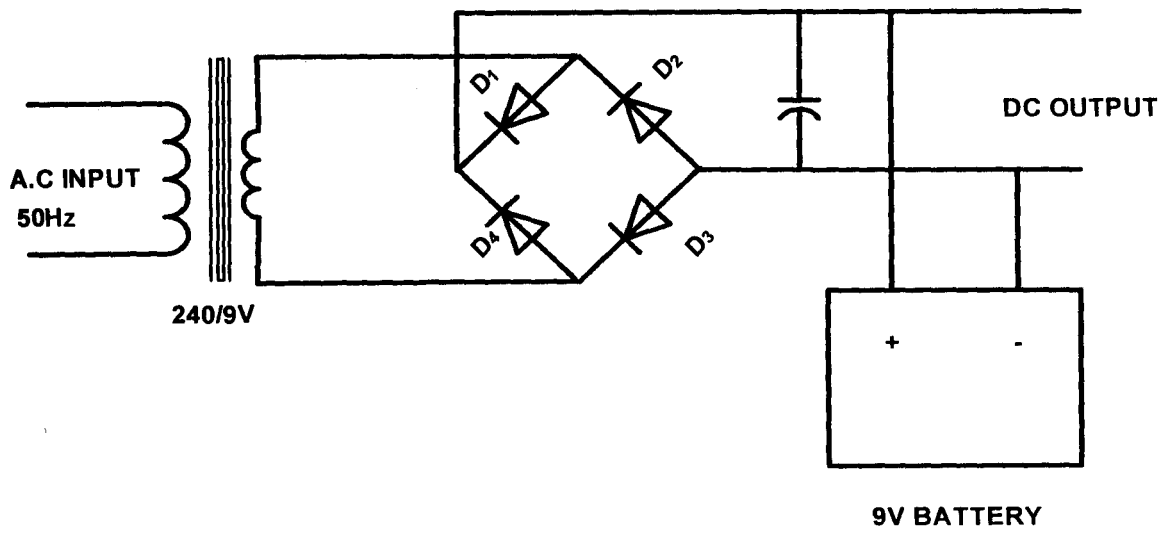


Fig. 2.1 Circuit diagram for the power supply unit

The block diagram of the process involved in the transformation of a.c voltage to d.c voltage is shown in fig 2.2 below

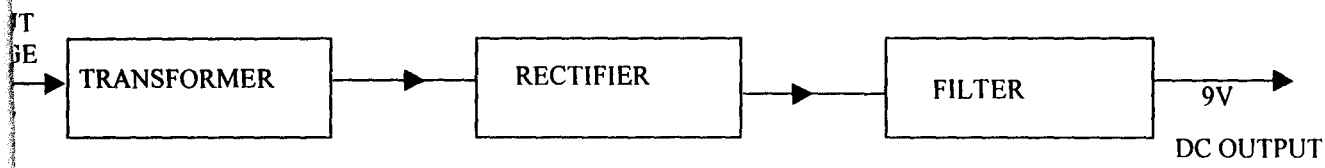


Fig.2.2 Block diagram for the transformation of voltage

2.2.1 THE TRANSFORMER

A 240V/9V step down transformer is used to step down the voltage from 240V from the incoming mains to 9V. The 240V a.c is fed through the power cord to the transformer and the 9V output is presented to the rectifier circuit, a bridge rectifier in this case for rectification.

2.2.2 THE RECTIFIER CIRCUIT

The circuit consists of four general purpose IN4008 diodes joined to form a closed ring. The input to the rectifier is fed through two junctions and the output of the rectifier tapped from the remaining two junctions as shown in fig. 2.3 below

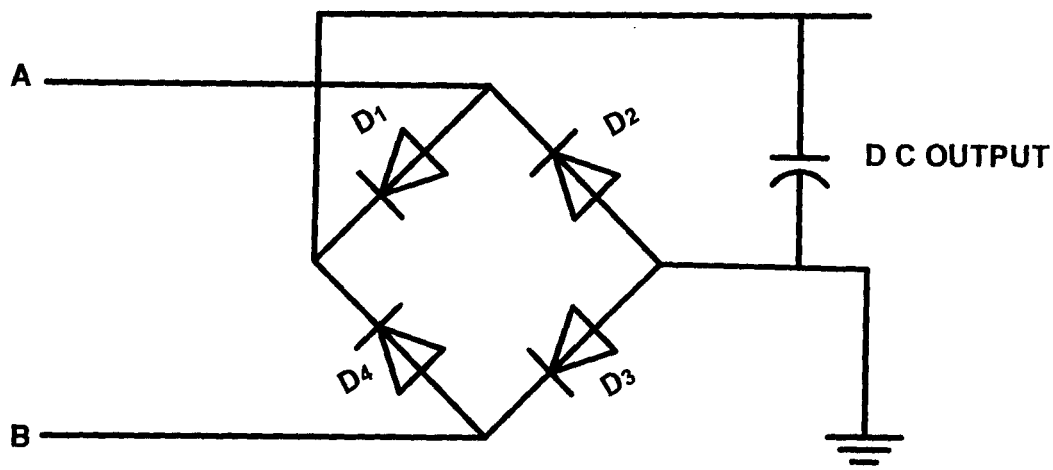


Fig. 2.3 Rectifier circuit

The rectifier circuit has produced a direct component of current but there remains however a large alternating component. It is required to keep this component small. The filter circuit does this by converting the full wave pulsating output of the rectifier into a very steady (smooth) d.c output voltage. The circuit consists of a large capacitor,

generally an electrolytic capacitor in parallel with the step down output of the transformer, the capacitor opposes any change in voltages. The pulsating d.c output is filtered out by the large capacitor whose value is 2200μF. The large value of the capacitor makes a good low ripples output voltage since it produces a large and fairly steady d.c voltage.

2.3.0 THE INPUT UNIT

The input unit consist of an oscillator 4060B (IC1), an up/ down counter 4029B (IC3), a BCD-to-7 segment decoder 4511B (IC4), an SR flip flop (IC5a), and the three push button switches (P1, P2, P3). This unit is used to enter the decimal number to be stored in the memory or to be used to open the lock.

The oscillator provides the pulse required to clock the up/down counter 4029B (IC3) .It is an electronic circuit that converts d.c energy to a.c energy at a frequency value without a switching, rotary or vibratory mechanism. The frequency at the output may be fixed, adjustable in steps or continuously variable. It generates waveform signals in the form of sine, square, saw tooth or pulse shapes. There are various types of oscillators, which include the RC, LC, and crystal oscillator.

The 4060B (IC1) is used as a RC oscillator to produce a series of very short electrical pulses. It is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuit. Also included on the chip is a reset function which places all the outputs into the zero state and disable the oscillator.

The IC is a 14-pin DIP CMOS enhancement mode device with supply voltage from +3Vd.c to +18Vd.c. The pin assignment diagram is shown in fig. 2.4 below.

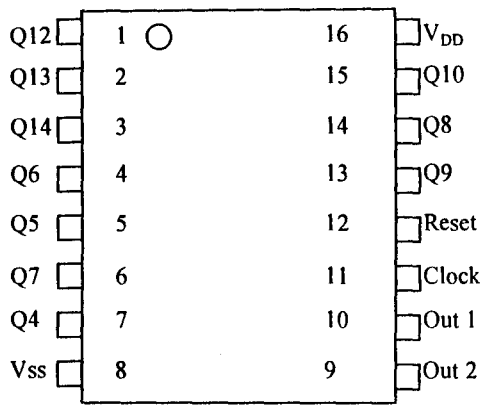


Fig. 2.4 Pin assignment diagram for 4060B

The 4060B (IC1) has a 33K resistor connected to pin 10 (OUT1) and a 100K resistor connected to pin11 (clock) and a 0.001 microfarad capacitor connected to pin 9 (out2), these resistors and capacitor are connected together in parallel.

The up/down counter 4029B (IC3) is used to send the required binary coded decimal (BCD) to the memory unit (as password) or to the comparator unit (to open the lock). A pulse is sent to the clock input pin of the up/down counter 4029B (IC3) when the

push button switch (P1) is depressed and released via the AND gate (IC2a) whose other input is the output of the oscillator.

A counter is a device which stores (and sometimes displays) the number of times a particular events or process has occurred, often in relationship to a clock. The counter is a very important digital system. There are many type of counters, but their purpose is to count either in binary or binary coded decimal (BCD) the changing levels or pulses. Counters are classified into two according to the way they are clocked. There are asynchronous counter and synchronous counter. In asynchronous counters, the first flip flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip flop. In synchronous counter, the external clock pulse is applied to all the flip flops so that they are clocked simultaneously.

For the electronic door lock, the 4029B (IC3) is the counter used. It is a synchronous binary/decade up/down counter constructed with CMOS enhancement mode device. The counter consists of D type flip flop stages with gating structure to provide toggles flip flop capability. It is a 16-pin DIP with input voltage ranging from +3Vd.c to +18Vd.c. The counter can be used in either binary or BCD operation and counting is done on the positive going edge of the clock pulse.

The pin assignment diagram and the truth table of the 4029B-up/down counter are shown below in fig 2.5a and fig 2.5b respectively.

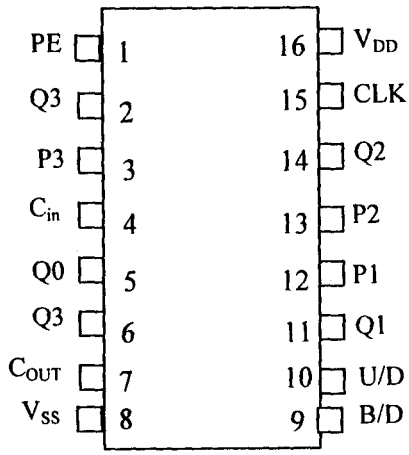


Fig. 2.5a Pin assignment diagram of 4029

Carry in	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count up
0	0	0	Count Down
X	X	1	Preset

X= Don't care

Fig. 2.5b Truth table of 4029B

The input section also consists of the D latch (IC5a) which requires pulse from the push button switches (P1 and P2) to the input of this latch, here the latch is used in the Set-Reset mode. A latch is a bistable multivibrator that can reside in either of the two states by virtue of a feedback arrangement in which the outputs are connected back to the opposite inputs.

The 4013B is a dual type D flip flop constructed from CMOS enhancement mode device. It is a 14-pin DIP with 6 pins each for the two flip flops and the two remaining pins for the power supply and ground voltage. The supply voltage is between +3Vd.c to +18Vd.c. Each flip flop has its own Independent data (D), direct set (S), direct reset (R), clock (C), and complementary output (Q and $\overline{Q}$) pins as shown by its block diagram in fig. 2.6 below.

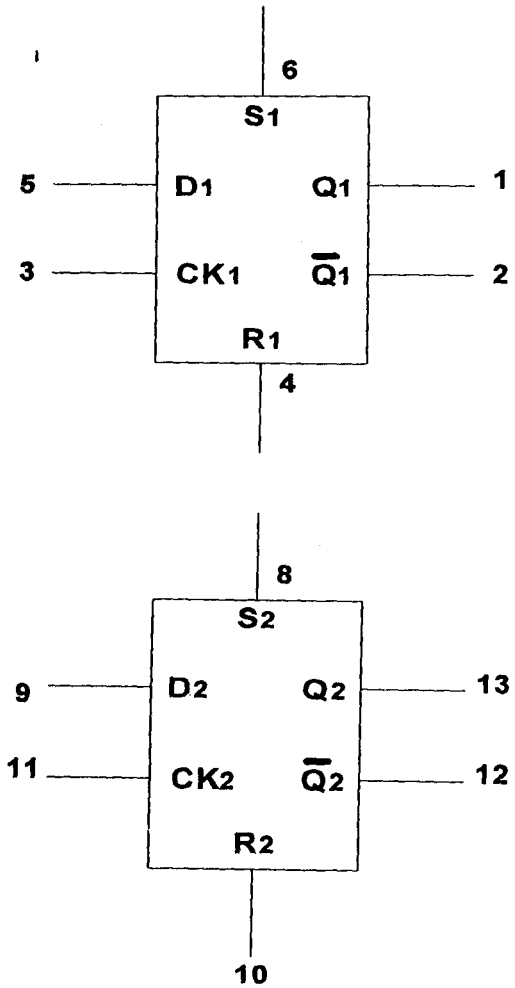


Fig. 2.6 Block diagram of 4013B

The pin assignment diagram and the truth table is shown in fig. 2.7a and fig. 2.7b below

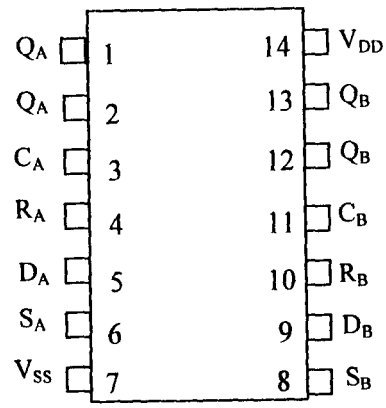


Fig. 2.7a Pin assignment diagram of 4013B

Inputs				**Output**	
Clock	Date	Reset	Set	Q	Q
⎍	0	0	0	0	1
⎍	1	0	0	1	0
⎎	X	0	0	Q	Q
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X=Don't care

+ = Level change

Fig. 2.7b Truth table of 4013B

As the truth table indicates, the logic level at the D input is transferred to the Q output during the positive going transition of the clock pulse. If the clock is transitioning from a HIGH to LOW, the outputs remain in their last state.

If the reset input is brought HIGH, it doesn't matter what the clock and the D input are doing, Q is HIGH and Q is LOW. If the set line goes HIGH, Q goes HIGH and Q LOW regardless of the condition of the clock and D input. The BCD-to-7 segment decoder

converts the binary output of the up/down counter 4029B (IC3) into decimal form, which is displayed by the seven-segment display.

A decoder is a combinational circuit, which generates at its output all the 2^n canonical product terms of the n-signal connected to its inputs. The 4511B (IC4) is used in this device to convert a 4-bit binary code into the appropriate decimal digits. It is a BCD-to-7 segment latch/decoder/driver, which is constructed with CMOS enhancement mode device. The circuit provides the function of a 4-bit storage latch, an 8421 BCD-to-7 segment decoder and output drive capability. The pin assignment diagram is shown in fig. 2.8 below

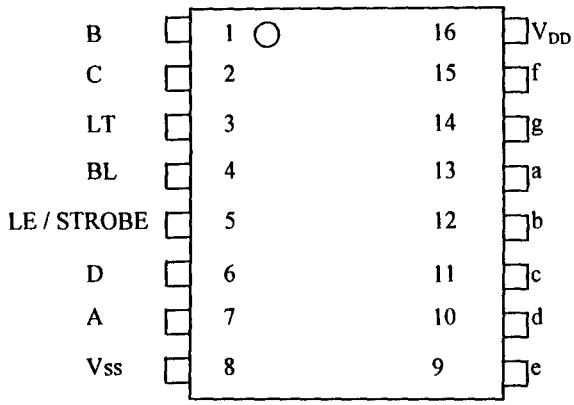


Fig. 2.8 Pin assignment diagram for 4511B

The decoder accepts the BCD code (4 binary numbers) on its input and provides output to drive seven segment display device to produce a decimal readout. The four inputs to the 4511B (IC4) is gotten from the output of the up/down counter4029B (IC3). The output of the decoder is fed to the seven segment display which indicates the decimal equivalent of the binary input. It helps in the decoding of the 4-bit BCD code into the seven outputs

that are required to light the segments of the seven segment LED chip to produces a decimal readout.

Its function is to decode the decimal number being inputted into the memory or that required opening the lock and displaying it on the seven segment display.

2.4.0 DIGIT INDICATOR UNIT

The digit indicator units consist of four D type flip flop (IC7a-b, IC8a-b) used as a shift register, six light emitting diodes (L1-L6) and a seven segment display. This unit shows when a certain process (action) has taken place.

The shift register (IC7a-b, IC8a-b) shows the binary coded number (decimal number) that has been entered into the memory unit or sent to the input pin of the comparator unit.

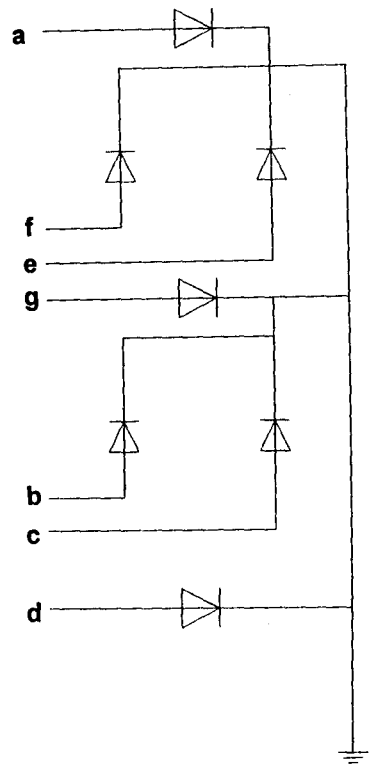
A shift register is a circuit used to store information (data) by shifting data from one stage (flip flop) to another; as such it can be used as a sequencer and in counters to store, delay and format information.

The 4013B is used as a shift register and its characteristics and operation has been described in section 2.3.0. It is used as a D flip flop.

The seven segment display shows the decimal equivalent of the number of pulses received by the up/down counter 4029B (IC3)

It is an opto-electronic device that is used to display a number. The dominant displays technologies today are light emitting diodes (LEDs) and the liquid crystal display (LCDs). They seven rectangular LEDs or LCDs which can form the digits 0 to 9.

The seven LED segments are labeled as shown in fig. 2.9 below.



Common cathode LED display

Fig. 2.9 Seven segment LED display

Each of this segment is controlled through one of the display LEDs, this seven segment display is used with 4511B (IC3) that decodes the BCD number and activate the appropriate digit on the display. Energizing certain combinations of these segments cause each of the ten decimal digits (0 to 9) to be displayed.

There are two type of LED display, the common anode and the common cathode type. In the common anode, the anodes of all the LEDs that form the seven segments are connected together. The common anode arrangement requires that the driving circuit provides a LOW level voltage in order to activate a given segment. When a LOW is applied to a segment input, the LED connected to it is turn ON and there is current through it. In the common cathode, the cathodes of all the LEDs that form the seven

segments are connected together. The common cathode arrangement requires that the driver provides a HIGH level voltage to activate a segment. When a HIGH (supply voltage) is applied to a segment input, the LED connected to it is turned ON and there is current flow through it.

In this device the common cathode seven segments display is employed. The input to the seven segment display is the output of the 4511B (IC4) which is fed through seven (330 ohms) limiting resistors to limit the current through the LEDs. The circuit connection is shown fig. 2.10 below

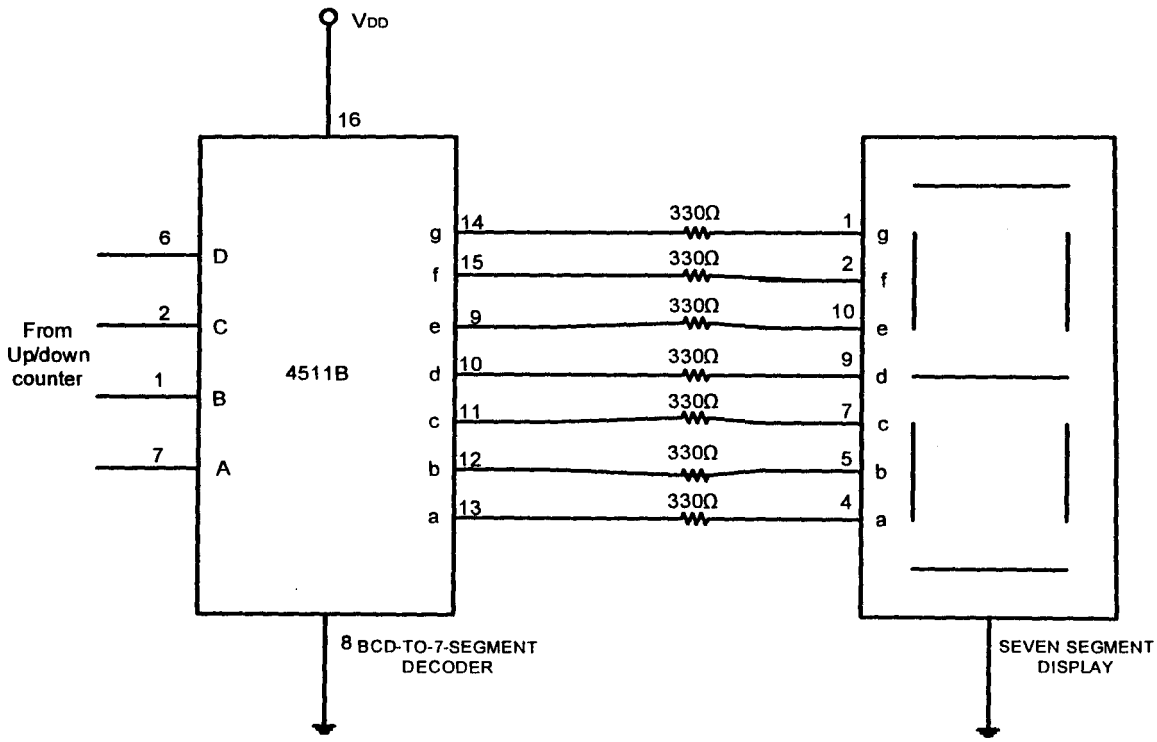


Fig. 2.10 The circuit connection of the seven segment to the decoder

The light emitting diode are connected to the shift registers (IC7a-b, IC8a-b) to show the number of binary coded decimal (BCD) that have been entered into the memory unit or to the comparator unit. They are special forward PN junction which emits light at different wavelength (and hence at different colours) determined by the material used. Forward currents from 5mA to 80mA are usual, a series resistor being used to limit the current drawn.

The colour of the emitted light depends on the type of material used, which determines the wavelength of the radiated light and thus the colour.

The LED material and the colour given out is written below.

Gallium arsenide- infrared radiation

Gallium phosphide- red or green light

Gallium arsenide phosphide- red or yellow light

The LED emits light in response to a sufficient forward current. This amount is proportional to the forward current. LEDs are used as lamp and display indicator.

2.5.0 THE PASSWORD ENABLE UNIT

The password enable unit consist of two push button switches (P3 and P5), a SR flip flop (IC6), an AND gate (IC17) and a light emitting diode (L5). This is used to enable the memory latch (IC9-IC12) to store data on the data line into it.

The push button switches P4 and P5 and the output of the AND gate (IC17) are used to change the state of the normal output of the SR flip flop (IC6) and this output is applied to one of the two data disable pin of all the four memory latches (IC9-IC12) simultaneously and this controls the storage of data on the data line into the memory latches (IC9-IC12) one after the other. The light emitting diode (L5) shows that this mode is enabled when it is ON.

2.6.0 THE CONTROL UNIT.

The control unit consist of the Johnson decade counter 4017B (IC13), an AND gate (IC2b), a push button switch (P4) and four NOT gates (IC14a-d). It is used to control the storage of bits to be used as password into the memory unit, to output this values stored in the latch to the input of the comparator unit and as an input to the AND gate (IC2c) whose output is required to open and close the lock.

The inverted outputs of the Johnson decade counter (IC13) are used to control the storage of data (password) on the data into the memory latches (IC9-IC12). One of these outputs (the fourth output) is also used to control the output unit via the AND gate (IC2b). These outputs of the Johnson decade counter are controlled by the input unit.

The Johnson decade counter is a special type of shift register in which the input is obtained directly from the output. The input of the first stage making up this counter is gotten from the output of the last stage making up this counter. Patterns of bits equal in length to the number of flip flop that make up the shift register thus circulate indefinitely.

The Johnson decade counter 4017B (IC13) is a14-pin DIP CMOS enhancement device with supply voltage ranging from +3Vd.c to +18Vd.c. It is a five-stage synchronous Johnson decade counter. It has ten decoded outputs which are normally LOW and goes HIGH only at their appropriate decimal time period. The output changes occur on the positive going transition of the clock pulse. Each decoded output remains HIGH for one full clock cycle. Input pins of the Johnson decade counter (IC13) include a clock, a reset pin, and a clock inhibit signal pin. The counter advances on the positive going edge of the clock signal input, if the clock inhibit signal is LOW. Counter advancement via the clock line is inhibited when the clock inhibit signal is HIGH. A HIGH applied to the reset pin clears the counter to the zero count. The pin diagram and truth table of the Johnson decade counter are shown respectively below in fig. 2.11a and fig. 2.11b.

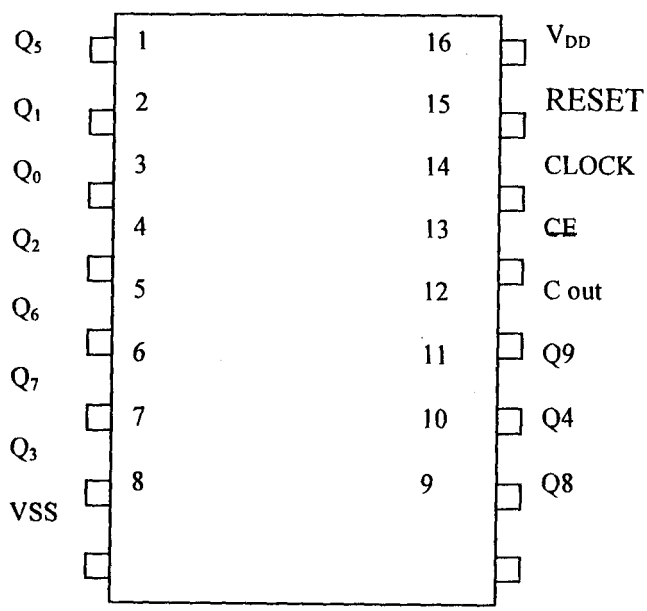


Fig. 2.11a Pin assignment diagram of 4017B

Clock	Clock Enable	Reset	Decode Output =n
0	X	0	n
X	1	0	n
X	X	1	Q0
⌐	0	0	n+1
¬	X	0	n
X	⌐	0	n
1	¬	0	n+1

X = Don't care

If n<5 Carry(C) = "1", otherwise C= "0"

Fig. 2.11b Truth table of 4017B

The fourth output is connected to the clock inhibit signal input. After the fourth clock pulse, the counter clock inhibit signal is enabled and this inhibit the counter in advancing to the next state.

2.7.0 THE MEMORY UNIT

Memory units are devices used for storing of data (binary information). It makes use of sequential circuits whose output depends not only on the present input but on the past ones as well. The order or the sequence in which the outputs are applied is imperative. The memory element of the sequential logic is usually obtained by feedback connection, which ensures that when the output changes the effect of the previous input is not lost. For handling information in binary logic, flip flops with their two stable states representing 1s and 0s can do the job and are readily switched from one state to the other by appropriate circuits.

The memory unit consists of four 4076B 4-bit register. The 4076B is a 4-bit register consisting of four D flip flop operating synchronously from a common clock. OR gated output disable input pins forces the outputs to high impedance state for use in bus organized systems. OR gated data disable input pins causes the Q outputs to be feedback to the D inputs of the flip flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. Input of the 4076B chips include two data disable lines, two output disable lines, a clock, a reset pin, four data lines and four output lines. The four BCD input values are stored only when the two data disable lines are LOW at the positive clock signal transition and this value is outputted only when the two output disable lines are LOW on the positive clock transition. If one or both of the data disable lines are HIGH, data at the data line will not be stored in the flip flop. Also if one or both of the output disable lines are HIGH, there will be not output from the flip flop, the output is forced into a high impedance state. A HIGH reset input clears all the four flip flops simultaneously independent of the clock or disable inputs. The pin assignment diagram and the truth table are shown respectively in fig. 2.12a and 2.12b below

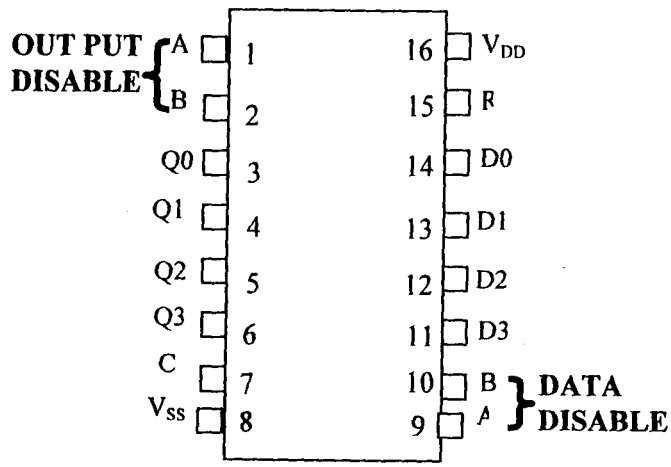


Fig. 2.12a Pin assignment diagram of 4076B

Inputs					
Reset	Clock	Data Disable A	B	Data D	Output Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⌐	1	X	X	Q_n
0	⌐	X	1	X	Q_n
0	⌐	0	0	0	0
0	⌐	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip flops is not affected.
X = Don't care

Fig. 2.12b Truth table of 4076B

The 4076B (IC9 –IC12) is used for storing the BCD value for each of the four decimal digits required as password to open the lock.

2.8.0 THE COMPARATOR UNIT

It is a combinational logic circuit that compares two sets of input binary quantities. It is used for decoding application. An output of the decoder is activated when the two sets of inputs are fed with the same binary pattern. The comparator outputs are needed to activate circuitry to enhance physical variable towards the reference value.

The comparator unit is made up of a quad 2-input exclusive-OR gate (IC15) and three OR gates (IC16a-c). The comparator unit output a LOW when the two sets of binary

inputs have the same binary pattern and a HIGH when the two sets of binary inputs differ. The diagram for the connection is shown in fig 2.13 below.

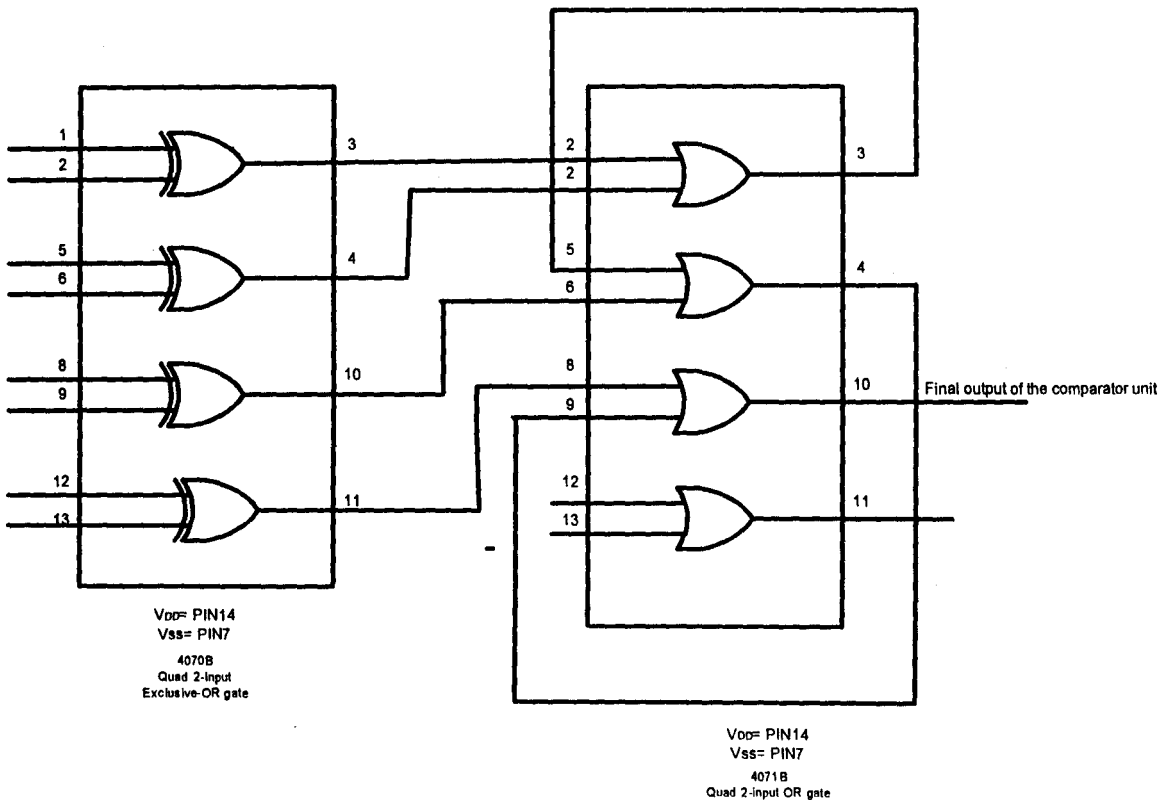


Fig. 2.13 The circuit connection of the comparator unit

2.9.0 THE OUTPUT UNIT

This unit consist of a SR flip flop 4013B (IC5b), two AND gates (IC2c-d), an NPN transistor 2SD400 (Q1), a d.c motor, a push button switch (P6) and a light emitting diode (L6) and a knob.

The normal output (Q) of the 4013B (IC5b) is controlled by the push button switch (P4) and the output of the AND gate (IC2d). This output is required to open the electronic lock via the output of another AND gate (IC2c). The LED (L6) is ON if the correct decimal digits sequences have been entered and the door will open or OFF if the wrong decimal digits sequences have been entered and thus the door will not open.

The output of the AND gate (IC2c) is applied to the base of the transistor (Q1) and this opens or close the lock depending on the input applied to the base of the transistor. The output of the transistor (Q1) is used in opening the door by the switching action of the transistor on the input applied to the base. The output of the transistor (Q1) is applied to one leg of the push button switch (P6) and the other leg is connected to the supply voltage.

The transistor used in this project work is 2SD400 which is a general purpose NPN transistor with V_{CBO} of 120V, V_{CEO} of 100V, I_C of 1A, gain (h_{FE}) of 200 and frequency of 140MHz. As a general purpose transistor, it can be used as an amplifier, driver or switch.

The NPN transistor 2SD400 (Q1) is used as a switch and as a switch it operates between two extreme situations namely at cut-off (non conducting state) or saturation (conducting state) in which the base current appears at the collector terminal or not. This circuit does polarity inversion of the input applied to the base of the NPN transistor 2SD400 (Q1) and the output at the collector terminal is connected to one leg of the push button switch (P6).

A push button switch (P6) is connected to the motor and it is use for rotating the armature and the knob connected to the armature to close and open the lock.

The electric motor is used to rotate the knob connected to its armature to open or close the door lock.

The motor used in this project work is a 9V DC motor.

2.10.0 THE WORKING OPERATION.

The electronic door lock starts working when it is powered ON. The password to open the lock is first stored. This is done by first pressing the push button switch (P4) to reset the following integrated circuits, the Johnson decade counter (IC13), the shift register (IC 7a-b, IC 8a-b) and to set the SR flip flop 4013B (IC5b). Then the push button switch (P3) is pressed and released to enable the data on the data line to be stored in the memory latches (IC9-IC12) one at time. By pressing the push button switch (P3), the SR flip flop (IC6) connected to this switch is set, the normal output (Q) of this flip flop (IC6) is HIGH which ON the light emitting diode (L5) connected to this normal output (Q). The inverted output (**Q**) of this flip flop (IC6) is connected to one of the two disable data pins of all the four memory latches (IC9-IC12) joined together and enable the storage of data on the data line on these latches one at a time, if the input to the other data disable pin LOW. The LED (L5) is the "dot LED" of the seven segment display. To store data into these memory latches (IC9-IC12), the two data disable pins must be LOW and this occurs at the positive transition of the clock pulse.

The first decimal digit to be stored as password is entered by pressing the push button switch (P1), the pulse from this push button switch (P1) with the low frequency value output pulse of the oscillator (IC1) activates the up/down counter (IC3) to start

counting. When the required decimal number to be used as password is reached, the push button switch (P1) is released. Then the push button switch (P2) is pressed and released to send clock pulses to the four memory latches (IC9-IC12) and allow data to be stored in the memory latch which has a LOW on both data disable pins which is memory latch (IC9) in this case. The decimal digit is shown on the seven segment display.

With the push button switch (P1) pressed and released, the normal output (Q) of the SR flip flop (IC5a) is HIGH which clock the Johnson decade counter (IC13) to advance to its first count during the positive transition of the first clock pulse. This makes the first output of the Johnson decade counter (IC9) HIGH, which is made low by the NOT gate (IC14a) and this is applied to one of the data disable pin and the two output disable pins of the first memory latch (IC9). When push button switch (P2) is pressed and released, it sends clock pulses to the four memory latches (IC9-IC12) and since only the first memory latch (IC9) has the two data disable pins LOW, it will store the data on the data line. When the push button switch (P2) is pressed and released, this push button resets the SR flip flop (IC5a) connected to it. The inverted output (**Q**) of this flip flop (IC5a) which is now HIGH is used to clock the shift register (IC7a-b, IC8a-b) which ON the first light emitting diode (L1) connected to the output of the first flip flop (IC7a) and shows that the first data (4 BCD code) has been entered.

For the second decimal digit, the push button switch (P1) is pressed again until the second required number is reached as shown on the seven segment display, and then it is released. The normal output (Q) of the SR flip flop 4013b (IC5a) which this push button switch is connected to, is HIGH which advances the Johnson decade counter (IC13) to its second output. This output is inverted by the NOT gate (IC14b) and applied

to the second flip flop (IC10), this has the two data disable inputs LOW and this latch (IC10) stores the data on the data line when the push button switch (P2) is pressed and released. The inverted output (**Q**) of the SR flip flop (IC5a) is HIGH when the push button switch (P2) is pressed and released and this output is applied to the second light emitting diode (L2) to ON it and show that the second data (4 BCD code) has been entered.

For the third and the fourth decimal digits, the above processes; that is pressing and releasing the push button switch (P1), then pressing and releasing the push button switch (P2) for each of the two remaining decimal digits. The four light emitting diodes (L1-L4) are ON to show that the four decimal values required for the password have been entered. After releasing the push button switch (P2) after the fourth decimal number has been entered, the push button switch (P5) is pressed and released, this push button is connected to the reset pin of the SR flip flop (IC6) and its normal output (Q) is LOW which turn OFF the light emitting diode (L5) connected to this output. The inverted output (**Q**) is now HIGH and this disable the four memory latches (IC9-IC12) from storing any data on the data line, since a HIGH is applied to one of the two data disable pins of all the four memory latches (IC9-IC12).

The fourth output of the Johnson decade counter (IC13) a HIGH is applied to its clock disable pin. This HIGH input disable the Johnson decade counter to advance to the next count and also disable the outputting of the password stored in the memory latches (IC9-IC12) to the input pin of the comparator unit. It also enables a HIGH to one of the two inputs of the AND gate (IC2b) which is applied to another AND gate (IC2c) whose output is required to open or close the lock. To close the door after inputting the

password, the push button switch (P4) is pressed and released, this resets the Johnson decade counter (IC13) to its initial state, clears the shift register (IC7a-b, IC8a-b) and OFF all the LIGHT emitting diode (L1-L4) connected to it and apply a LOW to one of the two inputs of the AND gate (IC2b) whose output a LOW is applied to another AND gate (IC2c), the output of this AND gate (IC2c) is a LOW and closes the lock.

To open the door lock when the lock is closed, the push button switch (P1) is pressed which activates the up/down counter (IC3) to count until the first decimal value to open the lock is reached, this digit is display on the seven segment display, then the push button switch (P1) is released. The push button switch (P2) is then pressed and released,this number (and any other number) will not be stored in any of the memory latches (IC9-IC12) because the password mode is not enabled and the inverted output (**Q**) of the SR flip flop (IC6) applied to one of the data disable pin of all the four memory latches (IC9-IC12) is HIGH, so will not store this number but output the stored number at the transition of the clock pulse of the push button switch (P2) applied to it. This decimal number is sent to one of the two input pins of the comparator unit.

With the push button switch (P1) pressed and released, it sets the SR flip flop (IC5a) and the normal output (Q) of this flip flop (IC5a) is used to activate the Johnson decade counter (IC13) to its first count. The first output is a HIGH which is inverted by a NOT gate (IC14a) to a LOW and this output is applied to one data disable pin and the output enable pins of the first memory latch (IC9), this allows the number stored in the latch (IC9) to be outputted to the second input the pin of the comparator unit at the clock pulse transition cause by pressing and releasing the push button switch (P2). This latch (IC9) is the only latch whose stored data is sent to the second input pin of the comparator

unit via the output data line, since it is the only one whose two output disable lines are LOW. Also with the push button switch (P2) pressed and released, the SR flip flop (IC5a) to which this push button switch is connected to, is in its reset condition and its inverted output (**Q**) connected to the clock pulse of the shift register (IC7a-b, IC8a-b) is HIGH which allows the first LED (L1) connected to the output of the first flip flop to be ON after the first clock pulse to the shift register to show that the first decimal number has been sent to the first input pin of the comparator unit.

The comparator unit compares the two set of inputs on it terminal (one from the up/down counter [IC3] and the other from the memory latch, in this case IC9 via the output line), and output a LOW if the binary inputs are equal and a HIGH if they are different. This output is applied to one of the two input pins of the OR gate (IC16a)

For the second decimal number, the push button switch (P1) is pressed until the second number stored as the number of the password is reached, as shown on the seven segment display then the push button switch is released. The normal output (Q) of the SR flip flop (IC5a) to which this push button switch is connected to, is in its set condition (a HIGH) and this is used to activate the Johnson decade counter (IC13) to its second output which is inverted by the NOT gate (IC14b) to a LOW and applied to one data disable pin and the two output disable pins of the second memory latch (IC10). Since only this latch (IC10) has a LOW on both output disable pins, it is only it that will output the stored value to the second input pin of the comparator via the output line on its clock pulse when the push button switch (P2) is pressed and released. The pulse of the push button switch sends a second clock pulse to shift register (IC7a-b, IC8a-b) which makes the light emitting diode (L2) connected to the output of the second flip flop (IC7b) to be ON to

show that the second decimal value to the first pin of the comparator unit has been entered.

The comparator compares the two sets of the second input on it terminal and output a LOW if the binary inputs are equal and a HIGH if they are different. This output is applied to the second input of the OR gate (IC16a), the output of the OR gate (IC16a) is applied to one of the two input pins of another OR gate (IC16b).

The third and the fourth decimal numbers to open the lock are sent to the comparator unit one after the other as done with the process of inputting the first and second decimal numbers. The comparator unit compares the two sets of inputs and output a LOW if they are equal and a HIGH if they are different. With the third number, the output of the comparator unit is applied to the second input of the OR gate (IC16b) and the output of this OR gate (IC16b) is applied to a third OR gate (IC16c) as one of the two inputs to it. Also the third light emitting diode (L3) is ON to show that the third number has been entered to the input pin of the comparator unit.

When fourth number to open the lock is entered, the output of the comparator unit is applied to the second input of the third OR gate (IC16c), this final output is applied to one of the two input pins of the AND gate (IC2d) whose second input is from the normal output (Q) of the SR flip flop (IC5a). This output is HIGH.

If the set of BCD codes applied to the comparator unit are the same as the value stored in the memory latches (IC9-IC12), the output of the comparator is a LOW and this output is applied to the input of the AND gate (IC2d) whose output is a LOW in this case and this leaves the normal output (Q) of the SR flip flop (IC5b) to which this output is connected to still HIGH from the set operation performed by the pressing and releasing of the push

button switch (P4) when the door was locked. But if any set of the BCD codes applied to the comparator unit is different from the BCD codes stored in the memory latches (IC9-IC12), the output of the comparator unit is HIGH and since the other input to the AND gate (IC2d) is a HIGH, it reset the SR flip flop (IC5b) outputting a LOW to the normal output of this SR flip flop (IC5b) and disable the last AND gate (IC2c) whose output is required to open the lock.

The lock will not open from the set condition to the flip flop (IC5b) provided by pressing and releasing the push button switch (P4) since the second input to the AND gate (IC2c) required to open the lock is gotten from the output of another AND gate (IC2b) which is a LOW and disable the final AND gate (IC2c) from opening the lock. This is a LOW from the resetting of the Johnson decade counter (IC13) whose fourth output is a LOW and this is applied to the AND gate (IC2b) and produces the LOW.

If the four decimal numbers are not the same as the four decimal numbered stored in the memory latches (IC9-IC12) in BCD values, inputting any other decimal number by pressing and releasing the push button (P1) and then pressing and releasing the push button (P2), without first pressing and releasing the push button switch (P4) to reset the Johnson decade counter (IC13) so as to make the value stored in the memory latches (IC9-IC12) to be outputted will have no effect on the opening of the lock. This is because entering any number without first pressing and releasing the push button (P4) will just send the number to the first input pin of the comparator unit with nothing from the memory latches (IC9-IC12) to the second input of the comparator unit, since the stored value to be outputted from the memory latches (IC9-IC12) have been disabled by a HIGH

on both output disable pins. The comparator unit will give no output since the second input to the comparator unit has nothing applied to it.

With the output of the comparator being LOW, the normal output (Q) of the SR flip flop (IC5b) is HIGH and the fourth output of the Johnson decade counter (IC13) is also HIGH after the fourth number as been entered. These two inputs are applied to the final AND gate (IC2c) and its output is a HIGH. This output is applied simultaneously to a light emitting diode (L6) and the base of the NPN transistor (Q1) via a limiting resistor. If this input is HIGH, the transistor acts as a switch in the common emitter configuration to invert the output to a LOW and this is applied to one leg of the push button switch (P6), which has the supply voltage applied to the second leg of the switch (P6). This makes the motor connected to the switch (P6) to start rotating when the push button switch is pressed and the knob connected to the armature of this motor is released to open the door in this case. But if the output of the final AND gate (IC2c) is LOW, the transistor (Q1) does polarity inversion of this input to a HIGH and the two pairs of the pole have voltage applied to them and this disable the motor from working.

To close the lock the push button switch (P6) is released to change the polarity of the motor and make the knob to be pushed back into the lock position.

To change the password, the door must be opened, since the output of the final AND gate (IC2c) is applied to one of the two inputs to the AND gate (IC17) required to activate the password mode and the output of this AND gate (IC17) is applied to the SR flip flop (IC6) which set this flip flop (IC6) when the door is opened and the push button switch (P3) is pressed and released and make the light emitting diode (L5) connected to the

normal output of the SR flip flop (IC6) to be ON. But if the door is not opened, the output of this AND gate (IC17) is a LOW and will not set the SR flip flop (IC17) and the light emitting diode (L5) connected to the normal output (Q) of this flip flop will be OFF to show that password mode is not enabled. If the push button switch (P3) is pressed and released the light emitting diode (L5) will be OFF if the door is not opened and the password cannot be changed. If the password mode is enabled, the password is changed as explained at the beginning of this section.

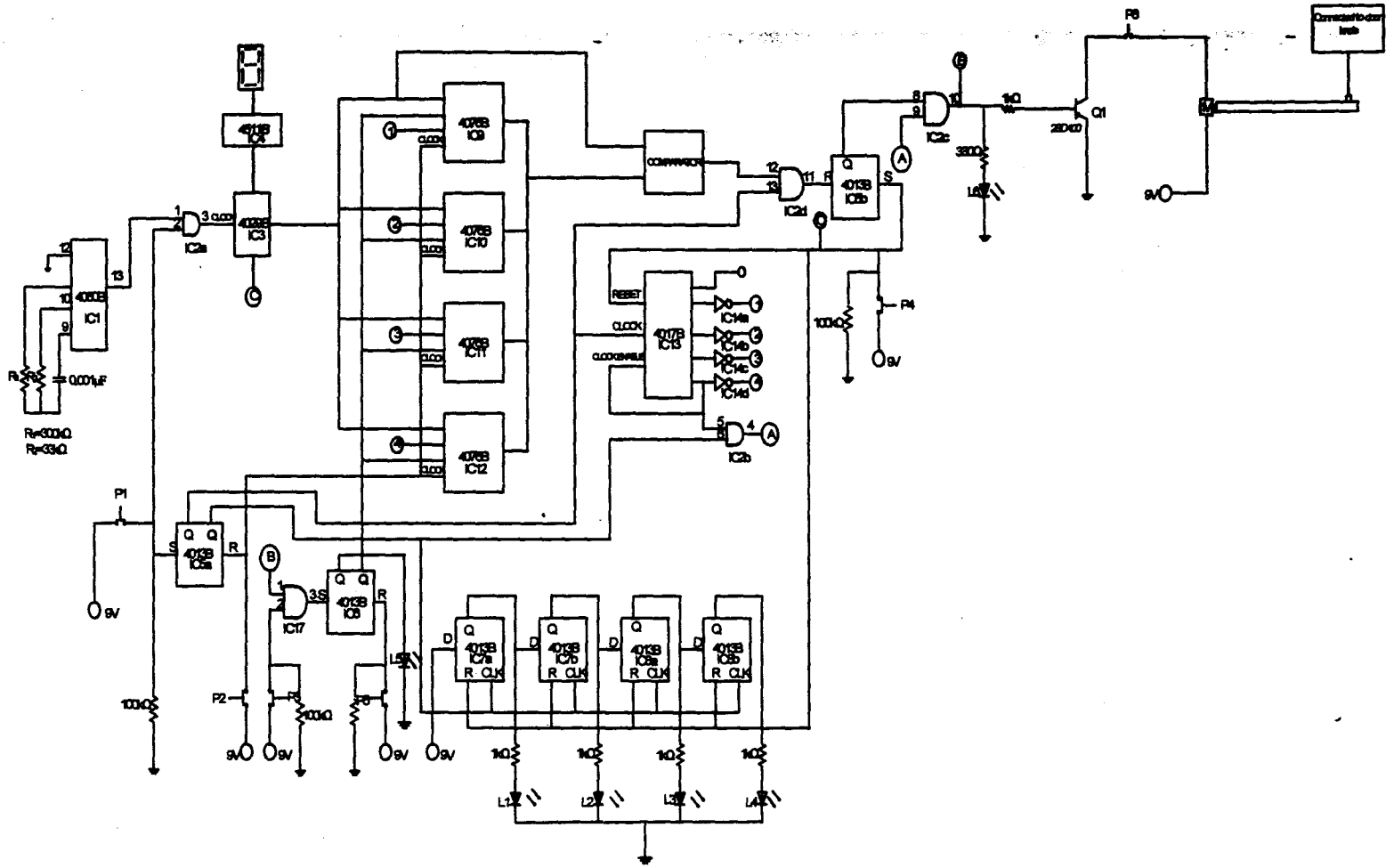


Fig. 2.14 The circuit diagram of electronic door lock

CHATPTER THREE

3.0.0 CONSTRUCTION, TESTING AND RESULT/INFERENCE

3.1.0 THE CONSTRUCTION

In the construction work the manufacturer's data sheet of the different ICs and transistor used for this project were studied to know about each pin and the different functions they perform and how to connect them.

The construction involve three stages, the initial stage was the construction of the project on the breadboard. This involves the arrangement of the components according to the circuit diagram giving attention to the polarity of polarized components (such as diodes, LEDs, transistor and electrolytic capacitor) on the breadboard. The circuit was powered using a 9V dry battery cell. This is to check that the circuit diagram is working as designed, before transferring the components to the Vero board.

The second stage was the transferring of the components in unit to the Vero board to ease construction work and to help detect fault if any one arise. The second stage involves planning a rough layout of the project on the Vero board using paper to show how and where the components making up the project work are to be mounted on the Vero board. In planning the layout physical proximity of these components and the multiple connections required between integrated circuits (ICs) and between integrated

circuit and other passive components were considered so as to effectively minimize the number and size of wire links. The Vero board was cut into two sizes, one for the power unit and the other for the remaining components making up the door lock taking into consideration the component spacing and clearance between components to avoid fault. The mounting of the diodes, electrolytic capacitor and the transformer forming the power unit were done to its Vero board taking note of the polarity of the electrolytic capacitor, diodes and LEDs and the primary side and the secondary side of the of the transformer. This was then compared with that of the circuit diagram and soldered. The other IC components and the passive components forming the door lock were also mounted using IC sockets for ICs that are prone to fault from excessive heat from the soldering iron. This was also compared with the circuit diagram taking note of the polarities of the LEDs and the power supply to the ICs.

The third stage was the soldering. Soldering was performed with due regard to safety. It was carried out using a low voltage soldering iron, operated from a transformer connected to the mains. A hot soldering iron is essential if good solder joints are to be produced. The hot soldering iron was placed so that it touches both the soldering lead and the terminal to be soldered. These steps were repeated for the soldering of each passive components, IC chips and IC sockets to the Vero board. Over heating of the joint (terminal) was avoided because it could damage the components being soldered and also soldering of bridge linking tracks together was avoided.

Flexible wires were then soldered to link the different components that form the circuit together while referring to the manufacturer's data sheet and to the circuit diagram

so that all components were properly connected and the right way round. On completion, the Vero board was carefully checked for any loose leg not soldered properly and for any wrong connection of polarized components. The circuit was tested before it was fixed onto the door by entering the password code to open the lock and testing this password code and wrong password codes, so as to rectify any problem before it is fixed to the door.

3.2.0 THE DOOR (CASING)

A wooden case was chosen for the door because of its cheapness, availability, ease of drilling holes, its light weight, its physical outlook and ease of modification.

In the construction of the door, a small of suitable size was cut out for the Vero board containing the different component that make up the door lock. Plywood of suitable size was cut on which small holes were drilled on it for the six push button switches, and for five light emitting diodes. Also an appropriate hole was also cut on the plywood for the seven segment display. This plywood was screwed to the front of the door and another plywood of appropriate size was screwed to the back of the door to hold the Vero board to position. The motor with the knob was also screwed to the back of the door, a small wood was placed by the side to the door to hold the knob in place when the door is locked.

3.3.0 TESTING

The device (door lock) was tested after construction to check if the circuit is working according to the design. The devices was tested as follows

1) When the device was connected to the power supply the wrong password was entered.

2) With the device still powered and the push button switch (P4) pressed and released, the right password was entered.

3) With the device still connected to the power supply the door was locked and the wrong was entered and then the right password was entered without pressing the push button switch (P4).

4) The push button switch (P4) was pressed and released and the right password was entered.

5) With the right password entered and the light emitting diode (L6) ON the password was changed by pressing and releasing the push button switch (P3), later push button switch (P5) was pressed and released after the fourth decimal number to be used as password has been entered and the steps 1-3 above were repeated for the new password.

6) Lastly the door was locked and the push button switch (P3) was pressed and released to store another new password and this new password was entered to open the lock.

3.4.0 THE RESULT/INFERENCE

The following results were obtained for the tests, as stated in section 3.4.0 above.

1) When the system was powered and the wrong password was entered, the door was locked being shown by the LED (L6) being OFF.

2) With the second step, the door opened and the LED (L6) was ON.

3) With the third step, the door was closed even with the right password entered immediately after the wrong password this was indicated by the LED (L6) being OFF.

4) With the fourth step, the door opened and also the LED (L6) was ON.

5) For fifth step, the "dot LED" (L5) of the seven segment display was ON when the push button switch (P3) was depressed and released and OFF when the push button switch (P5) was depressed and released. The door opened when the new password was entered for step 2 performed on this new password and this was indicated by the LED (L6) being ON and locked for the steps 1 and 3 performed on this new password as indicated by the LED (L6) being OFF.

6) In this last step, the "dot LED" (L5) of the seven segment display was OFF when the push button switch (P3) was depressed and released and the door did not open with the third password entered, this was indicated by the LED (L6) being OFF.

It was inferred that the right password is required to open the lock and that if a wrong password is applied first, the push button switch (P4) must be depressed and released before entering the right password so as to open the lock after inputting the right password. Also it was seen that the password cannot be changed unless the door is opened. In the process of testing, it was found out that two decimal numbers of the same value cannot be entered by depressing the push button switch (P2) twice to enter the number twice. This is shown by the next light emitting diode of the shift register (IC7a-b, IC8a-b) being OFF. This shows that even if two equal decimal numbers is to be entered into the memory latches (IC9-IC12) or to one of the two input pins of the comparator

unit, the push button switch (P1) has to be depressed again until that decimal number appear again as shown on the seven segment display before the push button switch (P2) is then depressed and released to the this second equal decimal digit. This is because the normal output (Q) of the SR flip flop (IC5a) to which the push button switch (P1) is connected, is required to clock the memory latches (IC9-IC12) to output the stored in the latch to the input pin of the comparator unit to provide the second input required for the comparator to send an output. Also the inverted input (**Q**) of the SR flip flop (IC5a) is required to clock the shift register (IC7a-b, IC8a-b) to ON the light emitting diodes (L1-L4) connected to the output of each flip flop that makes up the shift register, since the push button switch (P1) is not depressed and released before depressing the push button switch (P2) the will not change of state of the inverted output (**Q**) of SR flip flop (IC5a) required to clock the shift register (IC7a-b, IC8a-b) and the shift register (IC7a-b, IC8a-b) will not go to next stage and the next LED will be OFF since there is not clock pulse applied to the shift register.

CHAPTER FOUR

4.0.0 CONCLUSION AND RECOMMENDATION

4.1.0 CONCLUSION

It can be seen from the foregoing sections that the design of an electronic door lock, just like any other project work requires planning and implementation. This project work has been quite a challenging task; it has afforded me the opportunity of getting a better understanding of some basic electronic principle. The problem of getting the necessary textbook for research construction and report write up had to be contended with. Even with this, most of the construction and project write up was carried out through painstaking research.

The design and the construction of the door lock have successfully being constructed as explained in chapter three of this write up. From the various tests performed and the result obtained, it has shown that the aim of the project as stated in chapter one of this write up has been achieved and since the principle used for the electronic door lock worked according to specification and quite satisfactorily.

The electronic door lock constructed is relatively affordable, reliable, provide high level of security, uses low power consumption and easier to use (operate), which are the result technology and engineering standout to achieve.

4.2.0 RECOMMENDATION

The following suggestions are given on the project work generally and electronic door lock in particular

1) The department laboratory should be well equipped with the equipment that will help students in their project work and that project should be given to student before they go on their IT program so as to make them have a broader view (knowledge) and research on their project.
2) I also recommend that this project electronic door lock be used in the schools for locking each room in the hostel and for lecturer's offices.

Since the design can still be improved on, the following suggestions listed below were made to serve as a basis (guide) for further research in this project in the improvement of this project design work.

1) The design circuitry could be implemented to include an alarm unit to be triggered if the wrong password is entered three times, this will help increase the level of security provided by the device.

2) A bypass switch could be included into the circuit to open the lock in the event that the owner forgets the password, the position of this switch should be known to only the owner of the lock. This is to provide reliability of the lock in the event that the password is forgotten and prevent damaging the lock.

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