DESIGN AND CONSTRUCTION OF

A DIGITAL QUIZ DECIDER

BY

OLADEJO AKINTOLA O.

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A THESIS SUBMITTED IN PARTIAL

FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF

BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING,

SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY,

FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA,

NIGERIA.

NOVEMBER, 2004

CERTIFICATION

This is to certify that this project work was carried out and submitted by Mr. Oladejo Akintola O. with registration number 99/9059EE of Electrical/Computer Engineering Department, School of Engineering and Engineering Technology, Federal University of Technology, Minna, Niger state, Nigeria

..... DATE..08/12/04....

ENGR. USMAN ABRAHAM

(SUPERVISOR)

..... DATE..05/04/2005

ENGR. M.D. ABDULLAHI

(Head of Department)

..... DATE.....

(EXTERNAL EXAMINER)

DECLARATION

I hereby declare that this project work was entirely carried out by me under the supervision of Mr. Abraham Usman of the department of Electrical/Computer Engineering, School of Engineering and Engineering Technology, Federal University of Technology, Minna, Nigeria.

..... **Date**.....

Oladejo Akintola O.

(Student)

DEDICATION

I want to dedicate this work first of all to the Almighty God and my Saviour Jesus Christ who has made me the apple of His eyes and has continuously hid me under the shadow of His wings, lavishing on me His Salvation. Secondly, to my loving, virtuous and amiable mother who tirelessly bore the pain, the struggle and the challenge of my survival in the early stages of my life!

ACKNOWLEDGEMENT

I want to first and foremost acknowledge the mighty hand of God upon me and on this project right from the sourcing to the actualization of it. He is indeed a great Provider! I am grateful to my parents for their effort at seeing to it that I am educated. I say thank you PAPA and MAMA. I also say thank you to my stepmother.

I must specially mention my wonderful sister Miss Yemi Oladejo who contributed immensely to my university education. She was never tired of sharing her meager resources with me. She remembers to give me even before I ask. My prayer is that you will not miss God's purpose for your life. God will take up your case and bless you real good. Mrs. Olaleye contributed immensely to making this project a reality. She almost single handedly financed the work; you are a great and humble sister. I acknowledge my other sisters Mrs. Adebayo, Mrs. Solomon, Seyi Oladejo for their love and support. I also acknowledge my brothers Mr. Ezekiel Oladejo, Mr. Toyin Oladejo and Mr. Segun Oladejo. I say thank you to all my friends too numerous to mention. Kingsley and Edet, thank you for been wonderful brothers and roommates. Kpam and Fred you're great.

I am grateful to my supervisor Mr. Abraham Usman for being such a wonderful humble man. He made the work much easier for me and all of us under him. He was completely accessible.

I want to specially acknowledge my loving fiancée, Miss Beauty Ogoh. Thank you for believing in me. You are a jewel indeed and I consider myself privileged to have you. I love you.

ABSTRACT

This project work encompasses the construction of a digital quiz decider circuit. The circuit can be used in quiz contests wherein any participant who presses his/her button (switch) before the other contestants gets the first chance to answer a question.

The circuit given here permits up to eight (8) contestants with each one allotted a distinct number (1 to 8). The display will show the number of the contestant that presses his switch first. Simultaneously a buzzer will also sound. Any other contestant that presses his switch after the first to press will have no effect on the display and the buzzer. Both the display as well as the buzzer has to be reset manually using a common reset switch.

In the unlikely event of simultaneous pressing (within few nano seconds difference) of more than one switch, the higher priority number (switch number) will be displayed and simultaneously the buzzer will sound. The buzzer as well as the display can be reset (to show 0) by momentarily pressing the reset switch so that the next round may start.

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CHAPTER ONE

1.0 INTRODUCTION

Integrated circuits (ICs) have had variety of applications in the design of digital circuits for various applications. To employ these circuits and other active and passive components in the design of a digital quiz contest decider is another ingenuity in the world of digital circuit design.

1.0.1 Digital logic states

In digital electronics there are only two voltage states present at any point within a circuit. These voltage states are either high or low. The meaning of a voltage being high or low at a particular location within as circuit can signify a number of things. For example, it may represent the one bit of a number, or whether an event has occurred, or whether some actions should be taken. The high or low states can be represented as true or false statements, which are used in Boolean logic.

1.0.2 Number codes used in Digital Electronics

i) Binary

Because digital circuits work with only two voltage states, it is logical to use binary number system to keep track of information. A binary number is composed of two binary digits, 0 and 1, which are also called bits (e.g. 0=low voltage and 1= high voltage).

ii) **BCD Code:**

Binary-coded decimal (BCD) is used to represent each digit of a decimal number as a 4-bit binary number.

iii) **Octal and hexadecimal:**

Two other number systems used in digital electronics include the octal and hexadecimal systems. In the octal systems (base8), there are 8 allowable digits whereas in the hexadecimal there are sixteen which include 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F.

iv) **Logic states:**

Logic gates are the building blocks of digital electronics. The fundamental logic gates include the INVERT (NOT), AND, NAND, OR, NOR, exclusive OR (XOR) and exclusive NOR (XNOR) gates. Each of these gates performs a different logical operation. There is also a switch and transistor analogy for each gate.

v) **Combinational logic:**

Combinational logic involves combining logic gates together to form circuits capable of enacting more useful, complex functions. Combining logic gates to design more complex circuits is the building stone of digital electronic circuit designs. This however, involves using intuition which is of course the bedrock of this project work: Digital Quiz Decider.

1.1 LITERATURE REVIEW

Over the years here has been increasing need and demand for a precision circuit, which could serve as a quiz circuit. This needed circuit upon design and construction should be able to meet a basic requirement. It should make possible at least a situation where a person could be singled out among a group of players in a game show or contestants in a quiz contest as the first person who knows the answer to a question or who wants to make a trial first before others.

Taking the advantage of advancement in technology that has brought about the availability of integrated circuit in their compact form and also the availability of other passive and active components, electronics circuit designers took up the challenge of designing a circuit that could perform the aforementioned function.

Mr. Anc made an effort in year 2003 at designing a 4-input circuit that could serve in part the aforementioned purpose, employing the user of CMOS ICs and light emitting diodes (LEDs). Whereas this circuit would be able to select a desired person out of four contestants, it didn't produce an audiovisual alert to that effect. Thus, it wasn't a very effective device for the required purpose. His work could be found at www.mitedu.freeserve.co.uk/circuits/misc/quiz.htm.

Another designer made an improved effort at designing one that could serve for eight (8) contestants and also produce an audiovisual display as well as a time out. He made use of semiconductor-controlled rectifiers (SCRs). However his display was a light effect by light emitting diodes with different colours for each team. His work is at Electronics Hobbyist Handbook, 1993, p33 and figure FE34-2.jpg.

All these left an opportunity for a research into designing circuit which would give a display of the actual number of the contestant who knows the answer first (decimal

display) as well as a sound alert while retaining both the sound and the displayed number until the game show host or quiz coordinator clears the display and the sound through the reset.

CHAPTER TWO

2.0 THEORY AND DESIGN ANALYSIS

2.1 PRINCIPLES OF OPERATION

The circuit (fig. 2.1) employs the use of momentary switches (push- to – on switches), Octal D type latch and FF (74LS373), 8- input NAND gate (74LS30), Quad 2- input NAND gate (74LS00), BC 558 pnp transistor, 3v-24v buzzer, priority Encoder (74LS147), hex inverter (74LS04), BCD- to- 7- segment Decoder / Driver, seven segment display (common anode) pull up Resistors (10k) ceramic and electrolytic capacitors.

Initially when the reset switch So is momentarily pressed and released, all the outputs of the Oct D type latch and FF (74LS373) go 'high' since all the input data lines are returned to Vcc Via resistors R1 through R8 (pull up resistors). All eight outputs of the transparent latch (74LS373) are connected to inputs of priority encoder, 74LS147, as well as 8- inputs NAND gate. The output of (74LS30) thus becomes logic O, which after inversion by NAND gate N2 is applied to latch-enable pin 11 of 74LS373, the transparent latch. With all inputs lines (or pins) of the priority encoder, (74LS147) being logic 1, its BCD output is 0000, which is being inverted by the hex inverter gate (74LS04) and then applied to 7- segment decoder / driver (74LS47) which decodes the BCD input into seven segment outputs. Therefore, on reset the display shows O.

When any one of the push-to-on Switches S1 through S8 is pressed, the corresponding output line of the transparent latch, 74LS373, is latched at logic O level, the priority encoder, converts its input lines into the BCD equivalent and after inversion by the hex inverter gate the BCD codes is being decoded by the 7- segment driver into seven segment code and the display indicates the number associated with the specific

switch. At the same time, output pin 8 of the 8-input NAND gate becomes high, which causes outputs of both gate N1 and N2 to go to logic 0 State. Logic 0 output of gate N2 inhibits the transparent latch (74LS373), and thus pressing any other switch S1 through S8 has no effect. Thus, the contestant who presses his switch first, jams the display to show only his number. Simultaneously, the logic O output of gate N1 drives the buzzer through PNP transistor BC 558. The buzzer as well as the display can be rest (to show O) by momentary pressing of reset switch S_0. that next round may start.

In the unlikely event of Simultaneous pressing (within few nano- seconds difference) of more than one Switch, the higher priority number (switch number) will be displayed. The block diagram and the circuit diagram of the Digital Quiz Decider is shown below:

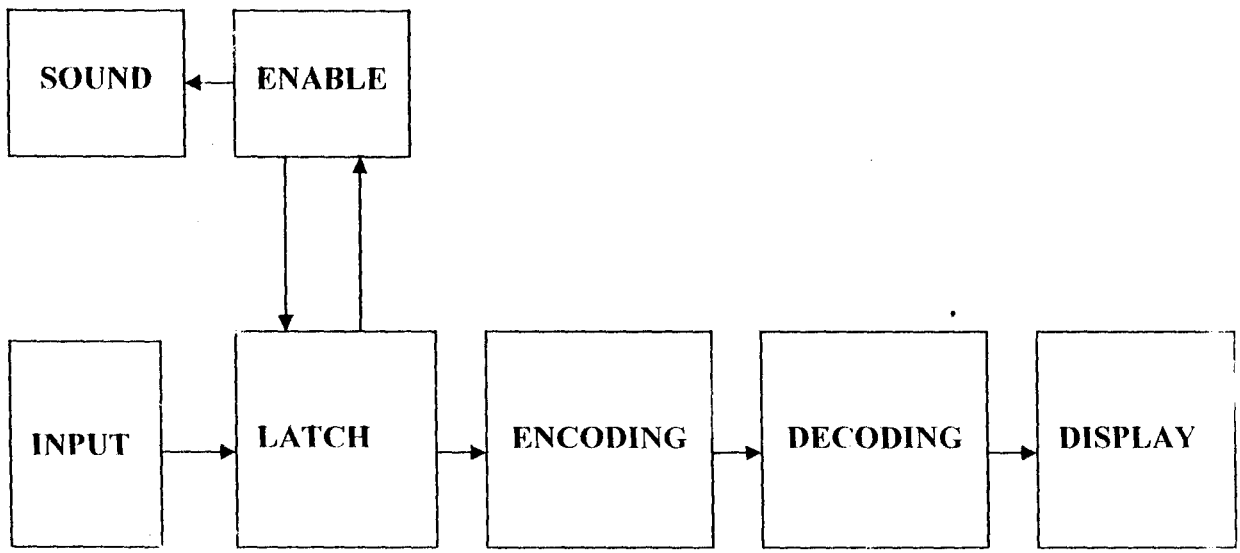
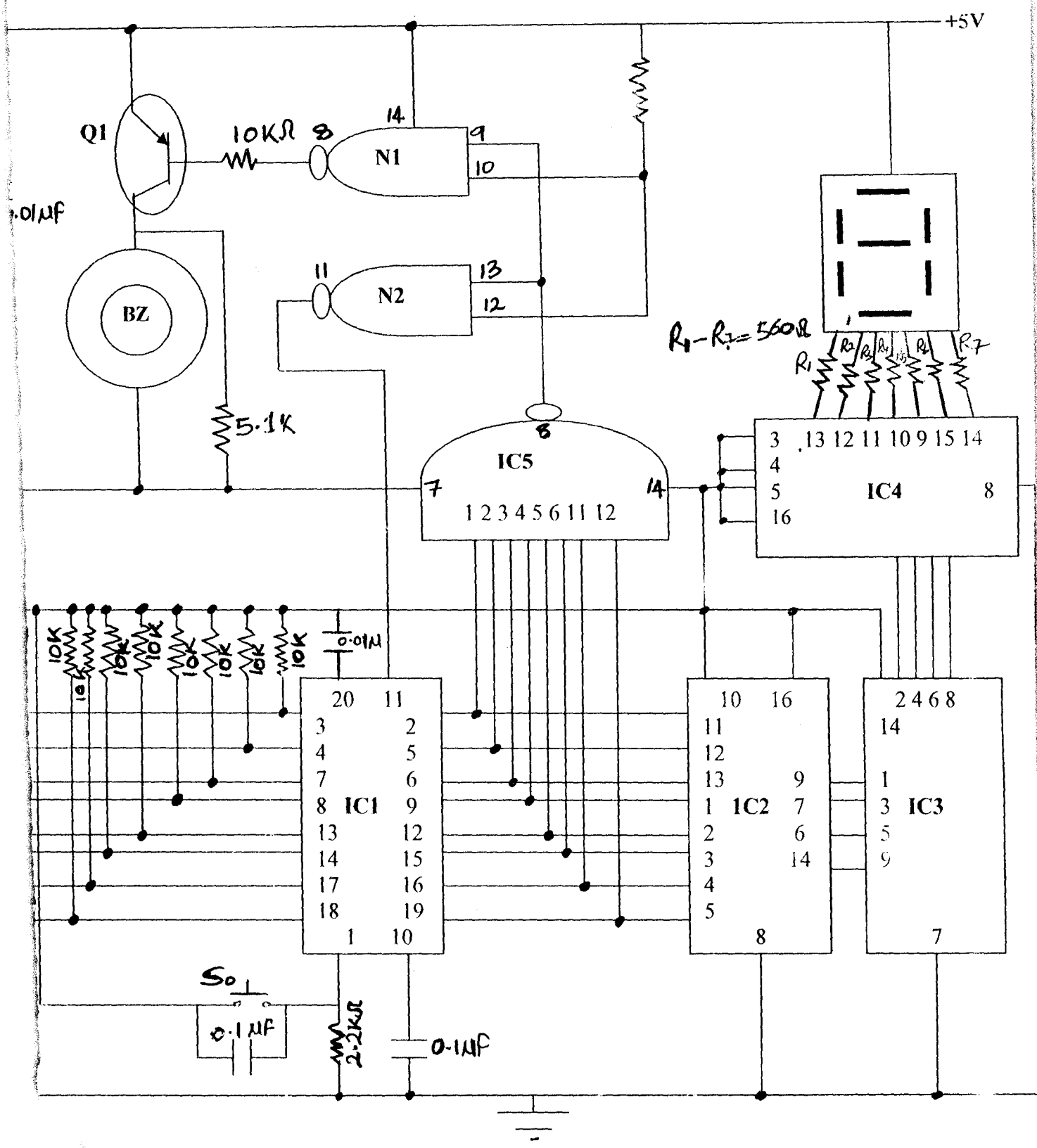


Fig 2.0 Block Diagram



KEY: IC1=74LS373 IC2=74LS147 IC3=74LS04 IC4=74LS47

IC5=74LS30 N1,N2=74LS00 Q1=BC558 BZ=Piezoelectric Buzzer

2.1 Circuit Diagram of Digital Quiz Decider

2.2 LOGIC FAMILY SELECTION

The integrated circuit devices on which modern digital circuitry depend belongs to one or other of several 'logic family'. The term 'logic family' simply describes the type of semi conductor technology employed in the fabrication of the integrated circuit. This technology is instrumental in determining the characteristics of a particular device which encompasses such important criteria as supply voltage power dissipation, switching speed, and immunity to noise.

The most popular logic families, at least as far as the more basic general purpose devices are concerned are the complementary metal oxide semi conductor (CMOS) and transistor - transistor logic (TTL). TTL also has a number of subfamilies including the popular low power Schottky (LS-TTL) variants. The transistor-transistor logic (TTL) family has been employed for this project due to the following reasons:

(a) They offer a good compromise between speed of operation and power consumption.

(b) They are commonly available (relatively) and at relative lower cost than other types.

© Powered by a regulated +5v, which can easily be designed and constructed using the regulator IC-7805.

3 POWER SUPPLY STAGE

Circuits usually require a dc power supply that can maintain a fixed voltage while supplying enough current to drive the load. This project certainly is not an exception.

The TTL family of IC employed in this project is powered by a regulated +5v supply (Vcc=+5v). The 74xx TTL series used will recognize a high input from 2.0 to 5v, a low from 0 to 0.8v, and a low output from 0 to 0.4v, hence a regulated 5v power supply was designed to meet the aforementioned power requirement of the project.

2.3.1 Step down

The voltage step down stage employs the use of a step down transformer (240/9v, 500mA). The supply mains ac. voltage was stepped down by the transformer and the output stepped down ac voltage at the secondary of the transformer was passed on to the rectification stage.

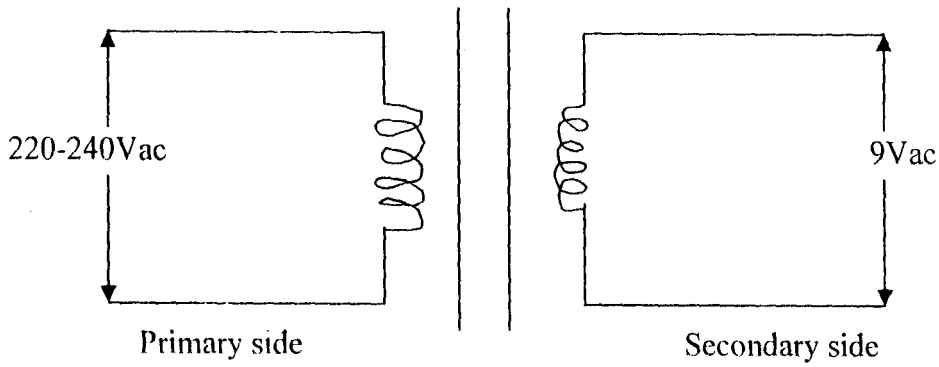


Fig 2.2 step-down circuit

2.3.2 RECTIFICATION

The bridge rectifier was employed for the rectification of the stepped down ac voltage. This converts the input ac voltage to equivalent ac voltage. It is shown in the figure below:

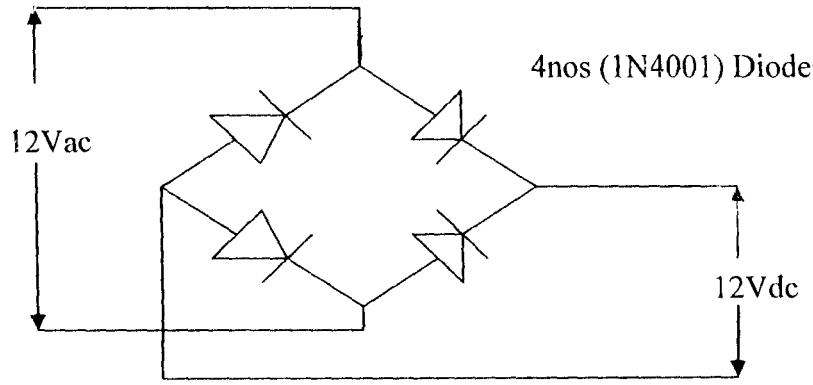


Fig 2.3 Bridge Rectification

2.3.3 FILTERING

The rectified voltage still contained some unwanted ripple voltage and this was eliminated using the electrolytic capacitor to filter out the ripples (smoothening) thereby producing a smoothened dc voltage. The filtering is shown below:

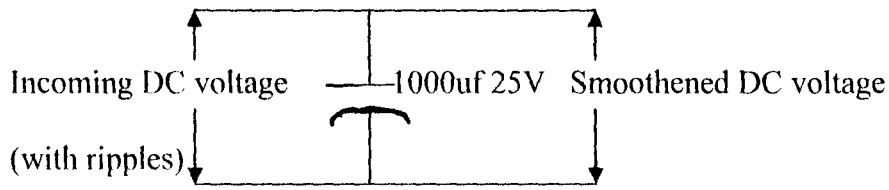


Fig 2.4 Filtering Circuit

2.3.4 REGULATION STAGE

The rectified and smoothened DC voltage is unregulated and needed to be regulated because in the unregulated form, it is unusable and possess damage to the circuit; hence the 7805 regulator IC was employed to regulate the incoming voltage. The regulation stage in shown below:

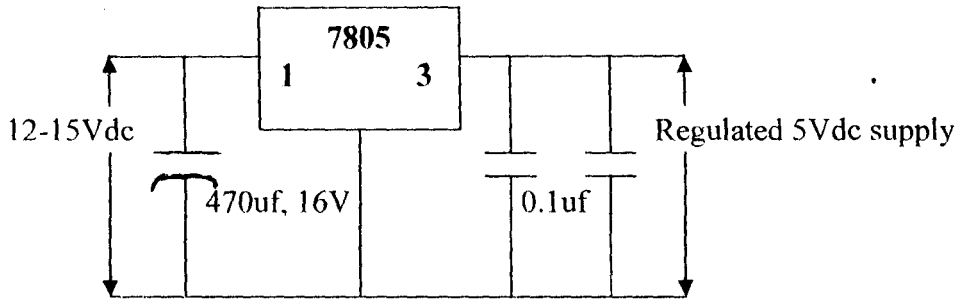
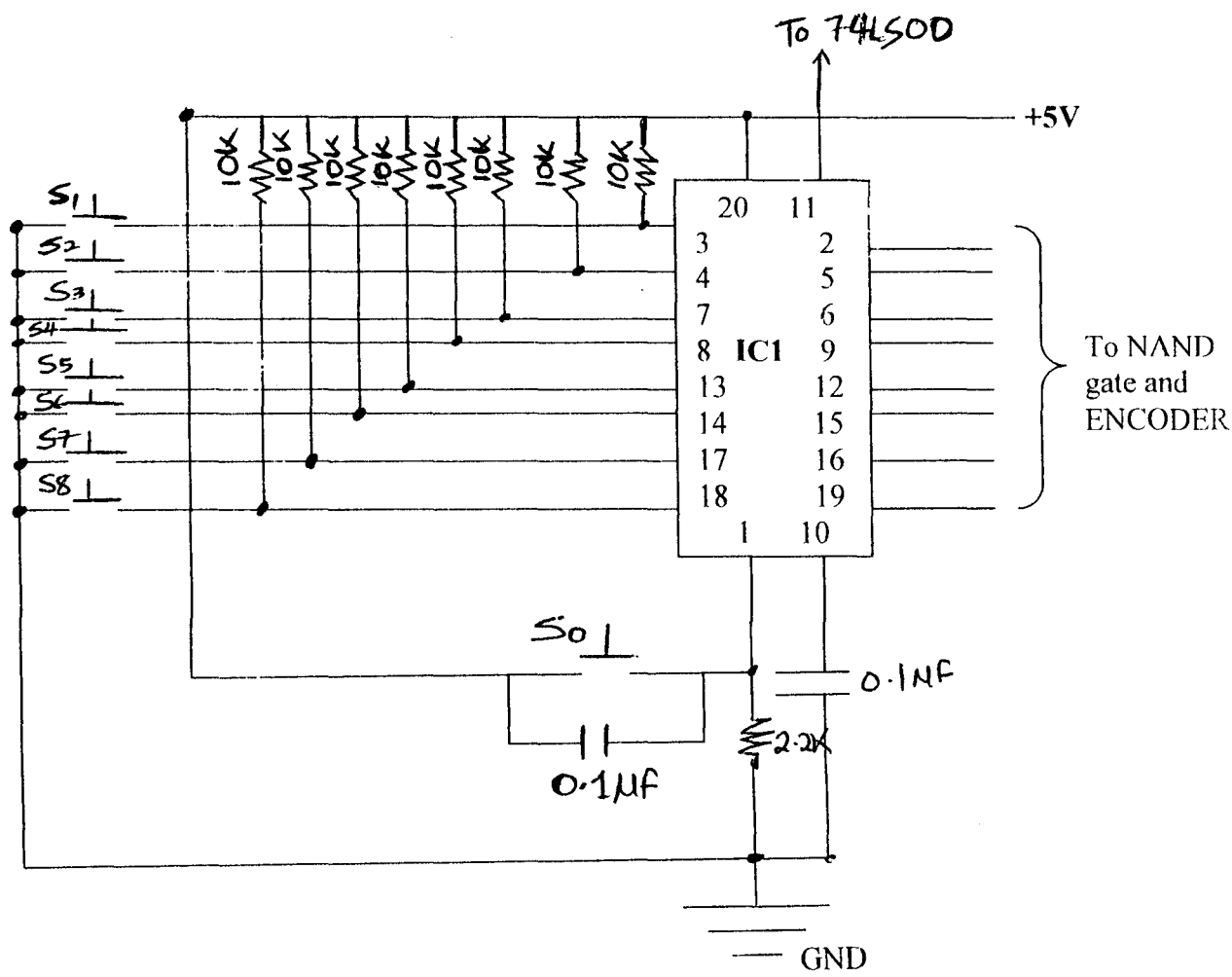


Fig 2.5 Regulation Circuit

2.4 THE INPUT STAGE

Switches 1 to 8 and the reset button (switch 9) forms the inputs to the circuit. The switches employed are the soft touch, push- to- on momentary, normally open type. Each of the 8-input lines to the octal D-type transparent latch are also connected via pull up resistors (R1 to R8) to the reset switch. The input lines are returned to Vcc via the pull up resistor on first powering the circuit irrespective of the whether the reset switch button is open or closed.

When any of the contestants switches 1 to 8 is pressed the corresponding bit pattern (8-bit) is sent through the switches to the required portion or other stages of the circuit for appropriate action. The work of the reset switch is to return the circuit to its original state. The input section is shown in fig2.6 below.



KEY: IC1=74LS373 (Octal D-type Latch)

Fig 2.6 Input Section

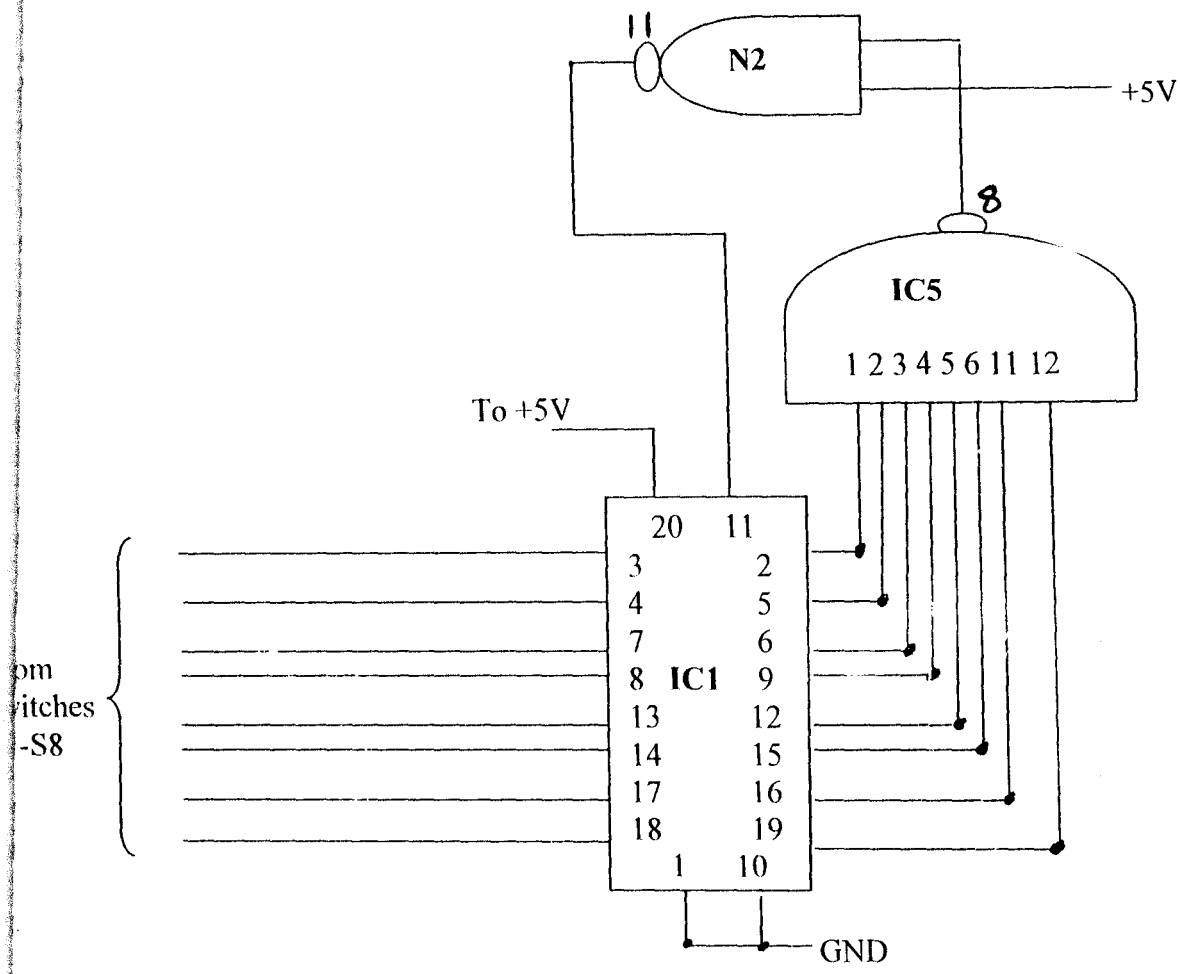
2.5 LATCHING UNIT

In this project, a three state octal latch or octal flip flop was employed at the latching stage of the circuit. The IC used is the TTL 74LS373, an octal D- type transparent latch. The IC contains eight D- type "transparent" latches. When its enable input (E) is high, the outputs (Q0-Q7) follow the inputs (D0-D7). This occurs only when all the inputs are high, that is, when the reset switch is pressed and all input lines are returned to VCC via the pull up resistors. When this happens, the output of the 8- input NAND

will be low and the corresponding output pin 11 of the Quad 2-input NAND (74LS00) will be high, thereby enabling the octal transparent latch.

When any of the switches 1-8 is momentarily pressed (i.e. pulsed low), the output of the 74LS30 (8-input NAND) is high and the output pin 11 of 74LS00 (Quad 2-input NAND) is low and so the latch enable pin E of 74LS373 is low.

When this occurs, data present at the inputs of the transparent latch are loaded into the latch. Since the latch is now disabled, any of the switches pressed afterwards will make no effect on the octal D-type latch. Furthermore, since when E is low the inputs are loaded into the latch, the display continues to retain the initial number displayed until the reset button (switch so) is momentarily pressed. The three–state octal transparent latch and flip flop (74LS373) therefore made a perfect latching device for this project since it has the ability to hold on to data present at its data inputs before transmitting the data to its outputs. This however, was the requirement of the circuit design. It was required that the display continues to hold the number displayed and the buzzer continued to sound until the quiz coordinator presses the reset button.
The logic symbol and IC package of the IC –74LS373 (octal D-type transparent latch and flip flop) therefore made a perfect latching device for this project since it has the ability to hold data present at its data inputs before transmitting the data to its outputs. Fig 2.7 shows the latching section.



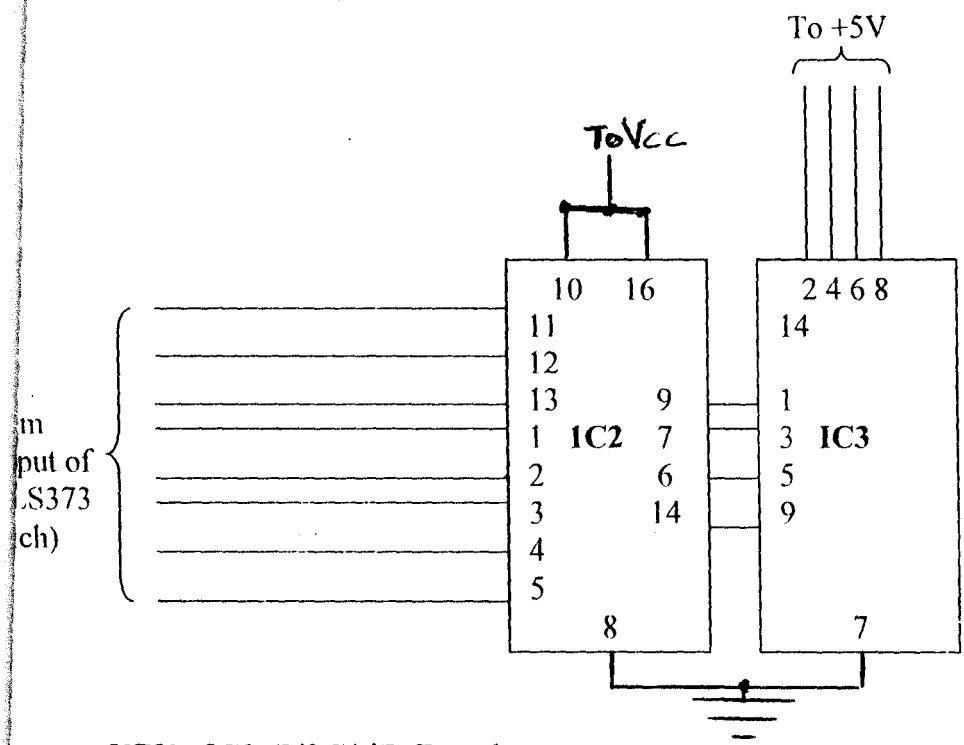
KEY: IC1=74LS373 IC5=74LS00 N2= 74LS00

Fig 2.7 Latching section

2.6 ENCODING STAGE

The encoding stage or unit of this project employed the use of 74LS147 TTL IC, which is a priority encoder. The logic symbol, circuit schematic and IC package is shown in figure below. An encoder generally is used to generate a coded output from a single active numeric input. The 74LS147 is a decimal – to BCD (10- line –to 4-line) priority encoder IC. It has active – low outputs. The IC encodes the keypad's input (switches 1-to 8) into its BCD (4bit) equivalent (negative logic).

When any of the switches is activated (in low state), the encoder generates the corresponding BCD (Binary Coded Decimal) of the logic inputs. The BCD output is then inverted and fed into a 74LS47 seven – segment LED display decoder /driver IC.



KEY: IC2=74LS147 (Encoder)

IC3=74LS04 (Inverter)

Fig 2.8 Encoding section

2.7 INVERTER STAGE

A hex inverter, 74LS04 IC, was applied at the inversion stage. An inverter was necessary since the output of the priority encoder is active low.

Four of the six-inverter gates in the 74LS04 IC were used and the rest left unconnected, this is allowed when using the transistor -transistor logic (TTL) IC.

The four-inverter gates convert the negative true logic output of the priority encoder into the positive true logic equivalent and then feed the seven-segment decoder/ driver. The hex inverter is shown in fig 2.8 above.

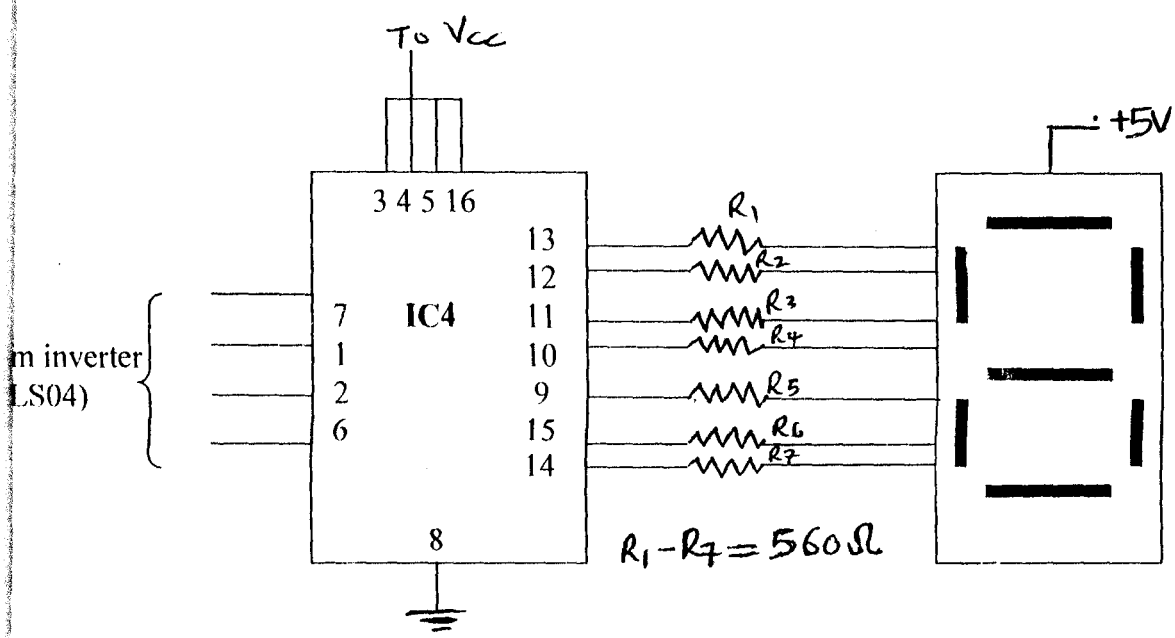
2.8 DECODING STAGE

A seven segment display decoder / driver IC, 74LS47 was employed for this stage of the project design. With this device (74LS47) more than one output can be driven low at a time, a characteristic that makes the 74LS47 different form other decoders. It is important that more than one output can be driven low at a time because it allows the 74LS47 to drive the seven –segment LED display used for th display part of this project design.

To create different numbers (contestant numbers) requires driving more than one LED segment at a time. For example in the fig below when the BCD number for 6 (0110) is applied to the 74LS47's inputs, all output except b go low. This causes LED segments a, b, c, d, e, f, g, to light up. The 74LS47 also sinks current through these LED segments as can be indicated by the internal wiring of the display itself.

The 74LS47 also comes with a lamp test active low input (LT) that can be used to drive all LED segments at once to see if any of the segments are faulty. The ripple blanking input (RBI) and ripple blanking output (RBO) can be used in multistage display applications to suppress a leading – edge and/or trailing edge zero in a multi digit decimal. However, for this project design, the LT, RBI and RBO pins are grounded.

When any of the input is pulsed low (that is momentarily pressing of any of switches 1to 8) the display decoder/ driver converts the BCD equivalent of the encoded input into a seven-segment display form. The fig 2.9 shows the decoding section



KEY: IC4=74LS47 (Decoder)

Fig 2.9 Decoding Section

2.9 THE DISPLAY UNIT

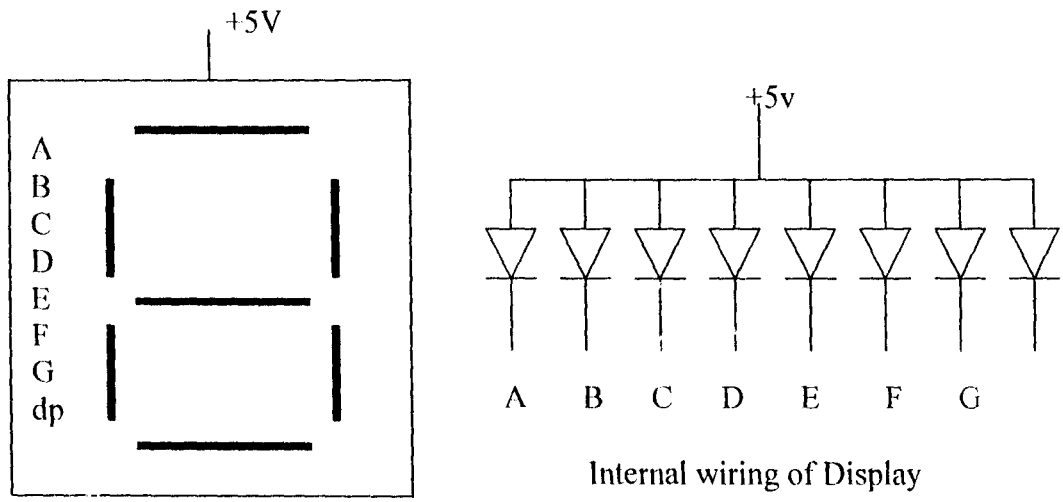
The display unit used in this project is the common anode seven – segment LED display. It is a simple display that can display the digits 0-9.The display readout is driven by the BCD to seven segment decoder / driver (74LS47) with active low inputs that apply a low voltage to the cathodes of the segments to be activated.

The cathodes are connected to the active low outputs of the 74LS47 decoder IC through current limiting resistors. When pulses are being sent from the inputs

switches, the desired segments of the display are activated and it displays the corresponding number of the switch being pressed.

The anodes of all the seven segments are tied together and connected to the VCC.

The seven- segment LED indicator arrangement and internal wiring is as shown below.



Common Anode Display

Internal wiring of Display

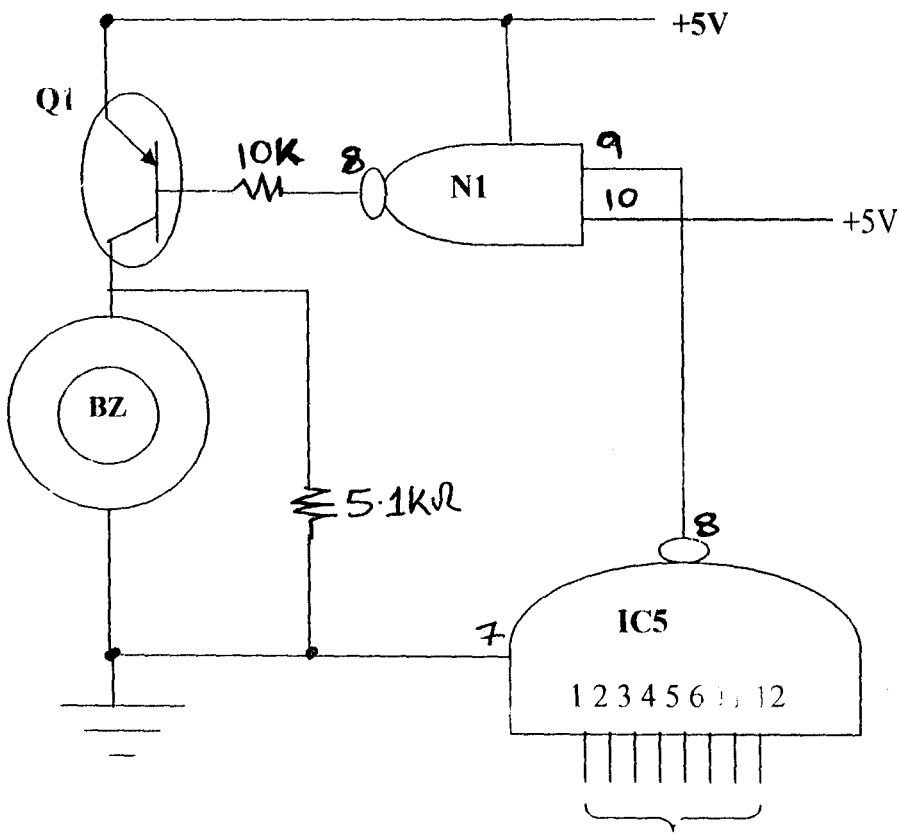
Fig 2.10 Display section.

2.10 SOUND STAGE

A piezoelectric buzzer was employed at this stage of the circuit design. The buzzer is rated 3-24V. Normally a buzzer sounds when the voltage across it is higher than its rated voltage. Therefore, since the circuit in power by 5V, the buzzer rating is adequate.

When any of the contestant presses his switch, the output of the 8-input NAND becomes high and this drives the output pin 8 of the quads 2-input NAND gate (74LS47) low. The low pulse drives the buzzer ON through the

pnp transistor, BC 558. Therefore, a buzzing sound (continuous due to the latch) is produced simultaneously on pressing (the first press) any of the input switches. The sound stage or unit in shown below:



KEY: BZ1= Buzzer Q1=BC 558

IC5= 74LS30 (8-input NAND gate)

Fig 2.11 Sound stage

CHAPTER THREE

3.0 CONSTRUCTION AND RESULT

3.1 CONSTRUCTION

In carrying out (successfully) the construction of the digital quiz decider several steps were taken. These meticulously observed steps at corresponding stages are analyzed below.

3.1.1 SIMULATION:

The very first step taken before embarking upon purchase of components and eventual construction was simulation. This was to ensure that the circuit worked before embarking upon further work. The simulation software employed includes the E DA workbench, then the Multisim package (both textbook and professional editions) and finally the circuit maker. During the various simulations (almost countless) carried out several ideas were examined and their workability tested with the different software. None of the simulation software seemed to provide the adequate result required. It later resulted to simulating the entire circuit in parts during which some reasonable results were obtained using the circuit maker software. Finally having been convinced about the workability of the circuit irrespective of the software's deficiencies, work proceeded to the other stages of the construction.

3.1.2 Prototype

Upon purchase of the various components needed for the construction of the digital quiz decider circuit, a model was there after made on the breadboard. This was carried out with the aid of the following tools:

(i) **Breadboard**: the panel or bench on which the circuit was built.

(ii) **Jumper wires**: the connecting wires used for routing signals and current in and around the board.

(iii) **Compact power supply unit**: used_for temporary powering of the model circuit

(iv) **Cutter/ pliers:** for wire cutting purposes.

3.1.3 Component layout:

Just about the commencement of the permanent hardware construction of the entire circuit on the Vero board, a careful planning of the component layout was carried out. This was necessary so as to minimize error, simplify wiring, make troubleshooting easier and enhance the overall readability and understandability of the circuit on the board. To achieve these, the following steps were consequently carried out.

(i) The IC sockets to sit each IC was positioned to almost perfectly follow the circuit diagram such that the one that was to be at the output (i.e. connected to) was placed immediately after it. By so doing, the various stages of the circuit were clearly shown

(ii) The pin configurations of the ICS were made to be consistent with one another.

(iii) Adequate and sufficient spaces were kept in between ICs and components generally.

(iv) Similar components or rather components serving similar functions like pull up resistors were aligned together.

(v) The leads of components like resistors, capacitors and transistor and switches were cut down to manageable lengths so as to avoid short circuit.

3.1.4 Construction Tools:

For the hardware realization of the circuit, the following construction tools were inevitably employed:

(1) Vero board: This is the panel on which all the various components were interconnected and the entire circuit mounted upon.

(2) Coated Copper wire: This was obtained from the winding of a transformer. It was coated with insulator, but when scraped at the edges it was used for interconnection between the necessary parts of the circuits.

(3) Soldering Iron and Lead: A 60w soldering Iron and alloy flux lead were used for the soldering requirement of the circuit.

(4) Razor blade: was used for scrapping the edges of the coated copper wire to allow for continuity.

(5) Digital Multimeter: This was significantly used throughout the entire project period for mainly continuity test, voltage measurement, and resistance measurement and buzzer test.

(6) Lead Sucker was used to remove desoldered lead away from the board.

(7) Pliers /Cutter: was employed for most cutting requirement with knife.

3.1.5 HARDWARE CONSTRUCTION

This involves the entire hardware realization and project design work on the permanent board – the Vero board. The key pad generating the input signals were soldered on one separate board, the display unit on another and the other parts of the circuit which include the latch, encoder and decoder, buzzer unit and the power supply unit on the third separate board.

The adequate pins of the ICS were well connected together with the aid of the copper wire (coated but scrapped at the edges). All the leads of the components were firmly and adequately soldered to the Vero board. No IC was left on the IC socket during soldering in order to prevent damage due to excessive heat. Moreover, the soldering was carried out mostly in the night when the power supply voltage is high and stabilizer was used sometime to regulate the voltage supply. All this was to enhance quick heating of the soldering iron. Also during soldering and coupling all the pins of the components e.g. the transistor were clearly identified before soldering and this prevented a lot of desoldering thereby enhancing neat work.

3.1.6 PACKAGING

The packaging was done with a combination of straw board, embossed cardboard and glossy cardboard. This is because one, the project is a model presentation and secondly it's cost effective while achieving a neater presentation compared to wooden or metallic substitute.

3.2 TESTING/RESULT OBTAINED.

Testing was carried out on the various stages of the design after the final soldering and the following results were obtained at the stages.

(1) Continuity: All the interconnected parts of the circuits were discovered to be well connected and one point was continuous to another.

(2) Power supply unit: the output of the regulator IC 7805 was tested and was discovered to give 5v as required and so the correct powering of the circuit was well assured and confirmed.

(3) Input stage: before any of the switches was closed, the entire circuit was on logic level 1(high or +5v). On pressing any of the keypad switches the corresponding input line into the latch IC [74LS373] was driven low with the other remaining high. When the reset switch was pressed the circuit returned to the previous high state.

(4) Latch stage: It was obtained that the logic state of the output of the transparent data latch IC remained the same after pressing and releasing,any of the 8 input keypad switches and only changes state when the reset in closed.

(5) The buzzer stage: the output pins 8 and 11 of the 74LS00 IC (quad 2- input NAND gate) are and remained at logic O anytime any of the keypad switches in closed, thereby powering on the buzzer through the PNP transistor BC 558 and also disabling the latch IC (74LS373) through the pin 11 signal. The buzzer also remains ON until the reset button or switch is pressed.

(6) Encoding / decoding stage: The priority encoder IC, 74LS147 generated the required BCD equivalent of the logic inputs applied to its input from the latch. The inverter inverted the generated BCD code and the BCD to seven-segment decoder enabled its corresponding output pins.

(7) Display Unit: The number corresponding to the switch pressed or closed was displayed on the seven-segment display and remained there until reset switch was pressed.

(8) The Result: The buzzer continued to sound and the number retained on the display until the reset switch was pressed after which the buzzer stopped and the number on the display was also cleared to zero.

3.3 DISCUSSION OF RESULT

All the results obtained at the various stages were the accurate and expected results to be obtained. It was then clear that on first pressing any of the switches, the buzzer sounds and the corresponding number of the switch is displayed on the display. In this way the quiz coordinator is alerted by the buzzer sound that someone has already pressed his switch and he sees the number of the person through the visual display. This sound and the number remains and only the quiz coordinator who has the reset button has the sole right and ability to stop the sound and clear the number and also calls on the contestant who pressed his switch first to answer the question. Any effort by any of the other contestants to force their own number on the display or produced their own sound would be totally frustrated by the machine, since the circuit only recognizes the very first press of the switch. Therefore, the results obtained were perfect and accurate and would serve its overall purpose.

3.4 CHALLENGES ENCOUNTERED

The major challenges faced were one, the difficulty of obtaining or purchasing components and secondly where it is available getting a functional one. Searches were carried out in five different cities including Minna, Kano, Kaduna and Abuja before obtaining the priority encoder IC used (74LS147) and was extremely relatively expensive.

Another challenge was that of obtaining the other components at relatively more expensive prices in Minna due to monopoly compare to what is obtainable in other cities like Lagos.

CHAPTER FOUR

4.0 CONCLUSION AND RECOMMENDATION

4.1 CONCLUSION

The aim and objective of this project work; the design and construction of a digital quiz decider, which is to provide a means by which a group of contestants could be subjected to equal test of their intellect as a way of answering the same question under the same subjected condition has been achieved.

With this machine the era of subjecting contestants in quiz contest to unequal and unjust test of their intelligent quotient by a way of asking them different questions at the same space of time or giving the whole lot a particular question to answer within a specified time frame is gone. Now we can know who exactly got the answer first and the actual nano second he got it.

4.2 RECOMMENDATION

For adoption and use this circuit is recommended in all secondary schools for the purpose of conducting quiz competition for their pupils. It is also recommended to JETS (Junior Engineers Technicians Scientists) and STAN (Science Teachers Association of Nigeria) and all intellect quotients testing body for use in order to achieve precision in their judgments. This would also benefit the IRS airlines as a substitute for what they are presently using in conducting their quiz contest.

For general improvement on the design the following recommendations could be considered:

(1) Various colour combinations of light emitting diodes could be used as the seven-segment display for colour effect and more beautiful display.

(2) The latching stage could be removed from the design. When this is done, cashiers could adopt it for use in banks in order to alert their customer in the queue of which particular cashier is free to attend to a customer. The cashier's number is displayed on the display and it disappears immediately so that any other free cahier can call for attention of the customers.

REFERENCES

1) www.epanorama.net

2) www.mitedu.com

3) www.electronicskits.com

4) www.aaroncake.net

5) www.discovercircuits.com

APPENDIX

BILL OF QUANITY

S/NO	ITEMS	QTY	UNTIY PRICE	TOTAL AMOUNT
1.	Casing and Accessories			
2	74LS147	1	₦1,700	₦ 1,900
3	74LS47	1	₦ 230	₦ 230
4	74LS30	1	₦120	₦ 120
5	74LS373	1	₦250	₦ 250
6	74LS00	1	₦120	₦ 120
7	74LS04	3	₦90	₦ 270
8	7 Segment display	1	₦250	₦ 250
9	Buzzer	1	₦120	₦ 120
10	Transistor	13	₦20	₦ 260
11	Resistors	20	₦20	₦ 400
12	Momentary Switches	12	₦30	₦ 360
13	Capacitor (Ceramic)	4	₦20	₦ 80
14	Electrolytic capacitors	4	₦30	₦ 120
15	Vero board	2	₦50	₦ 100
16	Breadboard	1	₦600	₦ 600
17	Soldering iron	1	₦120	₦ 120
18	Lead sucker	1	₦100	₦ 100
19	Lead	8	₦20	₦ 160
20	Connecting Cable	10	₦20	₦ 200
21	Transformer	1	₦150	₦ 150
22	IC Sockets	7	₦20	₦ 140
23	Digital Multimeter	1	₦600	₦ 600
24	7805	1	₦50	₦ 50
25	Toggle switch	1	₦50	₦ 50
26	Power cord	1	₦50	₦50
27	Packaging		₦500	₦500