DESIGN AND CONSTRUCTION OF A DIGITAL PUBLIC CLOCK

By Albishir B. Aduwu (2004/18776EE)

A Thesis submitted to the Department of Electrical and Computer Engineering, Federal University of Technology, Minna.

DECEMBER 2009.

Dedication

This project is dedicated utter mostly to the Almighty God for giving me the opportunity, physical, and mental ability to be able to execute this project.

This project is also dedicated to my parents Mr. and Mrs. Mark M. Aduwu, for their loving support throughout my course of study and life generally, together with the effort of my other family members as follows;

Mr. and Mrs. Meshack Aduwu
Mr. and Mrs. Danladi Aduwu (Eazy)
Mr. Reuben A. Aduwu (Eljay)
Miss Grace G. Aduwu (G – Race)
Mr. Josiah U. Aduwu
Mr. Dikum M. Aduwu
Miss Dorcas A. Aduwu,
And my supporting uncle Mr. Paul Aduwu,

Including all otlier family members not listed above. I would also like to include the following families;

Mr. Blaise (late) and Mrs. Blaise Adu and family
Mr. and Mrs. Bulus Boto and family
Mr. Barnabas (late) and Mrs. Barnabas Dama and family, particularly Mr. and Mrs. Samuel D. Dama
Mr. and Mrs Sunday Agai and family, particularly Mr. Stephen A. Agai (Stvnolysis) who is like an extra heart, and who is my partner in a lot, except crime.

I would also like to mention the following for their support;

Mr. Boman Avong
Mr. Christopher Enaboifo
Mr. Ahmed B.Alaga
Mr Yahaya Jibrin
Mr. Godwin Aboi.

Declaration

I, Albishir B. Aduwu, declare that this work was done by me and has never been presented elsewhere for the award of a degree. I also hereby relinquish the copyright to the Federal University of technology, Minna.

Mr. Albishir B. Aduwu
Name of student

21/12/2009.
Signature / Date

Dr. E. N. Onwuka
Name of Supervisor

02/02/10
Signature / Date

Dr. Y. A. Adediran
Name of H.O.D

(May 6, 2010)
Signature / Date

Name of External Examiner

09/02/10
Signature / Date

Acknowledgement

Firstly I would like to acknowledge the source of financial input to this project, The Aduwus, particularly Mr. Reuben Aduwu who contributed immensely in funding this work.

I would also like to acknowledge the staff of the Electrical and Computer Engineering department, F.U.T Minna for their individual contributions in imparting knowledge to me that led to the success of this project, particularly my project supervisor Dr. E. N. Onwuka, who ensured each part of this work was promptly and by standard completed, as well as my technical supervisor Mr. Umar Abubakar for all his input and assistance.

Abstract

The project is a public digital clock with a display board of four 7-segment light grid measuring about 5 feet by 2 feet, and an hourly tone.

The display is made by an arrangement of high intensity light emitting diodes (LED) in four 7-segment patterns mounted outdoors on a high elevation which can be seen, and the time read off from several hundreds of meters away in a clear line of sight.

The unit is also equipped with a pulse tone that is also produced after every hour, which can be heard several meters away.

It is powered by an a.c mains supply and equipped with a battery backup to maintain continuous operation of the timing circuit in the event that is a powering outage which is expected, but not supposed to occur. The battery backup is not wired to power the display during power outages because of the size of the display which will consume much of the batteries energy if the power outages are extended over a long period. When the mains power is restored, display of the correct time continues.

The clock time can be set by a wired panel that can be mounted within an indoor location. The setting panel also displays the time on a smaller display attached to it so that setting of time can be done without having to stand in front of the public display.

Table of Contents

Chapter Four: Tests and Results

Chapter Five: Conclusion

Appendices:

CHAPTER ONE: Introduction

1.1 Historical Background :

In the early generation, people were limited in ascertaining the accurate time of the day. One way was by looking at the position of the sun and telling what period of the day was present. Such statements were made as "at sun rise", "at mid-day", or "at sunset". As technology grew, the **'sundial'** came into existence, which was one of the first forms of technology. The device had a calibration of the twelve hours of a clock on a round wooden face, as well as the four cardinal points, and a protruding bar at its centre called a **'gnomon'**.

The cardinal points were pointed in their respective directions, and whenever the sun shines on the sundial, the shadow of the **'style'** (which is the edge of the gnomon) casts on the face to give the hour of the day [1,2]. Another means of timing used was the **' hour glass '**, a device in which free flowing sand was filled in two funnel-like glass chambers connected at their vertices with narrow openings, and sealed at their bottoms so that when the device was inverted, the sand flows completely from the upper chamber to the lower through the opening by force of gravity, in approximately one hour, hence its name the 'hour glass'. Though it is generally called the hour glass, other constructions exist between 15 minutes to 4 hours. [3, 4]

Another type of clock, which is the known most accurate clock in the world is the **'Atomic Clock'**. [5] states that "On December 29, 1999, the United States National Institute of Standards and Technology unveiled the NIST F-1, the most accurate clock in the world (a distinction it shares with a similar device located in Paris, France). NIST F-1, an atomic cesium fountain clock, replaces the NIST-7,

which served as the primary United States time standard from 1993 to the end of 1999. The new atomic timekeeper is so accurate that it could run for nearly 20 million years without gaining or losing a single second. The clock is called a fountain clock because it measures the light emitted by super-cooled cesium atoms as they fall through a microwave cavity".

The next generation of clocks was the mechanically driven type. Mechanical clocks and watches are powered by a mainspring, which must be wound periodically to provide energy to drive the clock. The force from the wound mainspring drives the power wheel, which transmits motion through a series of pinion gears to the hour wheel and the minute wheel. The escapement wheel slows and regulates the motion of the power wheel. The motion of the escapement is regulated by the back and forth movement of the pivot. This motion also produces the familiar "tick-tock" of a clock and ensures that the hour and minute hands keep accurate time. [6]

The modern day electronic clocks have changed the means of telling time by showing time more conveniently and accurately up to fractions of the hour. The digital clock is even more readily read, as it displays the time by the numbers themselves.

1.2 Objective of the Project

The project is aimed at giving a very large population of the public the correct time of the day, and to inform them periodically that an hour has passed, by an audible tone. This will help people keep track of their planned activities. In a school environment, it will very much remind students and lecturers when a period has elapsed, so as to meet-up to other lecture periods, and avoid intrusion of lecture hours by other lecturers.

Similar clocks exist in various locations of the world. One example is the famous **'Big Ben'**,(believed to have been named after Benjamin Hall, first Commissioner of works when the bell for the clock was made). The clock is an analogue type, and of a larger scale (7 m diameter), mounted on the Palace of Westminster Tower, London. The clock strikes a bell measuring 2.7m wide and 2.3m tall within the tower to produce an ' E ' note every hour [7, 8]. Another public clock is the remarkable ' Water Display ' digital clock outside Kanazawa Station Fountain, Japan [9].

A similar circuit for the project was designed in [10], but with the limitation that it always had to be connected to an alternating current (a.c) mains supply to receive and process its clocking signal, that is, it did not have its own pulse generator, therefore, each time there is any power outage or cutoff, the clock needed to be reset whenever power was restored. It was also not designed to be displayed on a large LED grid display board. It also did not have an hourly tone.

1.3 Methodology :

The project was built according to the circuit diagram in chapter three, on a project board, with four small conventional 7-segment LED displays sold at electronic component stores, and pulsed by a 1Hz quartz circuit. The circuit was tested long enough with the correct voltage for several days, and for a more accurate test, several months. After achieving accurate results, the display board was built to the desired size and boldness of the digits to be displayed, and then tested with the timing circuit. The overall connections was housed in a suitable aluminum / acrylic or plastic casing, depending on the mounting location and the cost of the casing

materials, because each casing's resistance to environment conditions varies.

1.4 Sources of Materials:

All the electronic components used in the project were obtained in Nigeria, within the electronic component stores / shops.

The parts used for the frames and casings for the project were also obtained in some hardware stores within the country, such as the acrylic plastic sheets, which can be obtained from the suppliers of sign board materials. The aluminum (angle 90 beam) obtained from suppliers of aluminum window and door materials. Rivets, screws, and silicone paste (for sealing) can be obtained within any hardware shop, especially those who sell workshop tools.

The 1Hz oscillator chip if not found in electronic component shops can be salvaged from any old wall clock circuit, and the necessary terminals determined.

CHAPTER TWO: Theoretical Background

2.1 Early Electronic Devices:

2.1.1 The Vacuumed Tube:

This is a device first built in 1904 by Sir John A. Flemming of Britain [11]. The device was the forerunner of the diode. It operated by allowing electrons to flow from the negative electrode to the positive, and for this reason, he named it 'The thermionic valve', similar to the way a mechanical valve operates, by allowing fluid to flow only in one direction.

More work was done on the device by De Forest of the United States, when he discovered the addition of a third electrode to control the current flowing through the device. This modification he called **'the audion'** [12], which gave rise to the amplifier, and radio communication, after further advancements.

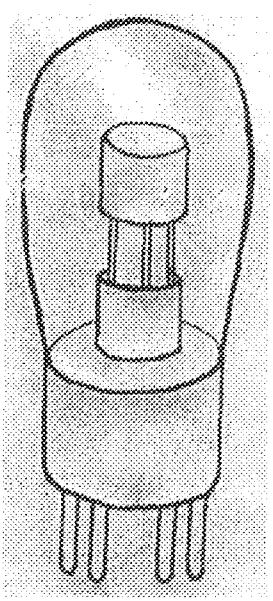


Figure 2.1 The Vacuumed Tube

2.1.2 The Transistor:

The device was first built by three scientists; Bardeen, Brittain, and Shockely working with bell laboratories (U.S.A) in 1947 [13].

It has replaced the vacuumed tube in almost all applications because of its greatly reduced size and power consumption. The device in its basic form has three terminals commonly the **'base' (b)**, for current control, the **'collector'(c)**, the **'emitter' (e)**, in which the last two form the current channel. Most commonly, the basic transistor exists in two forms, namely; the **NPN**, and the **PNP**, and can be made from silicon or germanium.

The NPN type is controlled by a positive 'P' voltage at its base and provides a negative channel for the flow of current, while the PNP type is controlled by a negative 'N' voltage at its base, and provides a positive channel for current flow.

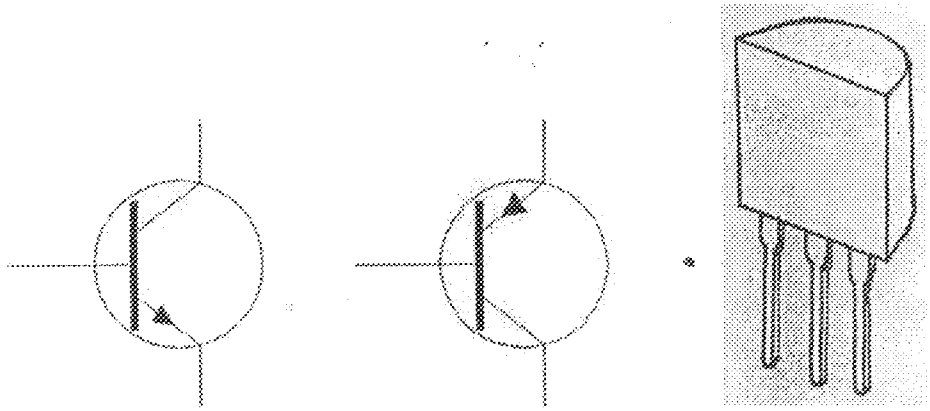


Figure 2.2; The NPN transistor symbol **(a)**, the PNP transistor symbol **(b)**, and physical appearance (TO - 92 I.C package) **(c)**.

The basic function of the transistor is to work as a current amplifier, it operates in the **linear region**, whereas when working as a switch, it operates in the **cutoff** and **saturation region**.

The operation as a simple amplifier using an NPN can be understood as follows:

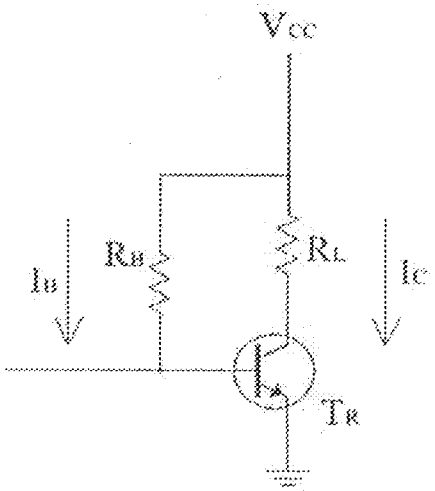


Figure 2.3 ; Biasing the NPN transistor.

The current (I_B) is given as ;

$I_B = (V_{CC} / R_B)$ Ampere, where; V_{CC} is the supply voltage, and R_B is the base resistor (biasing resistor), and neglecting the voltage drop in the base emitter junction (0.6v for silicon, and 0.3v for germanium).

The collector current (I_C) can be obtained by;

$$I_C = \beta I_B \text{ (Ampere).}$$

Where β is the gain factor for the particular transistor, also indicated as h_{FE}.

The voltage drop (V_{RL}) across the load resistor (R_L) is given as;

$$V_{RL} = I_C R_L \text{ (Volts)}$$

The voltage drop along the transistor channel (V_{CE}) is given as;

$$V_{CE} = V_{CC} - V_{RL} \text{ (Volts)}$$

[14] states a **"load line"** is sometimes plotted over a transistor's characteristic curves to illustrate its range of operation while connected to a load resistance of specific value:

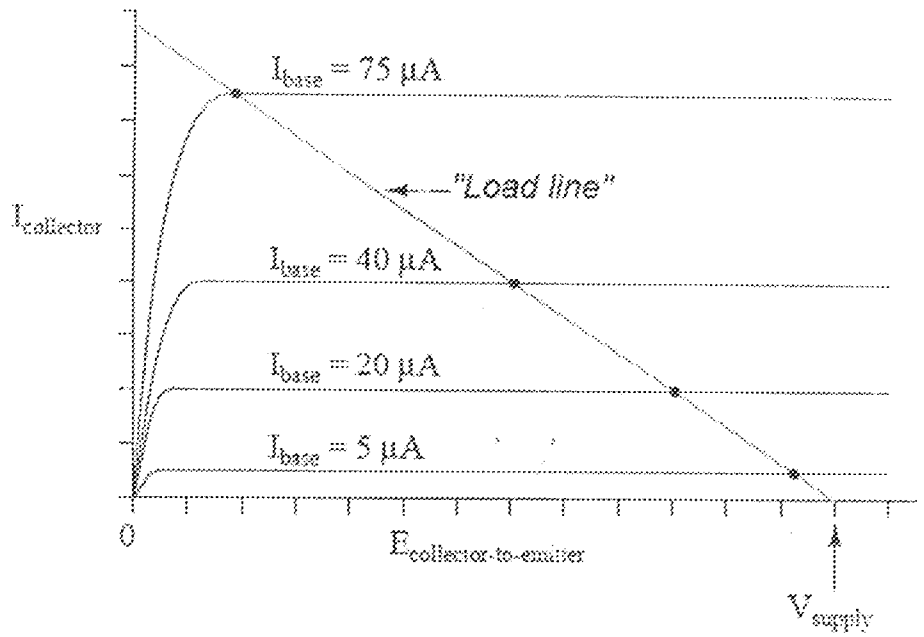


Figure 2.4 Transistor I – V characteristic

A load line is a plot of collector-to-emitter voltage over a range of base currents. At the lower-right corner of the load line, voltage is at maximum and current is at zero, representing a condition of cutoff. At the upper-left corner of the line, voltage is at zero while current is at a maximum, representing a condition of saturation. Dots marking where the load line intersects the various transistor curves represent realistic operating conditions for those base currents given.

2.1.3 The Integrated Circuit (IC)

This device incorporates many of the discrete transistors to a single very small package. [15] States that work done by Jack Kilby of Texas Instruments, (U.S.A) led to the development of integrated circuits in 1958. Integrated circuits are complex combinations of several kinds of devices on a common base called substrate, or on a tiny piece of silicon. They offer low cost at a high performance, good efficiency,

small size, and better reliability than an equivalent circuit built from discrete parts.

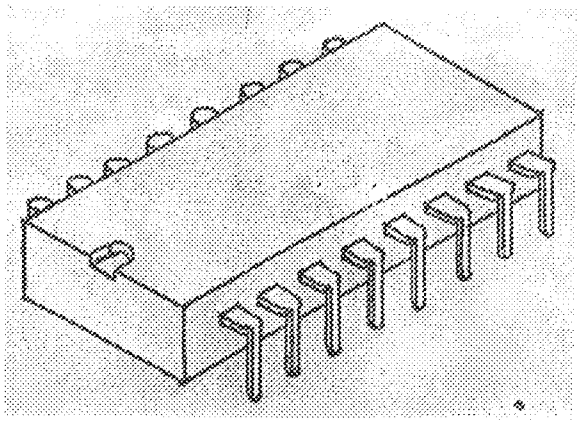


Figure 2.5: An 8-pin Dual in line package (DIP) IC.

2.2 Basic Digital Clock Architecture:

[16] The basic digital clock architecture is summed up in the block diagram of figure 2.6

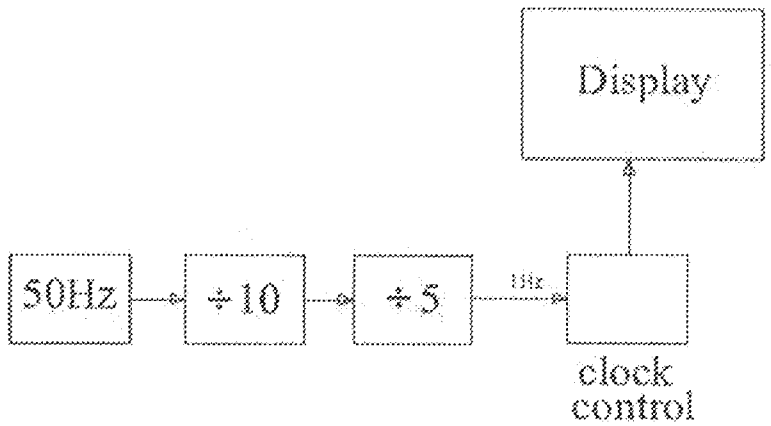


Figure 2.6; Basic Digital Clock Architecture

2.2.1 The 50Hz Time Base:

This part of the circuit is usually obtained directly from a stepped down a.c mains supply of 50Hz, and the signal shaped to square wave, and sent to the 'divide by ten' (÷10) counter.

2.2.2 The Divide by counter (÷X):

The 'divide by' counter is usually a package with the ability to be connected in various configurations to achieve various 'divide by' operations. The first stage of the basic digital clock is connected in a basic divide by ten configuration, which divides the 50Hz signal to 5Hz. This signal then passed to another counter with a divide by 5 (÷5) configuration to produce 1Hz pulses. The pulses are then fed to the clock control (also made of different divide by counters connected together).

2.2.3 The Seven Segment (7 - Segment) Display :

This is a digital display device made from seven light emitting diodes (LED) arranged in segments to form numbers 0 through 9 when lit-up in the specified manner. The device configuration are of two types; the **common anode**, and the **common cathode.** [17] states that to operate the common anode LED display, all anode terminals must be supplied by a positive voltage of 5v together, and for a number to light, the correct cathode leads must be connected to the ground.

A resistor is usually connected in series with each segment to limit the current flowing into the segment.

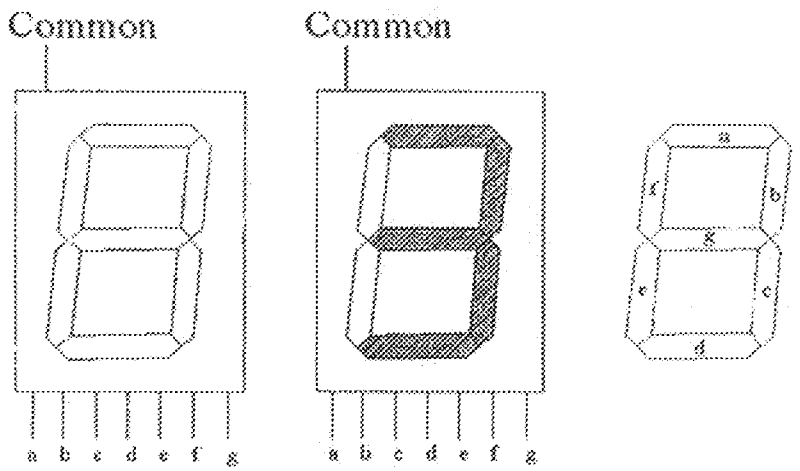


Figure 2.7; The Seven Segment Display.

2.3 The Project Components:

2.3.1 The 7447 Integrated Circuit (IC):

The 7447 integrated circuit is a binary code decoder / LED driver. [18] states that its output are buffered to a voltage level of 15v , and a current rating of 20mA to enable it drive a LED display directly. Figure 2.8 shows the pin configuration of the 7447 IC.

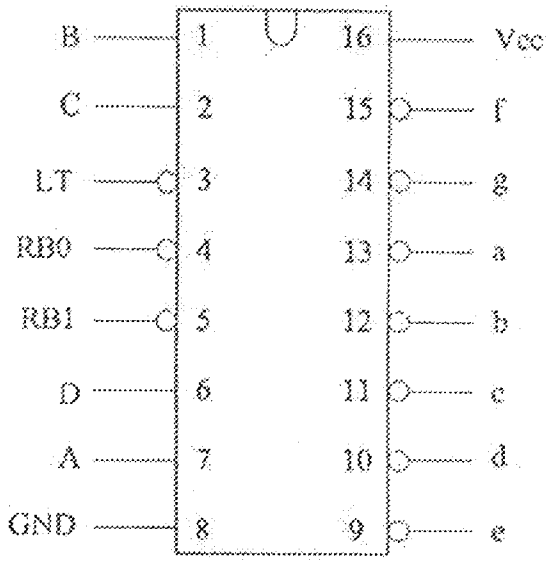


Figure 2.8, Pin Configuration of the 7447 Integrated Circuit.

The pins A, B, C, and D serve as the binary inputs, in which 'D' is the most significant bit (MSB). The pins labeled 'a' to 'g' are logic '0' or GND which are fed to a seven segment display. Pin three (3) is the 'lamp test (LT) which lights all the segments of the display when it is connected to a logic '0' or ground (GND). Pins 4 (RB0), and 5 (RB1) are used for ripple blanking output, and input respectively, and are active when connected to logic '0'.

2.3.2 The 7490 Integrated Circuit (I.C)

The 7490 I.C is a ripple through decade counter [19] with its internal gating arrangement, the 7490 can be connected to count in a number of different ways. Figure 2.9 shows the pin configuration of the 7490 I.C.

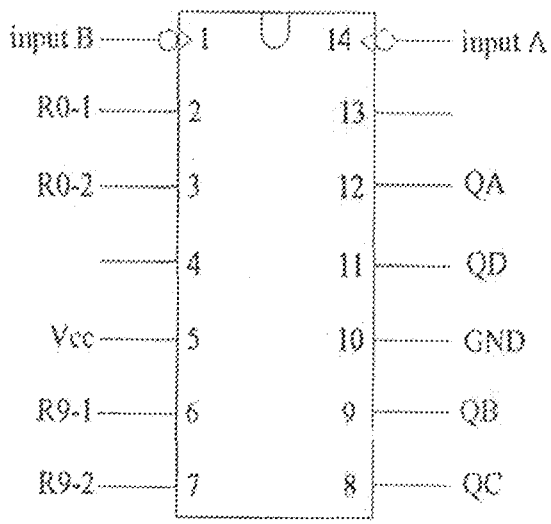
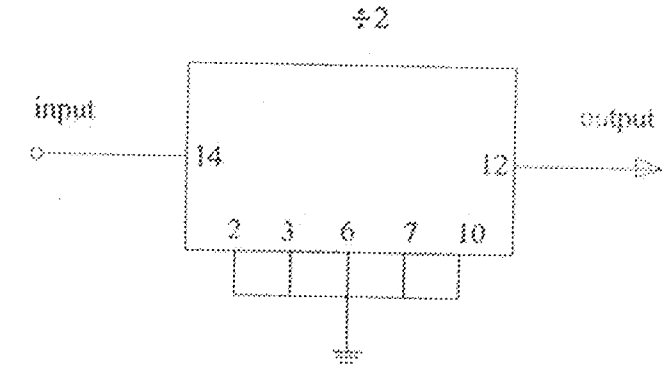


Figure 2.9 Pin Configuration of the 7490 I.C.

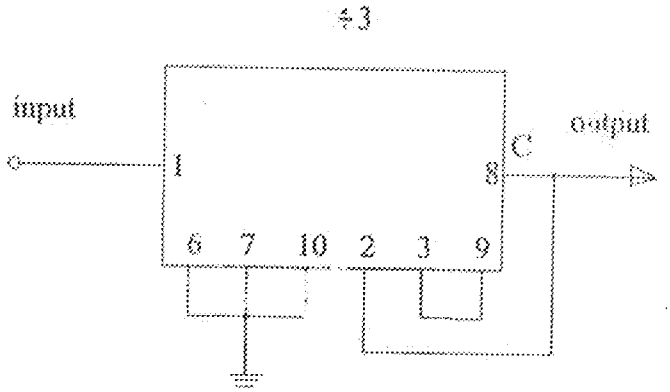
The pins 'A' and 'B' are the clock inputs, which are negative edge triggered. Pins 8,9,11, and 12 are the binary outputs; Q_C, Q_B, Q_D, Q_A respectively. The 7490 I.C has four reset leads; $R0_1$, $R0_2$, both of which when connected to the logic '1' together reset the counter to logic state '0000' for decimal '0', and leads $R9_1$, $R9_2$ of which when both connected to the logic 1 will set the counter to decimal 9 (logic '1001').

The 7490 I.C is powered with a 5v V_{CC} supply.

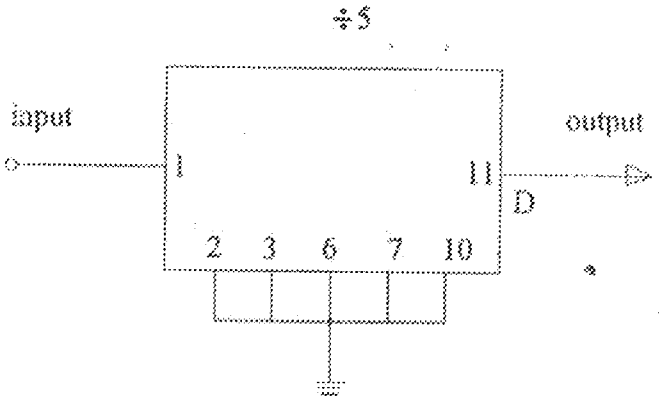
Figure 2.10 shows configurations for various divide by operations of the 7490 counter on an input signal.


÷2
input
output
14
12
2
3
6
7
10

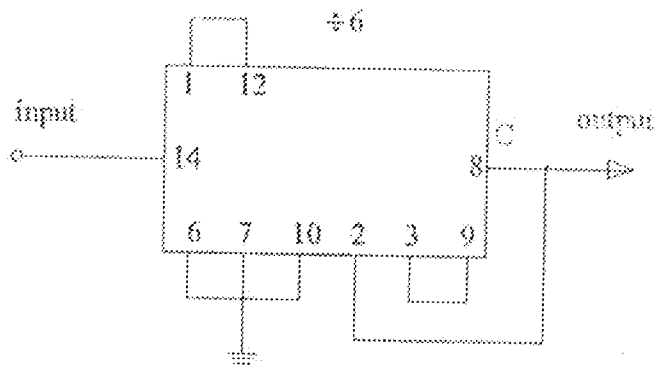
(a)


÷3
input
output
1
C
8
6
7
10
2
3
9

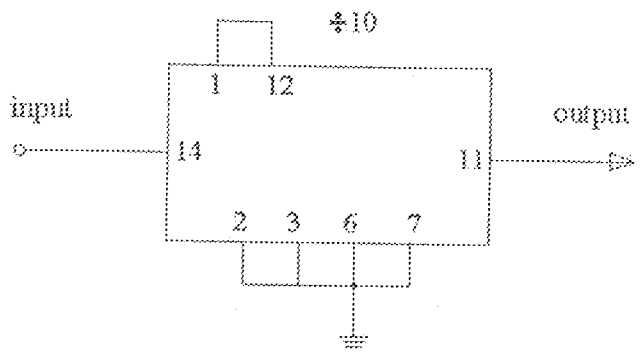
(b)


÷5
input
output
1
11
D
2
3
6
7
10

(c)



(d)



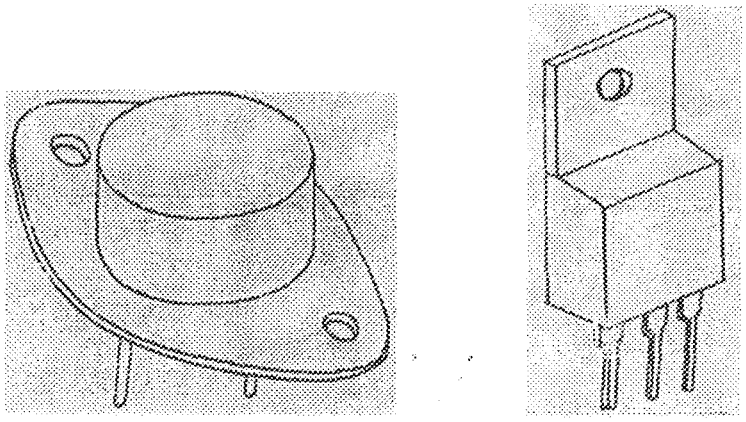
(e)

Figure 2.10 ('a' to 'e') ; Connection Configurations for various 'Divide by' Operations

2.3.3 The 7805 Integrated Circuit (I.C)

The 7805 I.C is a three pin device which belongs to a family called the 7800 (78XX) series regulator. These series produce a constant positive voltage output when a range of positive voltages are applied at its input. The 'XX' in its numbering represents the output voltage level. The 7805 is a 5 volt output device. A compliment of the 78XX series is the 7900 (79XX) series, which output a constant negative voltage when a varying negative voltage is applied at its input. The 'XX' in its

numbering also represents the negative output voltage level. The pins for the devices are labeled 'I' (input), 'G' (ground), 'O' (output). A typical 7800 or 7900 series I.C can handle a current of up to 1Ampere when mounted on a heat sink. The device is usually packaged in a TO220, 3 – pin I.C casing [20]. 3Amp and 100mA versions also exist packaged in a TO3 and TO92 casings respectively.



(a) (b)

Figure 2.11: TO-3 (a), and TO-220 (b) I.C packages for the 7800 and 7900 I.C regulators.

2.3.4 The 2N3904 Transistor :

The transistor is a universal NPN type, packaged in a TO-92 casing, used for small signal, and switching applications.

Table 2.2 describes its ratings:

Characteristic	Symbol	Ratings	Unit
Collector-Base voltage	V_{CBO}	60	V
Collector-Emitter voltage	V_{CEO}	40	V
Emitter-base voltage	V_{EBO}	6	V
Collector current	I_C	200	mA
Collector dissipation	P_C	625	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	-55~150	°C

[21] Table 2.2: 2N3904 transistor maximum ratings. (Table from AUK semiconductor)

2.3.5 The 2N3906 Transistor :

The transistor is a universal NPN type, packaged in a TO-92 casing. It is the compliment of the 2N3904 transistor. It is also used for small signal, and switching applications.

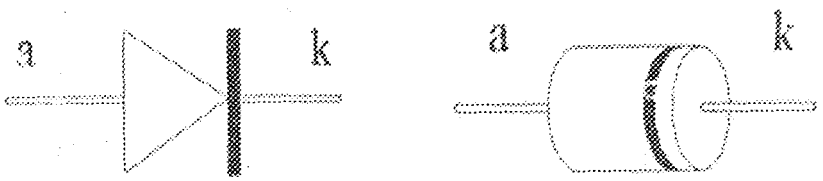
Table 2.3 describes its ratings;

Characteristic	Symbol	Ratings	Unit
Collector-Base voltage	V_{CBO}	-40	V
Collector-Emitter voltage	V_{CEO}	-40	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-200	mA
Collector dissipation	P_C	625	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	-55~150	°C

[22] Table 2.3; 2N3906 transistor maximum ratings. (Table from AUK semiconductor)

2.3.6 The 1N4001 Diode :

The device is a power rectifier type, with a voltage rating of 50v and current of 1A. It is packaged in a plastic cylindrical casing as shown in figure 2.12 (b). It allows current to flow only in one direction (anode 'a' to cathode 'k') as represented by the direction of the arrow in the circuit symbol of figure 2.12 (a).



(a) (b)

Figure 2.12; The 1N4001 Diode. Circuit symbol (a); and physical package (b).

2.3.7 The High Intensity Light Emitting Diode (LED):

The device is one which produces light at higher intensity than conventional

LEDs. It is available in red, green, and yellow.

Table 2.4 describes its characteristics.

Parameter	Red	Units
Peak Forward Current	90	mA
Average Forward Current	25	mA
DC Current	30	mA
Power Dissipation	135	mW
Reverse Voltage (IR = 100 mA)	5	V
Transient Forward Current (10 msec Pulse)	500	mA
LED Junction Temperature	110	°C
Operating Temperature Range	-55 to +100	°C
Storage Temperature Range		
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 3 seconds	

[23] Table 2.4; The High intensity LED .aximum ratings. (Table from Agilent Technologies).

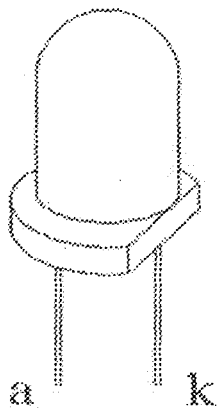


Figure 2.13: Physical representation of the High intensity LED

2.3.8 The BD140 Transistor :

[24] States; the BD136, BD138 and BD140 are silicon Epitaxial Planar PNP transistors mounted in Jedec SOT-32 plastic package (figure 2.14), designed for audio amplifiers and drivers utilizing complementary or quasi-complementary circuits. The complementary NPN types are the BD135, BD137 and BD139.

The pin configuration is as follows: pin1- Base (B), pin2 - Collector(C), pin3 - Emitter (E).

Table 2.5 describes its characteristics along with its relatives.

Symbol	Parameter	Value			Unit
		BD136	BD138	BD140	
V_{CBO}	Collector-Base Voltage (I_E = 0)	-45	-60	-80	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	-45	-60	-80	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	-5			V
I_C	Collector Current	-1.5			A
I_{CM}	Collector Peak Current	-3			A
I_B	Base Current	-0.5			A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	12.5			W
P_{tot}	Total Dissipation at $T_{amb} \leq 25$ °C	1.25			W
T_{stg}	Storage Temperature	-65 to 150			°C
T_j	Max. Operating Junction Temperature	150			°C

[25] Table 2.5: The BD136, BD138, BD140 maximum ratings. (Table from ST Microelectronics).

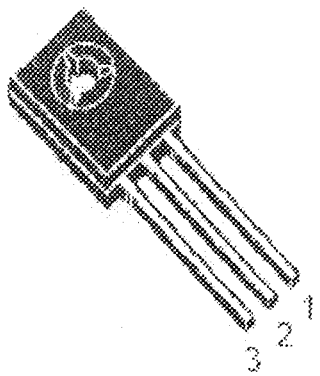


Figure 2.14: SOT-32 plastic package.

2.3.9 The 555 Timer I.C:

The 555 Timer is an 8-pin dual-in-line package (DIP) I.C. [26] States that the 555 Timer is designed to be flexible enough for a great variety of applications. As a **monostable**, its useful timing periods range from about 1 micro second (1μs) to 1 minute. It is easily connected so that the duration '**D**' or position of its output pulses

can be controlled by an input signal, and it has sufficient power-handling capability to operate an electromagnetic relay or drive a power transistor. The supply voltage (Vcc) can be anywhere in the 5-15v range.

The timer can also be configured as an **'astable'** oscillator with frequency '*f*' that produces a continuous train of high and low ('1' and '0') voltage pulses from its output.

Figures 2.13 **(a)** and **(b)** illustrate the 555 timer in monostable and astable oscillator modes respectively.

The values of **D** and *f* are given as follows;

$$D = RC \ln 3 = 1.1\,RC$$

$$f = 1 / [0.693\,(R_1 + 2R_2)C] = 1.44 / (R_1 + 2R_2)C$$

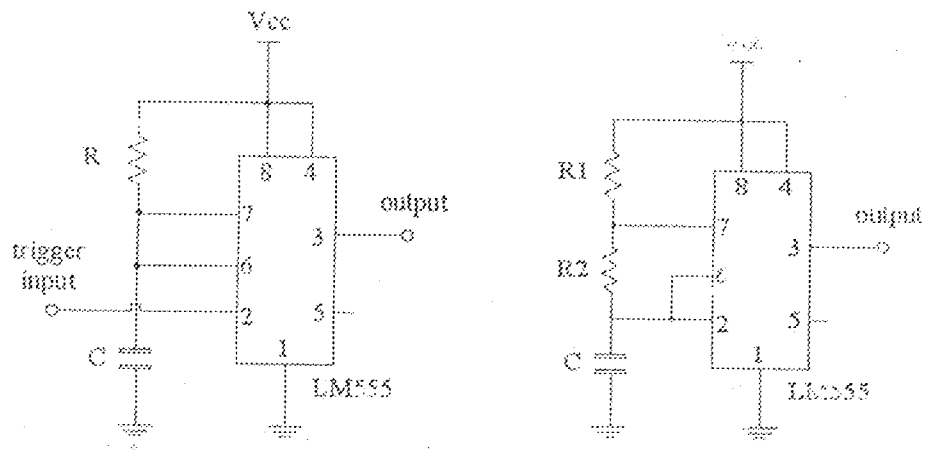


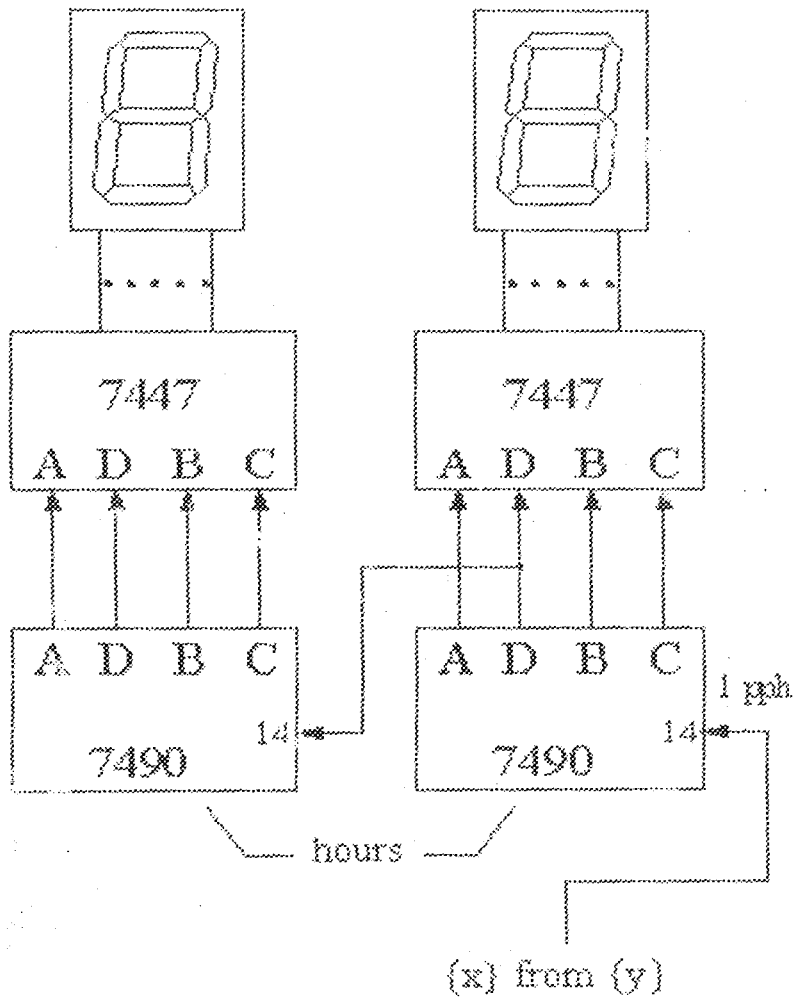
Figure 2.13: Circuit diagram of the 555 timer as a monostable (a), and an astable (b) oscillator

2.3.10 The Tone circuit :

[27] The ears of an average young person are sensitive to all sounds from about 15 Hz to 20,000 Hz (20kHz). The hearing of older persons is less acute.

particularly to the higher frequencies. The ear is most sensitive in the range from A above middle C up to A four octaves higher. Sounds in this range can be perceived hundreds of times more acutely than sounds an octave higher or two octaves lower.

2.3.11 The Block Diagrams for the design :



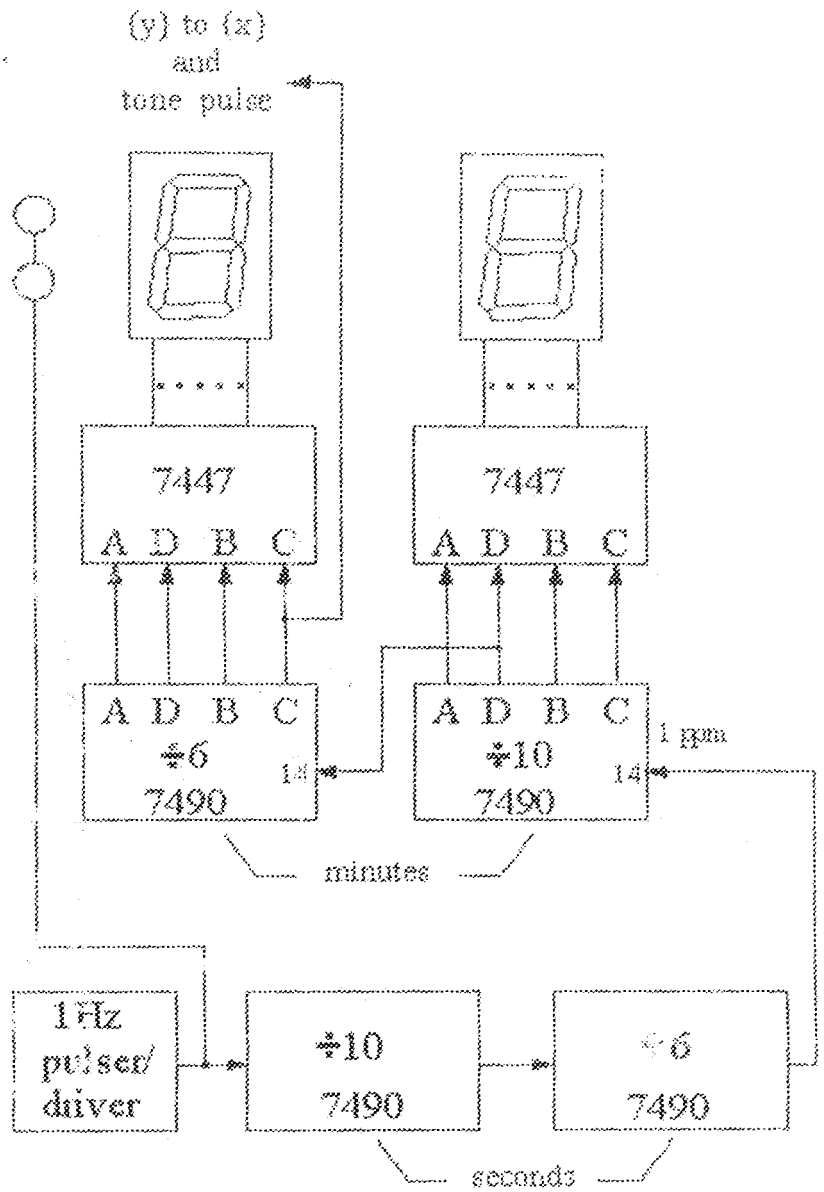


Figure 2.16: Block Diagram of the Clock Design (the block is split into two for convenience).

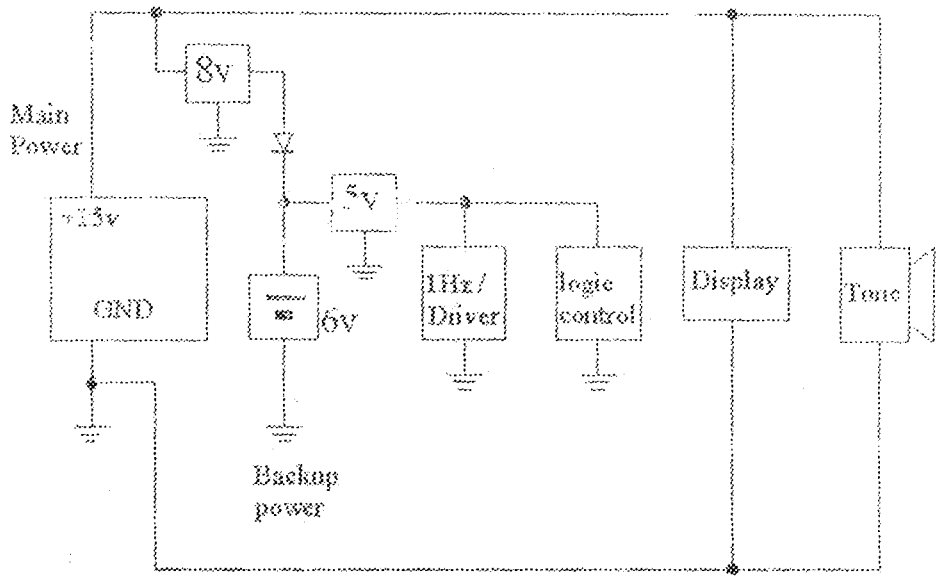


Figure 2.17; Block Diagram for powering all the Circuit Modules.

CHAPTER THREE: Design and construction

3.1 Main Power:

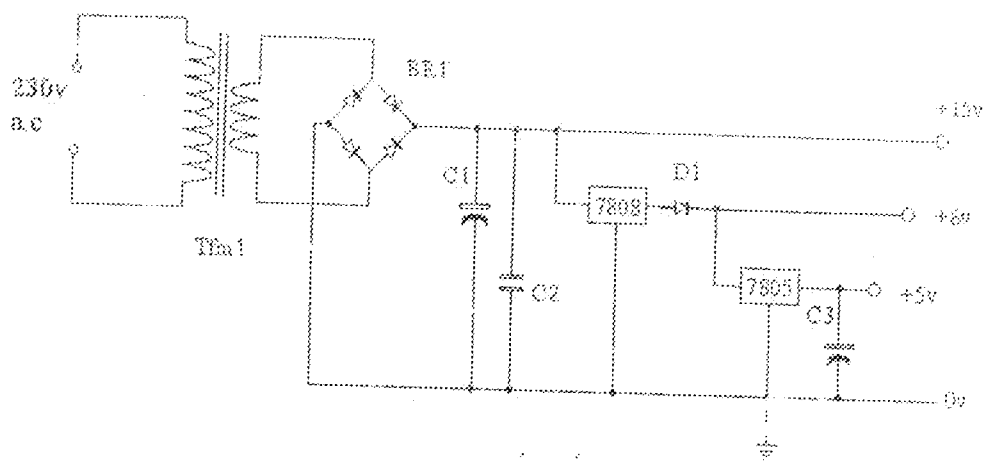


Figure 3.1; Circuit diagram for the main power

The transformer (Tfm1) is a 15v type, with current rating of 2Amp. The 15v is sufficient enough to make the 8v regulator fully functional (provided the mains supply voltage is up to 220v).

The capacitors C1 and C3 are chosen around 2000μF or higher with C1 voltage greater or equal to the transformer voltage rating (>15v). Their function is to smoothen the ripples that appear after rectification. Capacitor C2 (0.01μF) helps to remove spikes that may occur in the power supply.

The bridge rectifier (BR1) used must have a current rating greater or equal to that of the transformer.

Diode D1 (1N5401) serves as a path to charge the backup battery, and a power supply path to the 5v regulator. It prevents the cell current from flowing back to the 8v line in the event of a mains power outage. Any 2Amp (or greater) rated rectifier diode could be used.

3.2 The Backup Power:

The backup as shown in figure 3.1 is made up of a 6v, 4Ah rechargeable cell that delivers power only to the clock circuitry in the event of a power outage. Powering the clock circuitry makes it possible to keep the clock running for long periods when the main power is offline, which reduces the need to set the clock again when the main power resumes. Usually the cell charges from the 8v line when it is weak, and stops drawing current when it is full.

3.3 The 1Hz counter:

This part of the circuit could be salvaged from a conventional wall clock, or any other clock circuit that produces accurate 1Hz pulses. The reason for using such a circuit is because it is made with a quartz crystal which ensures its high degree of accuracy in delivering 1Hz pulses.

Using a 555 IC timer circuit to achieve very accurate 1Hz pulses is nearly impossible because the ideal component values that would determine the timing are not available, for example, there is the restriction of using only resistors from table of preferred values if one was to use fixed resistors. If choice is made to use variable resistors for timing the 555 IC, it is very difficult to set it to precise value that may require up to six or more decimal places away. Even if the right timing were to be achieved with the 555 timer for 1Hz pulses, over time and the influence of external temperature can vary the component conditions and slightly alter their values, which will adversely affect timing.

Consider the following effect;

If the 1Hz pulse circuit should delay by 0.001 seconds (1ms), in 1 hour (3600seconds), it will delay by 3600 x 0.001 = 3.6 seconds.

In 24 hours (1day), it will delay by 3.6 x 24 = 86.4 seconds (1min, 26.4sec).

In a week (7days), it will delay by 86.4 x 7 = 604.8 seconds (10min, 4.8sec).

Such a time variation is too costly in choosing a 555 timer to produce the 1Hz pulses.

3.3.1 Determining the 1Hz quartz pulser terminals:

The 1Hz quartz pulser from a conventional wall clock can easily be identified because it is the only circuit directly connected to the battery supply, and hence its power terminals could easily be deduced. It uses a 1.5v cell, so a suitable voltage divider was chosen to provide such power to the pulser as shown in figure 3.2.

The clock pulser provides 180° out of phase from two separate terminals (0.5Hz each) to an induction coil which magnetizes a circular permanent magnet to produce rotation every second. The terminals leading to this coil serve as the outputs (1 and 2). The outputs are fed to the driver circuit to be amplified and combined to give a single 1Hz from both.

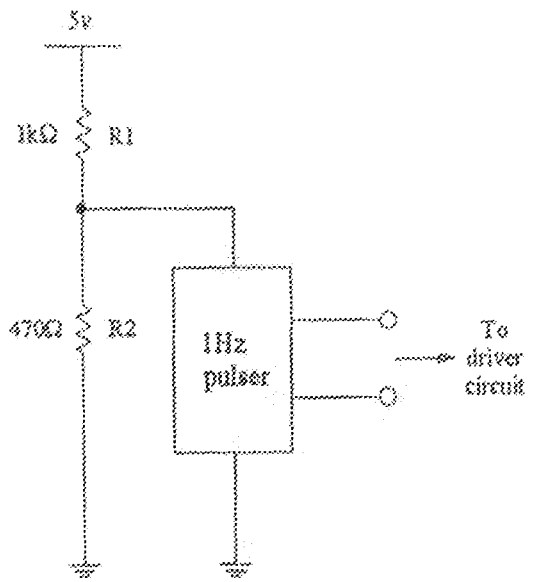


Figure 3.2: Voltage divider to power 1Hz pulser.

The voltage supplied to the pulser unit is the same as the one across the R2, given by;

$$V_{R2} = Vcc\ [\ R2 / (R1+R2)\ ].$$

Where Vcc = 5v.

» $V_{R2} = 5 [470 \div (1000 + 470)]$

» $V_{R2} = 5 [470 \div (1470)] = 1.6v$

3.4 The Clock Driver circuit:

This circuit amplifies the pulse signals from the quartz pulser and combines them to produce Hz from a single output. All the transistors (Q1, Q2, and Q3) are operating as switches (cutoff and saturation). Transistors Q1 and Q2 amplify the pulse from their respective terminals. They conduct one at a time within the space of 2 seconds that is each is 0.5Hz in 1 second (1Hz in 2sec). Since they are 180° out of phase, while one is conducting in its own phase, before its next phase two seconds away, the other will conduct and the process continues, giving a steady stream of 1Hz pulses when combined. Figure 3.3 is shown below to further describe the process.

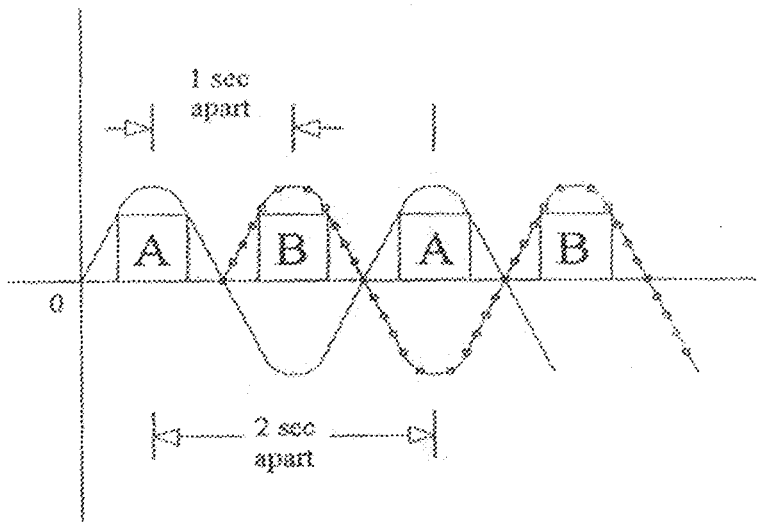


Figure 3.3; Waveform for output of 1Hz pulser.

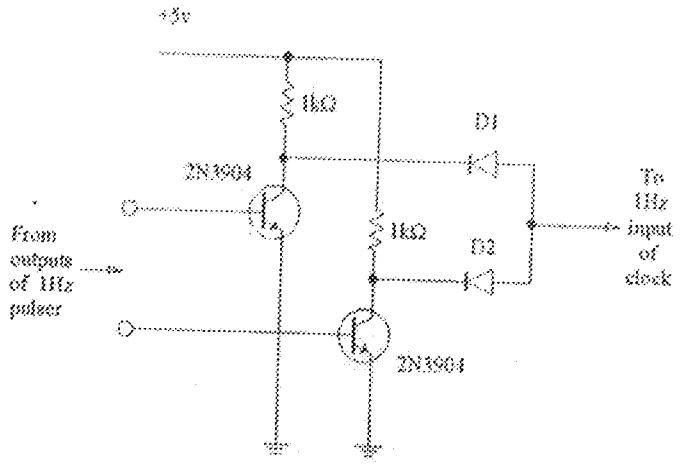


Figure 3.4; Pulse driver circuit.

The diodes D1 and D2 (of values 1N4001) serve as a drain path negative edge triggered 7490 decade counter clock input.

Transistors Q1 and Q2 could be 2N3904, or any other transistor with similar characteristics, since they are operating only as switches.

Transistor Q3 could be a 2N3906 for small load indicator applications, or a BD136 / BD140 (1Amp) for lager load indicator as in the case of the external display board for the circuit.

3.5 The Divide by six (÷6) counter:

The divide by six counter made from the 7490 IC is connected as shown in figure 2.10(d). The configuration is a combination of a '÷2' and a '÷3' counter to achieve the '÷6'. For every six input pulses at pin 14 of the 7490 IC, there is a corresponding pulse output at pin 8. By returning pins 8 and 9 to pins 2 and 3 respectively, the counter is reset to zero after completing its cycle.

3.6 The Divide by ten (÷10) counter:

The divide by ten counter is also made from the 7490 IC connected as shown in figure 2.10(e). The configuration is a combination of a '÷2' and a '÷5' counter to achieve the '÷10'. For every ten input pulses at pin 14 of the 7490 IC, there is a corresponding pulse output at pin 11. Pin 12 is the output for the '÷2', while pin 1 is the input for the '÷5'.

3.7 The Clock Hour circuit:

The circuit comprises of two 7490 BCD / decade counters connected in a '÷24' configuration as shown in the circuit diagram of figure 3.5.

The 7490 IC counts from 0 to any configured modulus, therefore in the 24hr clock format (modulus 24, count 0 to 23), it counts from time 00:00 (zeroth hour) to 23:59.

An arrangement for a 12hr format can be made, but this requires gating the clock with additional components to start its hour count from digit 12' rather than 00', and continue in the order 01', 02', 03', etc, which means more power consumption, use of more components, and hence more cost. Also in the 12hr format, the display panel usually is required to display the 'AM' and 'PM' time range, which also results to use of more LEDs to convey that message on the display, leading again to use of more components, power supply, and hence more cost.

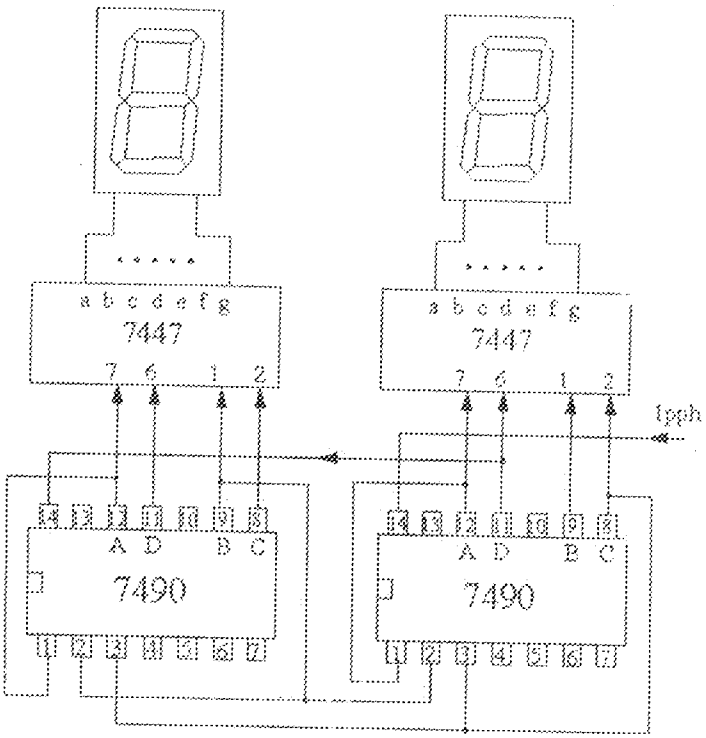


Figure 3.5; Circuit diagram for the clock circuit.

3.8 The Time setting panel circuit:

The time setting is achieved by configuring a 555 timer IC to oscillate at two independent frequencies for fast and slow setting to set the hours and minutes respectively. The timer is used to pulse the 1st divide by IC in the clock circuit ('units' of second), in order to speed up its clocking. The circuit for the setting panel is shown in figure 3.6 below.

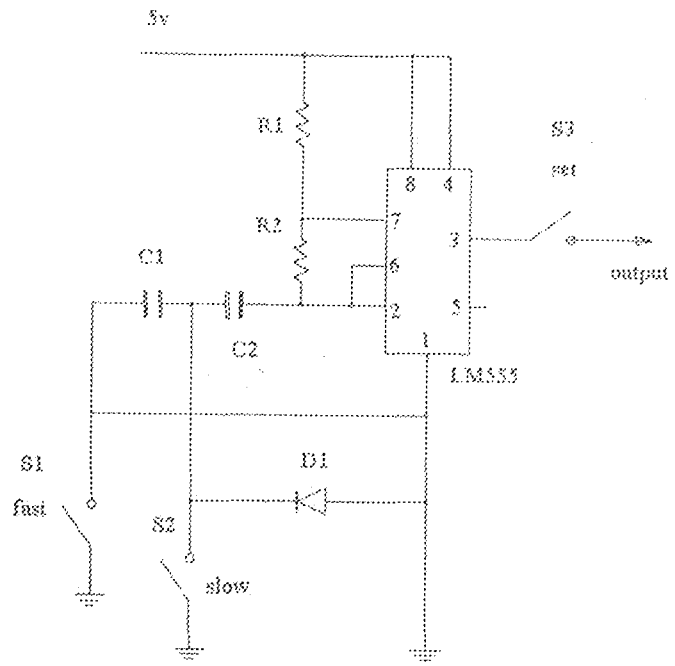


Figure 3.6: The time setting panel circuit

The 'set' button has to be pressed simultaneously with the 'fast' or 'slow' button in order to achieve an increase in count. Closing S1 causes C1 and C2 to be in series (forming the timing capacitance for the oscillator), also completing the path for grounding pin 1 of the 555 IC, while closing S2 causes only C2 to be used as the timing capacitance for the oscillator. D1 forms the return path for the 555 IC when S2 is pressed. Note that omitting D1 leads to a loss of return path when S2 is pressed, and placing a bridge in place of D1 renders C1 useless.

The circuit elements were chosen as follows;

$C1 = 0.1\mu F$ $C2 = 1\mu F$

$R1 = 1k\Omega$ $R2 = 10k\Omega$

The frequency for fast setting (f_1) is given by;

$$f_1 = 1.44 / \{ (R_1 + 2R_2)C_f \} .$$

But the capacitance C_f is the magnitude of C_1 and C_2. Since they are in series, total

capacitance (C_f) = ($C_1 \times C_2$) / ($C_1 + C_2$) Farad.

$C_f = (0.1 \times 10^{-6} \times 1 \times 10^{-6}) / (0.1 + 1) \times 10^{-6} = 0.09\mu F$. So,

$f_1 = 1.44 / (21 \times 10^3 \times 0.09 \times 10^{-6}) = 762Hz$.

The frequency for slow setting (f_2) is given by;

$f_2 = 1.44 / \{(R_1 + 2R_2)C_2\}$

$= 1.44 / (21 \times 10^3 \times 1 \times 10^{-6}) = 69Hz$

3.9 The Tone circuit:

The tone circuit is made up of a 555timer oscillator, oscillating at a frequency chosen between 2-5 KHz (which is the range most easily perceived by the human ear). The tone circuit monitors all the logic outputs of the clock circuit IC (7490s) with the exception of the hour ICs, and the MSBs for the divide by six counters. When all the logic states of the ICs are at '0', (14 pins altogether), the 14-input NOR gate (achieved by DTL configuration) switches on the tone circuit for a period of 1 second. The tone circuit is shown in figure 3.7 below.

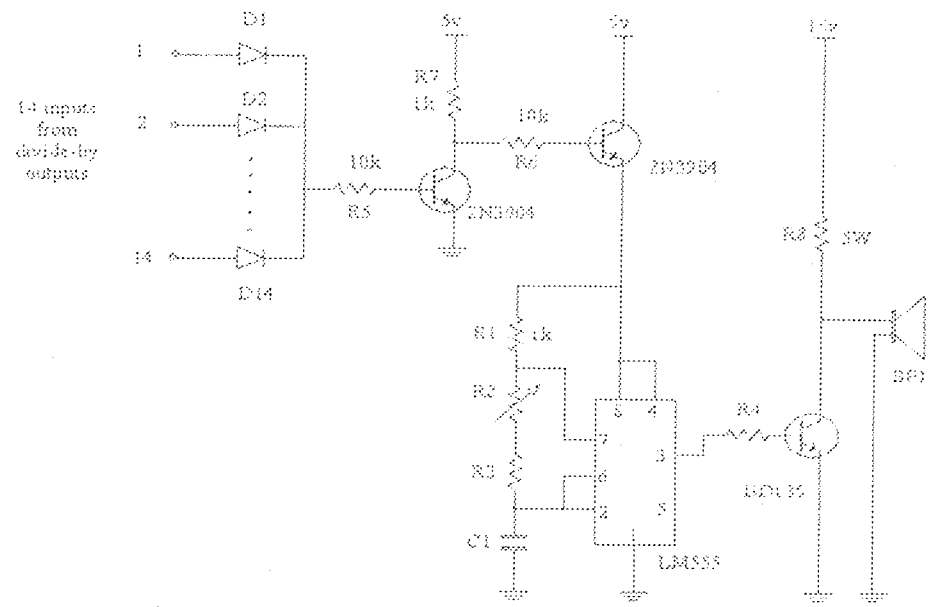


Figure 3.7: Circuit diagram for tone circuit.

The circuit elements were chosen to give a tone frequency near 3kHz according to the values stated below;

$R1 = 1k\Omega$, $(R2 + R3) = 23k\Omega$, $C1 = 0.01\mu F$

From the established formula,

Tone frequency (f) = $1.44 / (1 + 54) \times 10^3 \times 0.01 \times 10^{-3} = 3.07$ kHz

To find the resistance of the base resistor (R4) for the BD135 power transistor, and noting that a piezo speaker is used for output, consider the following;

The load resistor (R8) power rating (P) is 5W.

The supply voltage at the output stage (V) = 15v

The voltage across the collector-emitter channel of the transistor (V_{CE}) = 0.7v (for a silicon transistor).

The voltage across the load resistor (V_R) = $V - V_{CE} = 15 - 0.7 = 14.3$v

Current through the load resistor (I_C) = $P / V = 5 / 14.3 = 350$mA,

but (I_C) = $b\, I_B$, where: b = gain of an NPN transistor (also h_{FE}), which is 230 for the BD135 transistor in question, and I_B is the base current to the transistor. Therefore,

$I_B = I_C / 230 = (350 \times 10^{-3}) / 230 = 1.52$mA

Base resistance (R4) = V_{BE} / I_B, where: V_{BE} is the base-emitter voltage supplied by the 555 timer IC, and is 3.4v (max), therefore,

R4 = $3.4 / (1.52 \times 10^{-3}) = 2.24k\Omega$, approximately $2.2k\Omega$ (chosen from table of preferred values for resistors.

3.10 The 7-Segment LED Grid Display:

The grid display panel is made up of four 7-segments, two of which display the hours and the other two which display the minutes. Each segment on the display is made up of 38 LEDs (D1 to D38), therefore in a four 7-segment board, there are 38 x 7 x 4 LEDs (1064 LEDs) excluding the 'seconds' pulse LED array. Each segment is driven by one PNP transistor (BD140), 38 transistors in all excluding the 'seconds' display array. The LEDs are physically arranged on a 'Vero-board' to give the shape of a conventional 7-segment display. Figure 3.8 below shows the circuit diagram for each segment.

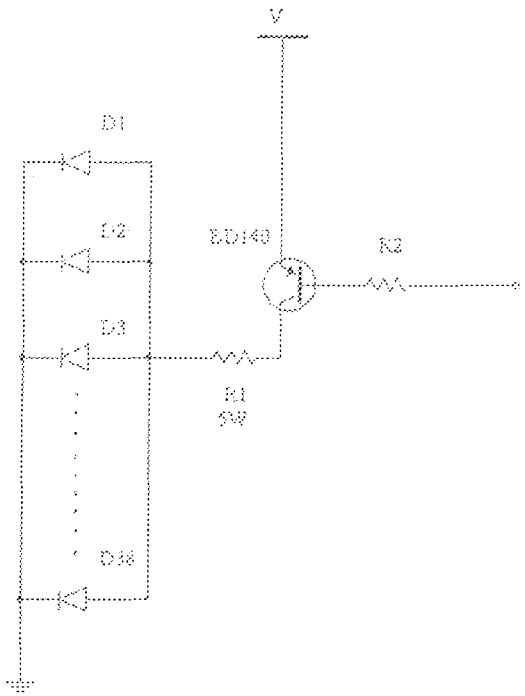


Figure 3.8; Circuit diagram for one segment in the display board

Note that each segment on the board is controlled by the corresponding output from any of the 7447 decoder ICs. When the decoder IC outputs a positive pulse ('1') to the base of the driver transistor (BD140), the transistor switches off because it is a PNP

type, thereby opening its collector-emitter channel and switching its corresponding display segment off. On the other hand if a negative pulse ('0') is applied to its base by the decoder IC, the transistor switches off its corresponding segment.

The resistor R2 (10kΩ) is to limit the base current to the driver transistor.

The 7447 decoder IC sinks the current from the BD140 emitter-base channel, by convention, a negative base-emitter voltage ($-V_{BE}$) flows through the base-emitter channel. From data sheets, the emitter-base cutoff current (I_{EBO}) is 10μA (at base-emitter voltage V_{BE} of 5v). The minimum value of base resistance (R_B) that will cut-off the collector-emitter channel is given by;

$$R_B = V_{BE} / I_{EBO} = 5 / (10 \times 10^{-6}) = 500k\Omega$$

Any resistor lower than the above with a Vcc of 5v will cause the transistor to start conducting, hence a 10kΩ resistor was chosen which sufficiently causes conduction in the collector-emitter channel of the BD140 transistor.

The limiting resistor R1 is calculated as follows;

From the datasheet of the high intensity LED, each forward bias voltage (V_f) = 2v, at a forward current (I_f) of 20mA.

There are 38 LEDs per segment, therefore total forward current (I_{TF}) is given by; $I_{TF} = I_f \times 38 = 20 \times 10^{-3} \times 38 = 760mA$.

The voltage across the resistor (V_R) = ($V - V_f$) = 15 – 2 = 13v

Supply voltage (V) = 15v

The value of the limiting resistance (R1) is given by;

$$R1 = (V_R / I_{TF}) = (13 / 760 \times 10^{-3}) = 17\Omega$$

Such a resistor caused the BD140 transistor to heat up excessively, therefore a 330Ω resistor value was chosen, which allowed the transistor to operate at a safe heat.

The display is meant to be on for very long periods, and so the LED array

limiting resistor (R1) heats up to a great extent, especially the hour's segments, therefore a higher watt resistor (5W choke) was used. A parallel combination of lower watt resistors could be made, of course considering the total resistance when paralleled.

CHAPTER FOUR: Tests and Results

4.1 Power Supply:

The power supply was tested after construction at its respective voltage regulator outputs, and was found to be as shown in Table 4.1 below.

Regulator	Output (v)
5v	5.1
8v	7.9
Bridge rect. (unregulated)	13.6

Table 4.1: Power Supply output voltage results.

The 13.6v output is the result of the rectifier diodes. At any instance during regulation, only two out of the four diodes conduct, and the voltage drop across each is 0.7v, therefore their sum is 1.4v. Subtracting their voltage drops from the 15v volts power supply gives the resulting 13.6v, that is;

15v – 1.4v = 13.6v

4.2 The 1Hz pulser voltage supply:

The 1Hz pulser was connected according to Figure 3.1 (Chapter Three), and after measuring the voltage across R2, it was found to be 1.6v, which is sufficient enough to power the 1Hz pulser connected in parallel to the resistor.

4.3 The Time Setting Panel:

Based on the component values chosen for the timing of the 555 timer IC, and by closing S1 (fast setting), it was found that the IC oscillated at a period (T) of 98μs after measuring with an oscilloscope, hence the frequency (f) was deduced as;

$$f = 1 / T \quad \Rightarrow \quad 1 / (96 \times 10^{-6}) = 10.42 \text{ kHz}$$

After closing S2 (slow setting) and measuring with an oscilloscope, it was found that the 555 IC oscillated with a period (T) of 18ms, hence the frequency (f) was determined as:

$$f = 1 / T \quad \Rightarrow \quad 1 / (18 \times 10^{-3}) = 55.55 \text{ Hz}$$

The signal traces for both conditions are shown in Plates 4.1 and 4.2 respectively.

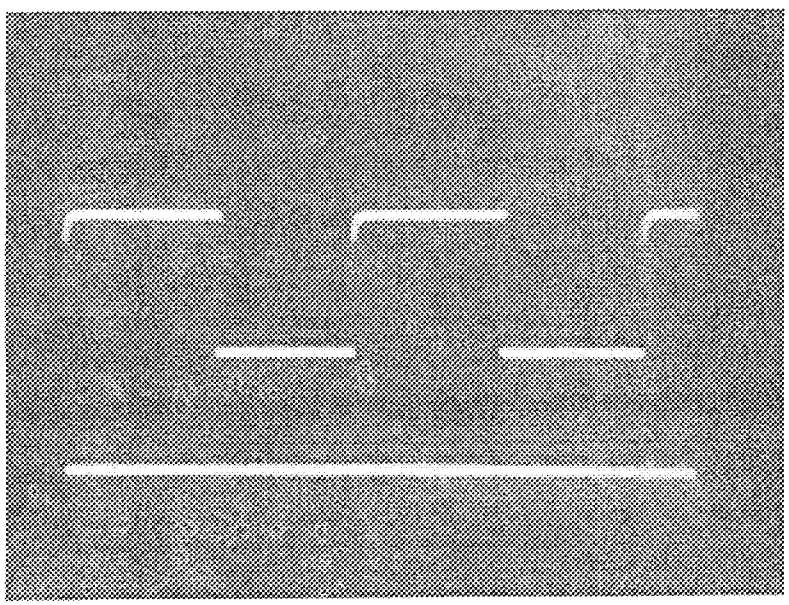


Plate 4.1; Signal trace for fast time setting, O-scope set at 20μs/div[time], 2v/div[voltage].

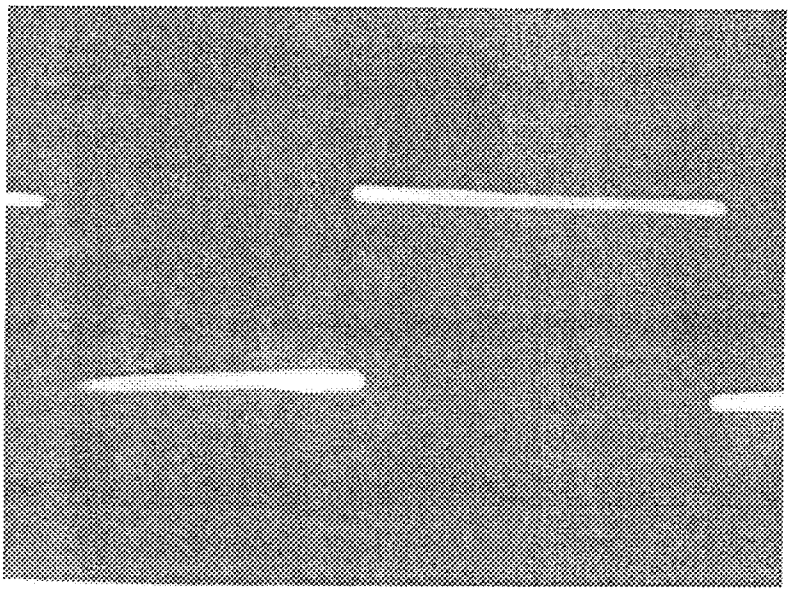


Plate 4.2; Signal trace for slow time setting, O-scope set at 2ms/div[time], 2v/div[voltage].

4.4 The Display Board:

4.4.1 Expected conditions:

The standard power rating of a high intensity red LED according to the data in Table 2.4 (Chapter Two) is 135mW. There are 38 LEDs per segment. It is expected that the power consumed by each segment (P_{seg})is;

P_{seg} = Power for one LED x 38 $\Rightarrow$ $135 \times 10^{-3} \times 38 = 5.13W$

The expected power consumed by each 7-segment ($P_{7\text{-}seg}$) is given by;

$P_{7\text{-}seg} = P_{seg} \times 7 \Rightarrow 5.13W \times 7 = 35.9W$

The expected maximum power consumed by the board (P_{Total}) at maximum number of segments 'on' (time 08:08, 26 segments will be on), neglecting the seconds is given by;

$P_{Total} = P_{seg} \times$ number of on segments

$= 35.9W \times 26 = 933.4W$

4.4.2 Actual conditions:

After measuring with a digital multimeter connected appropriately, it was found that each segment draws only 60mA at 1.7v

The current also drawn by the display during the maximum 'on' segments (time 08:08) was found to be 740mA, and a voltage of 1.6v.

The current drawn by the display during the minimum 'on' segments (time 11:11) was found to be 430mA, and a voltage of 1.6v.

The 'off' state of a segment had a voltage of 0.22v across it, which is satisfactorily low not to light the segment.

The difference of the actual from the expected is very likely due to the manufacture type of the LEDs which deviate from standard high intensity type. This could be seen from the display that even when powered with sufficient current and voltage, it does not appear to be very bright especially during the day.

4.5 The Tone Circuit:

The output signal of the tone circuit was measured with an oscilloscope and found to cover a period (T) of 0.32ms, hence the frequency (f) was deduced by formula:

$$f = 1 / T \quad \Rightarrow \quad 1 / (0.32 \times 10^{-3}) = 3.1 \text{ kHz}$$

which is a similar value to the calculated value (3.07 kHz). This shows that the established formula for setting the 555 timer astable oscillating frequency holds true.

A photographic plate of the signal trace on the oscilloscope is shown in Plate 4.3 below.

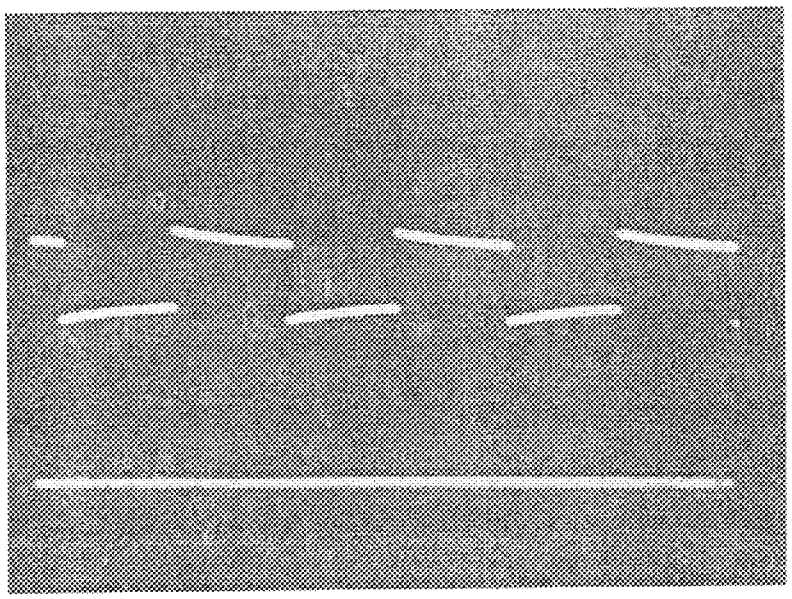


Plate 4.3; Signal trace for tone, O-scope set at 0.1ms/div[time], 2v/div[voltage]

4.6 Limitations:

The main limitation of the project is the fairly low illumination of the display board which is caused by the LED type. Difficulty was encountered in obtaining the highest intensity type, as they were not available.

Another limitation is that the unit does not display the time when power from the a.c mains supply is cutoff.

CHAPTER FIVE: Conclusion

5.1 Recommendation:

The following are recommended for building a more advanced unit;

i A good addition that could be made to the unit is a more complex tone circuit which would not just produce an hourly tone, but also produce a number of tones corresponding to that hour.

ii The unit could also be interfaced with another display (slave display) for the public located at a different direction who cannot see the main display.

5.2 Summary:

The aim of the project was achieved, but absolute satisfaction would have been reached if not for the limitations presented in Chapter Four.

Some of the problems encountered could be solved in the case of future building of this project, such as:

i The low daytime illumination of the display could be improved by using the standard high intensity LED type. Difficulty in obtaining such LEDs was encountered. Due to the limited availability of such components, importation may be necessary.

ii The use of a higher current rated power transformer would ease heating to it, and also decrease its load burden.

iii A higher Ampere-hour (Ah) cell(s) combination could be connected to sustain the display, during the event of an a.c mains power supply failure (from

P.H.C.N).

It is hoped that in time to come a more reliable and power efficient unit would be built, with a bigger and brighter display as well as a louder hourly tone to serve a larger community.

References :

[1] McGraw-Hill. *Encyclopedia of Science and Technology.* McGraw-Hill, 1982, Vol. 13, p.32

[2] Grolier Inc., *Family Encyclopedia.* U.S.A. Vol. 18, p.25. ISBN 0-7172-5364 -3

[3] Grolier Inc., *the Encyclopedia of Americana*, International Edition, Connecticut, U.S.A., Vol. 14, p.458. ISBN 0-7172-0120-1 (V.1)

[4] World Book Inc., *The World Book Encyclopedia* , World Book Inc., Chicago , U.S.A., 2004, Vol. 9, p.379. ISBN 0-7166-0104 – 4

[5] Microsoft ® Encarta ® 2008. © 1993-2007 Microsoft Corporation. All rights reserved. , search = clocks and watches / atomic clock.

[6] Microsoft ® Encarta ® 2008. © 1993-2007 Microsoft Corporation. All rights reserved. , search = clock / mechanism / inside a mechanical clock.

[7] Grolier Inc., *the Encyclopedia of Americana*, International Edition, Connecticut, U.S.A., Vol. 3, p.733. ISBN 0-7172-0120-1 (V.1)

[8] www.destination360.com/europe/uk/big-ben.php. May 2009

[9] www.wikipedia.org/wiki/kanazawa-station/digitalclocks. May 2009

[10] J.R. Nowiki, L.J. Adam, *Digital Circuits*, Chapman and Hall Inc., New York, U.S.A., 1990, p.301. ISBN 0-7131-3641-3

[11, 12] I. Zherebstov, *Basic Electronics*, Mir Publishers, Moscow, USSR, 1981, p.11, ISBN 5-03-0000212-6

[13] Shuler, Electronics; *Principles and Applications*, Glencoe / McGraw-Hill, U.S.A, 1999, p.2, Fifth Edition. ISBN 0-02-804244-1

[14] Tony R. Kuphaldt, *Lessons In Electric Circuits, Volume III -Semiconductors*, Fourth Edition, December 16, 2002 http://www.ibiblio.org/obp

[15] Shuler, Electronics; *Principles and Applications*, Glencoe / McGraw-Hill, U.S.A, 1999, p.3, Fifth Edition, ISBN 0-02-804244-1

[16] www.electronics.howstuffworks.com/gadgets/clocks-watches/digital, June 2009

[17] M.S. Ahmed, Adamu M.B. Zungeru, Ambafi James G., Tola James Omokhaefe. *Department of Electrical and Computer Engineering, Federal University of Technology, Minna. Laboratory Practicals (ECE415)*, p.109, ISBN 978-5126-38-4

[18] M.S. Ahmed, Adamu M.B. Zungeru, Ambafi James G., Tola James Omokhaefe. *Department of Electrical and Computer Engineering, Federal University of Technology, Minna. Laboratory Practicals (ECE415)*, p.107, ISBN 978-5126-38-4

[19] J.R. Nowicki, L.J. Adam. *Digital Circuits*, Chapman and Hall Inc., New York, U.S.A, 1990, pp.187-190. ISBN 0-7131-3641-3.

[20] B.L Theraja, A.K Theraja. *A Textbook of Electrical Technology*. S. Chand, New Delhi, India. 2003, p.1965. ISBN 81-219-0289-4.

[21] http://www.datasheetcatalog.org/datasheet/auk/2N3904.pdf, May 2009

[22] http://www.datasheetcatalog.org/datasheet/auk/2N3906.pdf, May2009

[23] http://www.datasheetcatalog.org/datasheet2/d/0j4wyscaxa9zueg8jg9outxt7y7y.pdf, May 2009

[24, 25] http://www.datasheetcatalog.org/datasheet/SGSThomson Microelectronics /mXyzsxt.pdf, May 2009

[26] A. Bruce Carlson, David G. Gisser, *Electrical Engineering Concepts and Applications*, Addison Wesley, p373, ISBN 0-201-03940-0.

[27] Microsoft ® Encarta ® 2008. © 1993-2007 Microsoft Corporation. All rights reserved, search = loudest tone to human ear / Audiometer: sensation of tone.

APPENDIX A: Operational Manual

Powering the unit:

The unit derives its primary power from a 230v a.c mains power supply, hence, to power the unit simply plug it to a 230v a.c supply.

Setting the time:

To set the time for the unit, press the 'set' button simultaneously with either the 'fast' button for quick setting of the hour or with the 'slow' button for slower setting of minutes. To set a particular hour, it is advised to set an hour just before the required one using the fast setting, and the use the slow setting to achieve the particular hour needed with its corresponding minutes. When the unit is first switched on, it some times display numbers which are not time, it should not be worried about, just go on setting the correct time. This is as a result of the clock counter circuit skipping over its recycle state, as setting the time will initialize the unit back to normal.

Precautions to usage:

The unit must be prevented from falling or receiving any other vibrations that could lead to shock.

Liquids must not be spilled in the unit.

Any repairs should be carried out by a qualified personnel in electronics.

APPENDIX B: Trouble Shooting

The following points describe some possible solutions to likely future problems, which is strongly advised to be handled by a qualified personnel in the field of electronics. A good understanding of logic circuits by the service personnel will be of advantage.

Problem	Solution
No power to the setting panel, tone, and display.	Check components at the power section, particularly the transformer and the voltage regulator I.Cs
No power to only the display.	Check the main power supply lead to the display panel (a 15v cable).
No power to a particular segment on the main display.	Check the corresponding segment on the small setting panel and confirm if they should be both 'on'. If that on the main display is 'off ', then check the driver transistor (BD140) on that particular segment, possibly replace.
No power to a particular LED	Change the LED, it is likely burned.

The time cannot beset even when the set buttons are pressed.	Test pin 3 of the 555 timer on the setting panel with a logic probe or an oscilloscope to see if it is oscillating. If it is not, then power to the panel has been cutoff likely from the supply lead. Check connection.
No tone at the speaker.	Check the functionality of the driver transistor (BD135) for the speaker, possibly replace.
Unit does not save time when a.c mains power supply is cut off.	Backup battery is likely disconnected, or may have exhausted its useful life and needs replacement.

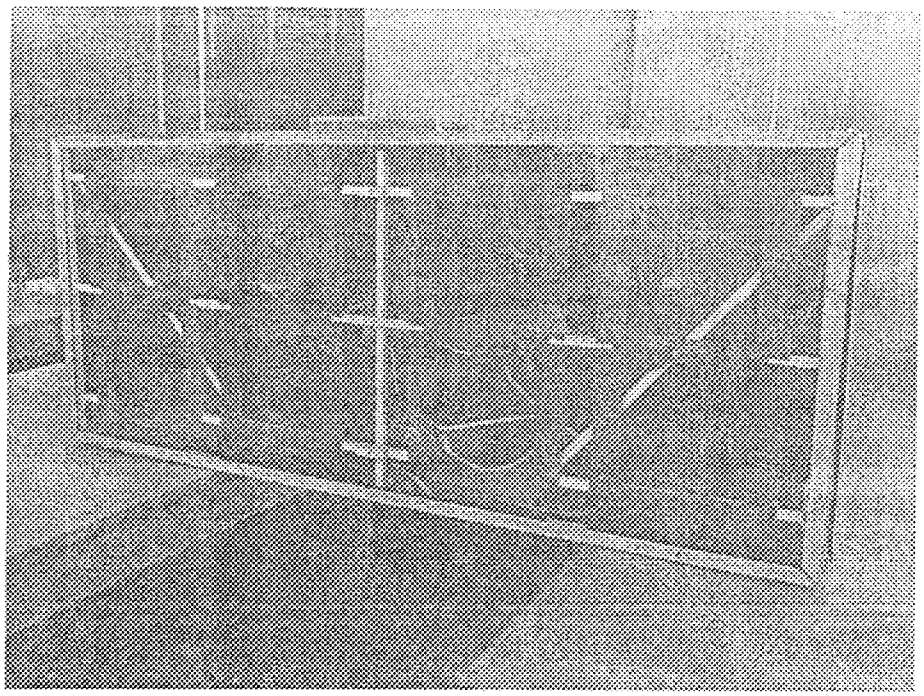
APPENDIX C: Bill of Components

Component	Price each in Naira	Quantity used	Total Cost in Naira	
74LS47	80	4	320	
74LS90	100	6	600	
BD140 (PNP)	30	29	870	
BD135 (NPN)	30	1	30	
1N4001	5	16	80	
Vero board 7"x3")	50	2	100	
Vero board 10"x4")	90	15	1350	
25v,3300μF capacitor	80	2	160	
Twin 7-segment display (1"x1")	200	2	400	
High Intensity LED (red)	6	1146	6876	
v, 4Ah Cell	500	1	500	
Bridge rectifier S4VB)	50	1	50	
30Ω, 5W esistor	20	30	600	
70Ω, 0.5W esistor	10	1	10	
kΩ, 0.5W esistor	10	7	70	
2kΩ, 0.5W esistor	10	1	10	
0kΩ, 0.5W esistor	10	5	50	
oldering lead ll(40/60 alloy)	200	1 roll	200	
805 regulator C	40	1	40	
808 regulator C	40	1	40	

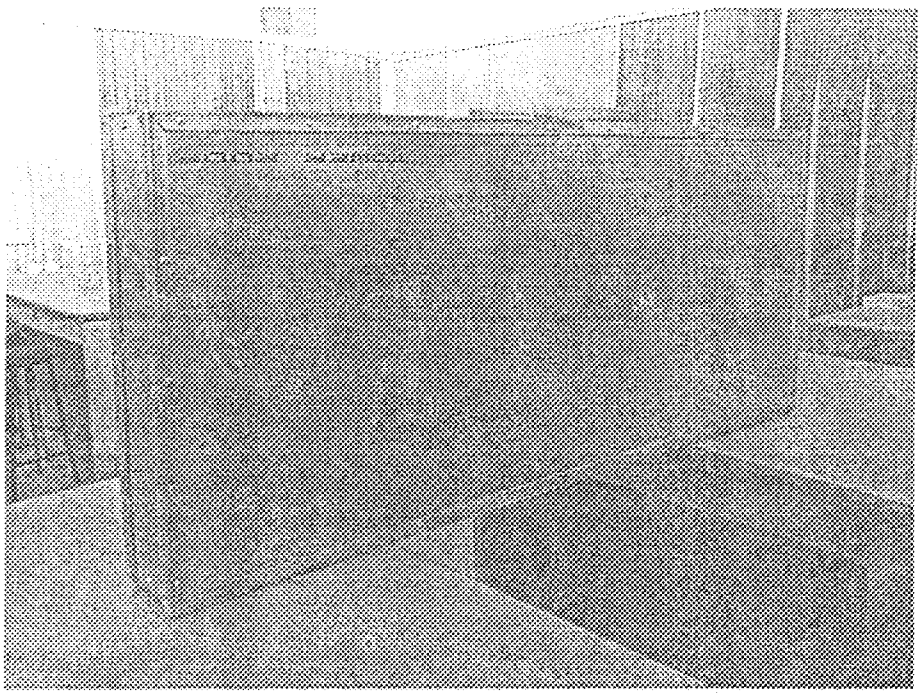
Component	Price of each in Naira	Quantity used	Total Cost in Naira	
2N3904 (NPN)	40	4	160	
1N5401 diode	40	1	40	
Button switch	20	3	60	
LAN cables	50 per yard	13	650	
15v, 2A Power transformer	450	1	450	
Large rivets	10 for 3pcs	72	240	
4mm, 2 inch bolt and nut	60 for 9pcs	31	210	
4mm, 1 inch bolt and nut	60 for 20pcs	20	60	
4mm, 1.5 inch bolt and nut	60 for 9pcs	10	60	
1 x 1 inch trunking PVC	100 per length	3	300	
Tint sticker for display	300 for 20 x 42 inch	20 x 42 inch	300	
Aluminum angle 90 iron (25 x 25)	1600 for 6m length	2 lengths	3200	
Acrylic plastic screen	3800 for 70 x 26 inches	70 x 26 inches	3800	
Aluminum Back and side sheet	2800 for 63 inches length	63 inches length	2800	
Piezo horn tweeter	400	1	400	

The Net expenditure for components is 25,086 Naira

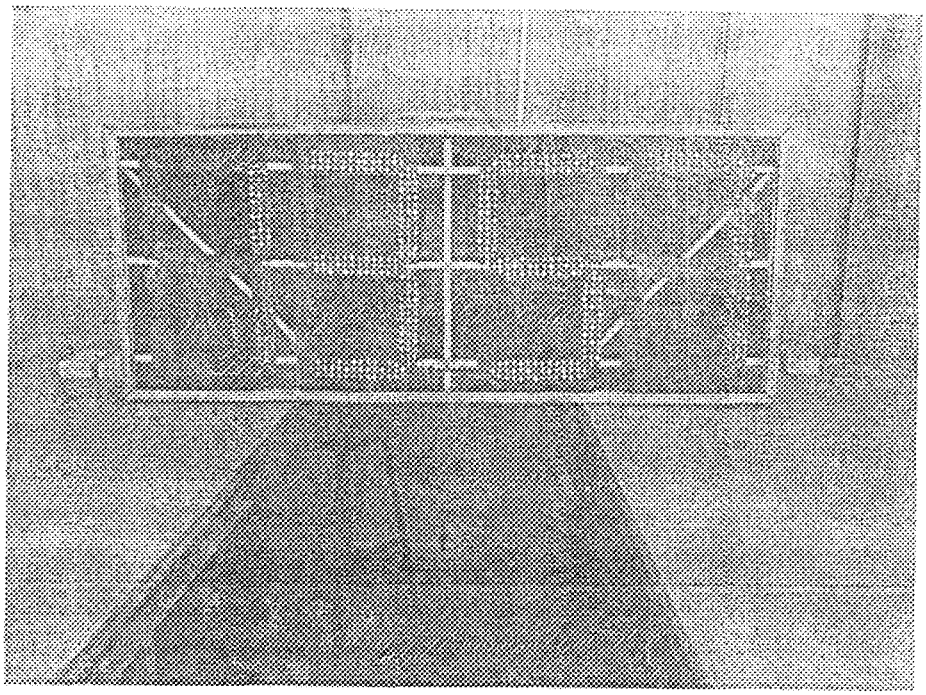
APPENDIX D: Photos



Front view of clock without tinted screen

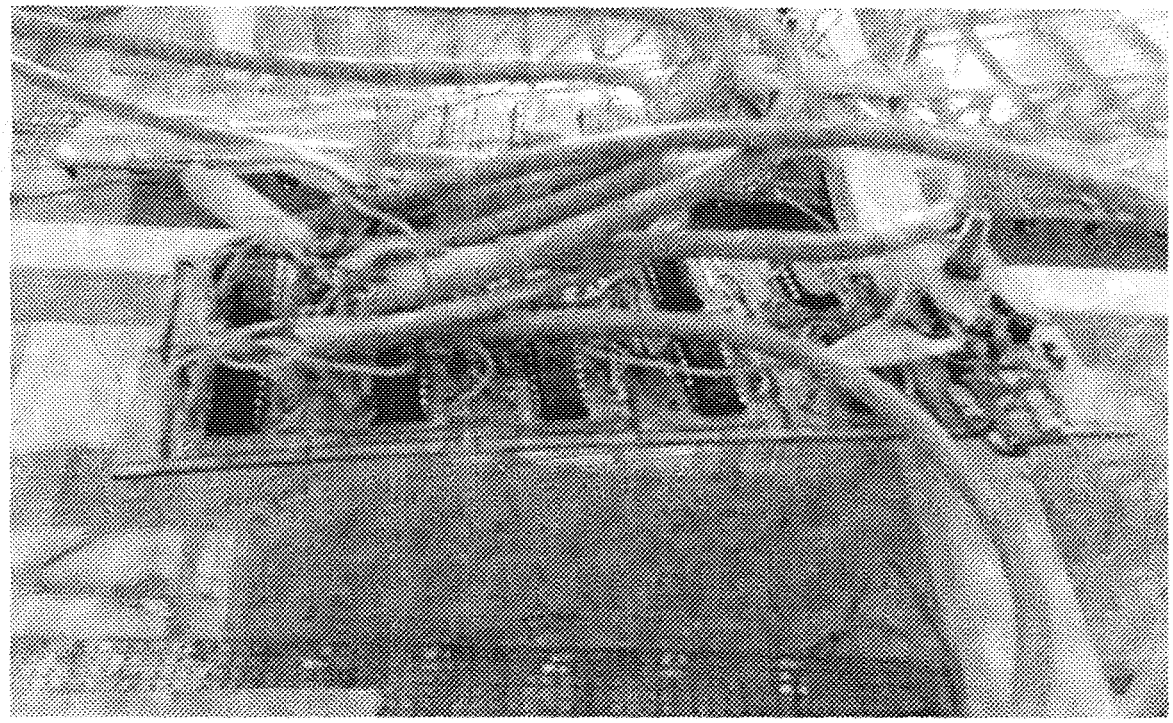


Back view of clock

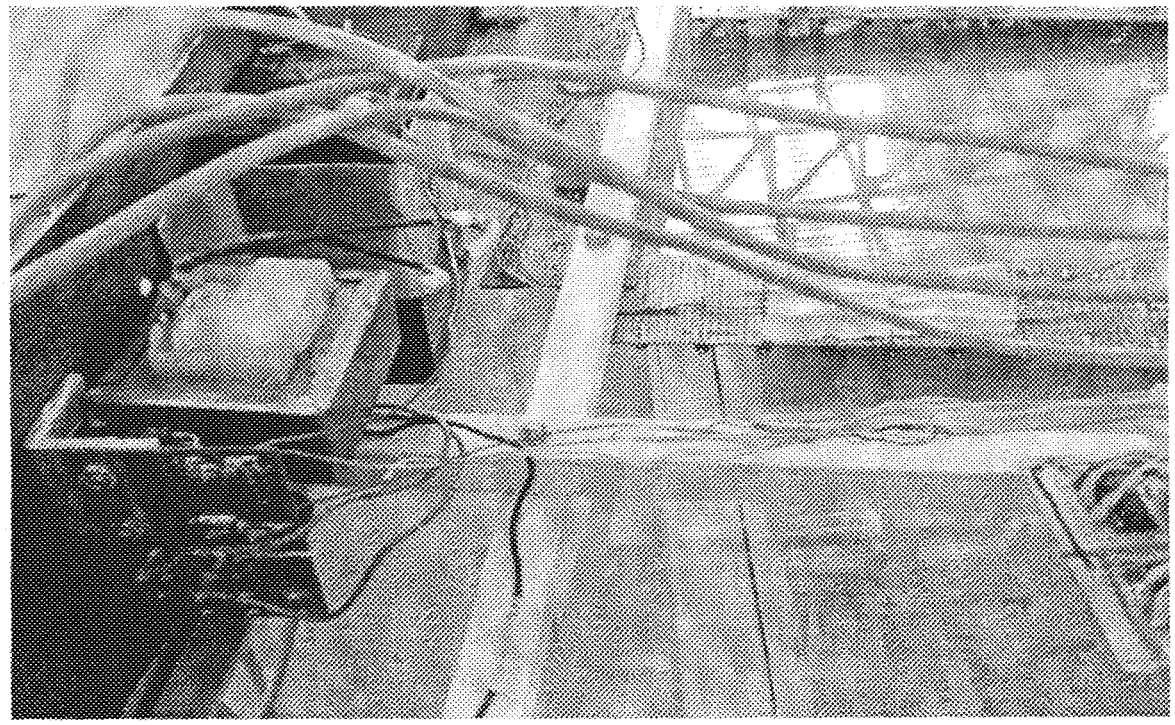


Front view at time '13:57'

Top-left aerial view



Internal circuitry, showing Logic control circuit



Power section, with back-up battery close to a.c transformer, and heat sink for regulator ICs.