DESIGN AND CONSTRUCTION OF A 4-WAY TRAFFIC LIGHTS CONTROL SYSTEM

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award of Bachelor of Engineering (B.Eng.) degree in the
Department of Electrical and Computer Engineering,
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Federal University of Technology, Minna.

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DECLARATION

l Onwuanaku Boniface Emenike declare that this project is my concept and was designed, constructed and tested under the supervision of Engr. P. O. Attah, Dept. of Electrical/Computer Engineering.

CERTIFICATION

I hereby certify that this project was carried out by Mr. Onwuanaku Boniface Emenike of the Department of Electrical/Computer Engineering, School of Engineering and Engineering Technology, Federal University of Technology, Minna.

.... 9th Dec., 2004
Engr. P. O. Attah   **Date**
(Supervisor)

....   31/07/2005
Engr. M. D. Abdullahi   **Date**
(H.O.D)

....
External Examiner   **Date**

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DEDICATION

This project is dedicated to my beloved and sweet mother Mrs. Theresa Onwuanaku who has always wanted me to have the best in life.

ACKNOWLEDGEMENT

ABSTRACT

The traffic lights control system is built around the TTL (Transistor-Transistor Logic) family-74LS145 IC (1-out-of 10 decimal decoder/driver). The circuit is designed such as to drive relay contacts, which then switches on the lamps according to the logic combinations. The circuit is pulsed by an LM555 astsble oscillator, the rate at which the lamps switches ON and OFF is determined by the value of the variable resistor, R_b. The output of the oscillator triggers the 74LS90(decade counter), which produces a ten step-binary coded decimal outputs that subsequently drives the 74LS145 IC. The output of the 74LS145 IC energizes the relays thus switching ON the lamps.

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CHAPTER ONE

1.1   INTRODUCTION

Transportation as a problem has been greatly alleviated in the last century by the advent of Motor vehicles. The alleviation of transportation by Motor vehicles has been accepted by all. Since many operations and many processes rely on a very smooth and steady transportation system. However, as advantages as it is, Motor vehicles and other means of mobility brought about the problem of traffic congestion and this in turn prompts the need for rigid traffic control.

The congestion of our roads is so serious that the problem calls for rigid road traffic regulations in order to bring order and hence safety on our roads. These traffic control systems are made up of signs, signals and marking placed on or adjacent to a street, highway or intersection as the case may be, by authority of a public body, for example, local government authority, which is within their jurisdiction to regulate, warn or guide traffic. The purpose of this control mechanism is to greatly reduce the delay on our roads on traffic users. The control mechanism facilitates safety on the roads and smooth driving.

1.2   TYPES OF TRAFFIC CONTROL SYSTEM

The very first and the simplest type of traffic control system is the use of humans known as traffic warders. This form is the commonest but with

so many disadvantages among which is the exposure of the warder to great danger. Other types of traffic control system are those that are controlled electrically. These are categorised basically into two main groups- sequential and programmed traffic control systems.

1.2.1 Sequential Logic Traffic Control System

These are the type of traffic control systems that are designed based on simple theory of combinational logic, decoders, multiplexers and counters of which this project work has adopted.

1.2.2 Programmed Traffic Control System

In this type, the control system is based on inbuilt program on the microprocessor which enables it to emulate a traffic warder.

The above form of electrically controlled systems can be combined to have what is called programmable sequential traffic control system. The control system has a sequential drive circuit and also has programs in electrically programmable-read-only-memory (EPROM)

It is very important to note here that before the advent of the above mentioned electrically controlled traffic system, semaphores had been in use which are operated manually. Semaphores are automatic fixed cycles of signals giving alternate stop and go periods of predetermined length.

1.3   ELECTRONIC TRAFFIC CONTROL SYSTEM

The project work is an electrical mechanism which controls the operations of the traffic light signals. This includes the equipment

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operating mechanism that drives the lights in the signal heads. The signal head is made up of three light bulbs arranged vertically above one another with the red on top, amber in the middle and green at the bottom. It is important that the following requirements are met by any traffic controlling device:

i.   It should provide for orderly flow of traffic and also increase the traffic handling capacity of most road intersections.

ii.   It should be capable of reducing certain types of accidents such as right-angled collisions.

iii.   It should provide for adequate flow of vehicle traffic at a moderate speed along a roadway when co-ordinated with one another.

iv.   It should provide for safe crossing of heavy traffic.

In order to ensure that the above mentioned requirements are met, some basic considerations should be employed which include:

i.   **Design:** The design of traffic control signals should be such that features like size, shape, colour etc are combined in a way that the attention of the road users will be drawn to it.

ii.   **Placement:** The placement of traffic control systems should be such that it will command the attention of road users. Also, the device should be located so as to give adequate time for a driver to make proper response if he/she is driving at a normal speed.

iii.   **Maintenance:** The device used as traffic control should be maintained properly as this will make it look official and enforcing, thus commanding compliance from its users.

iv.   **Uniformity:** It is expected that a traffic control system signals should have the same meaning as illustrated in the next section.

1.4   THE TRAFFIC CONTROL COLOUR CODE

The conventional colour code employed in traffic controlling are red, amber and green. The red light indicates stop, hence, it prohibits entry into any intersection. The amber (yellow) light gives an indication that there will soon be a phase change. The vehicles on queue must be on the alert to go while the approaching vehicles on the other crossing must slow to stop when the amber (yellow) light is on. The green light indicates go, it permits safe entry through the intersection.

However, it is expected of every driver to regard the safety of other persons within the intersection regardless of signal indications before crossing the junction. The four possible combinations for each unit of these colours is shown in table 1.1

Table 1.1   Traffic Combinations.

Colour combination		Indications
Red	●	
Amber	○	Stop
Green	○	
Red	●	
Amber	●	Get ready to move
Green	○	
Red	○	
Amber	○	Go, if road is free
Green	●	
Red	○	
Amber	●	Stop at stop line
Green	○	

The optical unit of a signal consists of a lens, a reflector, lamp and lamp socket. The lens is that part of the unit which redirects light from the lamp to the desired area. The reflectors of the signal lights would be lighted by 40-60Watts incandescent lamps that are coloured, with diameter between 6-8inches.

The type of mounting for signal heads suggested is along the roadway side or in the middle of the intersection with about 8-15feet high posts.

When the view of these signal heads is not physically obstructed, it should be clearly visible to drivers at distances up to 1000feet under normal atmospheric conditions. Each signal head should be so adjusted that its beams will be at maximum effectiveness to the approaching traffic.

1.5 TYPES OF ELECTRONIC TRAFFIC CONTROL SYSTEMS BASE ON THEIR MODE OF OPERATIONS

There are two main groups of roadway traffic signal based on their modes of operation. These include:

i.   Pre-timed traffic control systems

ii. Vehicle-actuated traffic control systems.

1.5.1 Pre-timed Traffic Signal Control System

A pre-timed signal control is a traffic control signal which directs traffic to stop and permits it to proceed in accordance with a single predetermined time schedule or series of such schedule. Its operation consists of a consistent regularly repeated sequence of signal indication given to the traffic. This type of signal is most efficient at intersections where traffic patterns are relatively stable over a long period of time. The total cycle length required for a complete sequence indication as specified in traffic manual is such that it may be adjusted from 30 seconds to a maximum of 120 seconds. With the use of attached auxiliary devices or remotely located supervisory equipment, the operation of pre-timed

control can be changed within certain limits to meet requirements of traffic more precisely.

1.5.2 Vehicle-actuated Signal Control System

The operation of the vehicle-actuated signal control systems varies in accordance with the demands of traffic as registered by the actuation vehicle or pedestrian detectors. In this case, a detector pad is placed in the carriage way at some distance back from each stop line and every vehicle approaching the section registers its approach by actuating the appropriate detector. Thus, traffic signals are automatically adjusted to meet the needs of the traffic signals are automatically adjusted to meet the needs of the traffic and this may vary from time to time throughout the day depending on the volume of traffic. It is important to note that many operating variations are possible with vehicle-actuated control. Each of this traffic signal control has its advantages over the other. Among these advantages include:

ADVANTAGE OF PRE-TIMED CONTROL

- Consistent starting time and duration of intervals of the pre-timed control facilitates co-ordination with adjacent traffic and provides more precise co-ordination than vehicle-actuated control.

- Pre-timed control may be more acceptable in areas with large and fairly consistent pedestrian than actuated control, and also where confusion may arise as to the operation of pedestrian push-buttons.

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- The installed cost of pre-time equipment is less than that of vehicle-actuated equipment and it is also simpler and more easily maintained.

ADVANTAGES OF VEHICLE-ACTUATED CONTROL

- Vehicle-actuated control may provide maximum efficiency at intersections where fluctuations in traffic cannot be anticipated and programmed for with pre-timed control.

- Vehicle-actuated control may provide maximum efficiency at complex intersections where one or more movements are subjected to variations.

- Vehicle-actuated control is preferred to pre-timed control in intersections where traffic control is needed for only brief periods during the day.

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CHAPTER TWO

2.0 THEORY OF SYSTEM COMPONENTS

2.1 INTRODUCTION

The basic electronic components which consist of resistors, capacitors, diodes, relays, and integrated circuits (IC) were used in the design of this project work. In figure 2.1 shown below, the block diagram representing the traffic light control systems is clearly shown. The whole operation of this system is based on the sequential operation of a 4 - bit decade counter and a BCD 1 of 10 decoder/driver unit. The sequence of light changes were obtained by decoding the outputs of the IC, 1 of 10 BCD decoder/driver unit which were then used to switch relays connected incandescent lamps fed from the domestic power supply.

```
        ┌──────────────────────────────┐
        │         POWER SUPPLY          │
        └──────────────────────────────┘
   ┌──────────┐      ┌──────────┐      ┌──────────┐
   │  PULSE   │─────▶│ COUNTERS │─────▶│ OUTPUTS  │
   │GENERATOR │      │          │      │          │
   └──────────┘      └──────────┘      └──────────┘
```
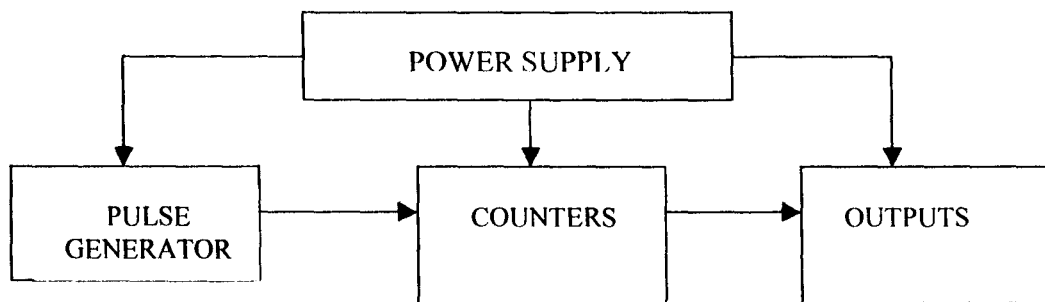
Fig 2.1 Traffic Lights Control System Block Diagram.

2.2 INTEGRATED CIRCUITS.

Integrated circuits are complete electronic circuits in which both the active and passive components are fabricated on an externally tiny single

silicon clip. These consist of large number of components working dependently to give fast and accurate response depending on what is meant to do.

2.2.1 Types of Integrated Circuits

Integrated circuits can be classified based on their functions as well as how they are constructed. Based on construction we have :

i. Monolithic integrated circuits

ii. Thick film integrated circuits

iii. Hybrid integrated circuits.

Based on their functions we have :

i. Linear integrated circuits

ii. Digital integrated circuits

The linear integrated circuits contain several amplifier circuits for either audio or radio frequency (RF) signals while digital integrated circuits contain an array of pulse switching circuits which are used in performing logic functions.

2.2.2 Advantages of Integrated Circuits

i. An IC is extremely small in size physically.

ii. It has a very small weight which makes it very important in military and space applications

iii. They are considerably cheap due to reduction in size and weight

iv. Integrated circuits consume very low power.

v. They are suitable for small signal operation.

2.2.3 Disadvantages of Integrated Circuits

i. They can only withstand very limited amount of power.

ii. Coils and inductors cannot be fabricated into IC form

iii. They are very delicate and cannot withstand rough handling and excessive heat.

2.2.4 Bipolar and Unipolar Integrated Circuits

Bipolar ICs are those made using bipolar junction transistors, BJT, example of this is the transistor transistor logic (TTL) ICs.

Unipolar ICs are those made using field effect transistors (FET and MOSFET), example of this is the complementary metal oxide semi – conductor (CMOS) ICs.

2.3 TRANSFORMERS

A transformer is an electrical apparatus which consists of two or more electrical circuits (primary and secondary windings). These circuits are interlinked by a common magnetic field for the purpose of transferring energy between the windings. The windings are wound on a magnetic core, which ensures that there is high magnetic flux linkage between the windings. The alternating voltage across a winding is due to induction from the altering voltage of the other windings. The induced voltage is a function of the number of turns of the windings. Turns is the number of times the wire (coil) is wound around the core.

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When the number of turns on the secondary winding is more than that of the primary, then we have a step-up transformer while when it is vice-versa, it is step-down transformer. The voltage, number of turns and the current are related as shown below in equation 2. 1

$$Vp/Vs = Np/Ns = Is/Ip \text{------------------}2.1$$

Where Vp, Np and Ip are the primary voltage, number of turns, and current in the primary winding of the transformer respectively, while Vs, Ns and Is are the voltage, number of turns, and the current in the secondary winding of the transformer respectively.

2.3.1 Transformer Construction

There are basically two types of transformers by construction. These are:

i. Core type

ii. Shell type

In the construction of the shell type, the winding coil is shielded by the core, while in the core type, the core is shielded by the coil winding.

2.3.2 Choosing and Specifying Transformers

Transformers are specified according to their power, voltage and current ratings of the secondary windings and the regulation.

Power rating is the product of voltage and current of the secondary winding which once the voltage and current ratings have been known is neglected.

Transformer regulation specifies the degree to which the secondary voltage varies with the load. It is very necessary to consider this when working out the maximum voltage rating of the smoothing capacitor.

Once the required voltage is known, it is necessary to choose a transformer which gives the output at the required current rating.

The minimum voltage of a transformer is given by :

$$V_{TXMIN} = V_{TX}\left[1 + \frac{Reg_{TX}(1 - I/I_{TX}) - Reg_{Mains}}{100} \right] \text{----- -----2.2}$$

The maximum voltage of a transformer is given by

$$V_{TXMAX} = V_{TX}\left[1 + \frac{Reg_{TX}(1 - I/I_{TX}) + Reg_{Mains}}{100} \right] \text{------2.3}$$

where,

V_{TX} = stated transformer voltage

I_{TX} = stated transformer current

I = current drawn from the transformer

Reg_{TX} = Stated transformer regulation factor = 13%

Reg_{Mains} = state mains regulation factor = 6%

It is important to note here that transformer minimum voltage evaluated at full load is used for selection of transformer, while the transformer maximum voltage evaluated at zero load is used to calculate the smoothing capacitor working voltage and the maximum voltage evaluated at full load is used to determine regulator power dissipation.

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2.4 DIODES

These are semi-conductor devices that allow the flow of current in one direction. Semiconductor diodes act on the basis of PN junction. It is constructed by combining a P-type and N-type semiconductor materials. Since diodes can pass current only in one direction within a specified limit, they are mostly used as switches. When a diode is reversed biased, it conducts a very low current until it researches a certain voltage called the breakdown voltage, at this, large current flows at constant voltage. A diode constructed to act in this form is called a Zener diode.

2.4.1 Diode Application

Diodes are used in the following circuits;

i.   Rectifying circuit

ii.   Chipping circuit

iii. Clamper circuit

iv.   Voltage doubler

v.   Over voltage and over current regulation

2.4.2 Rectification

This is a process of converting AC voltage or current to a DC voltage or current.

2.4.2.1 Types of Rectification

i. Half wave rectification

ii. Full wave rectification;

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a) Center tap rectifier.

b) Bridge rectifier

2.4.2.2 Full wave Rectification
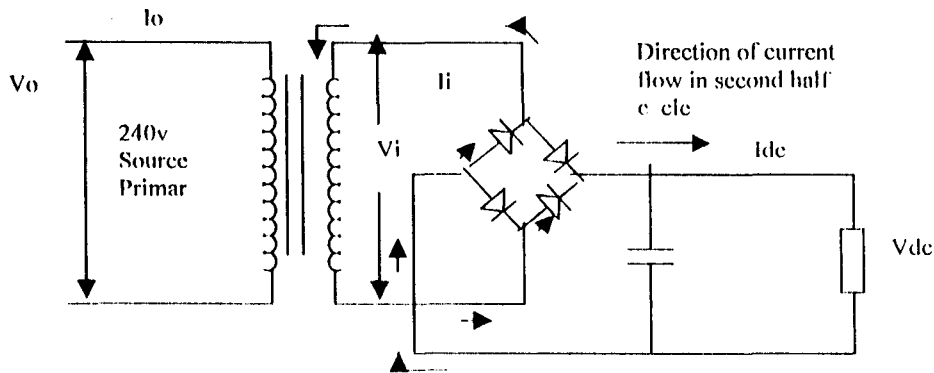
Fig 2.1 Full-wave Rectification Circuit with Resistive Load and Capacitive Filter.

$V_i = V_p$ Sin wt

$I_i = I_p$ sin wt

$$I_{rms} = \tfrac{1}{2}\pi \int_{0}^{2\pi} I^2\, d\,(wt) = I_p\sqrt{2} \dots\dots\dots\dots\dots\dots\dots\dots\dots 2.4$$

$$V_{rms} = \tfrac{1}{2}\pi \int_{0}^{2\pi} Vi\, d\,(wt) = V_p\sqrt{2} \dots\dots\dots\dots\dots\dots\dots 2.5$$

$$I_{dc} = \tfrac{1}{2}\pi \int_{0}^{2\pi} Id\,(wt) = 2I_p/\pi \dots\dots\dots\dots\dots\dots\dots\dots 2.6$$

$$V_{dc} = \tfrac{1}{2}\pi \int_{0}^{2\pi} Vi\, d\,(wt) = 2Vm/\pi \dots\dots\dots\dots\dots\dots\dots 2.7$$

With a resistive load;

$$V_{dc}\, 2\sqrt{2}/\pi\ V_{rms} = 0.9\ V_{rms} \dots\dots\dots\dots\dots\dots\dots\dots\dots 2.8$$

$$I_{dc} = 2\sqrt{2}/\pi I_{rms} = 0.9\ I_{rms} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots 2.9$$

With a capacitive filter;

$$V_{dc} = 1.41 V_{ac} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots 2.10$$

$$I_{dc} = 0.62\ I_{ac} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots 2.11$$

With a capacitive filter

$$V_{dc} = 1.41\ V_{ac}\text{---}2.10$$

$$I_{dc} = 0.62\ I_{ac} \text{---}2.11$$

Due to the diode voltage drop V_d,

$$V_{dc} = 1.42 V_{ac} - V_d \text{---}2.12$$

The waveform of the output of a full wave rectifier is given below in fig 2.2
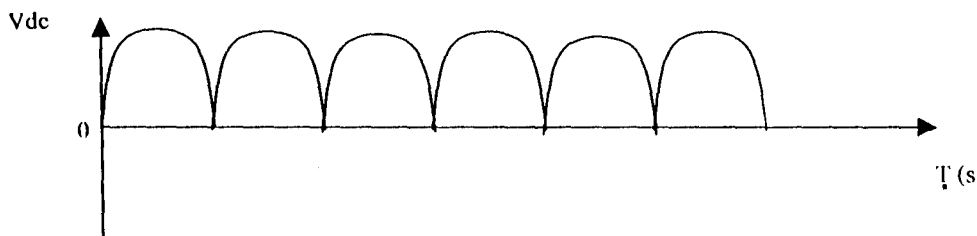
Fig 2.2 Waveform of a Full Wave Rectifier

2.4.3 Peak Inverse Voltage

This is the maximum voltage that occurs across the rectifying diode in the reverse direction. It is also the minimum voltage to which the diode can be subjected.

5 INTEGRATED CIRCUIT VOLTAGE REGULATORS

The two basic elements of a stabiliser circuit, i.e. the voltage reference and voltage amplifier, can easily be combined into an IC, offering the advantages of extremely good regulation, compact size and easy to use. The principle of operation is still based on the Zener diode mode of operation but with some added improvements. IC regulators are designed for specific fixed voltage.

An example of a typical IC regulator is shown in figure 2.3 below. C_A and C_B are decoupling capacitors that maintain low output impedance at all frequencies. The output impedance of all regulators tends to rise at high frequencies. It is very important to note that the minimum permissible input voltage of all IC regulators should be greater than their rating for proper functioning. Examples of typical IC regulators are 780s, 79L0S, 78H05, 79L05, 78L12, 317 etc.
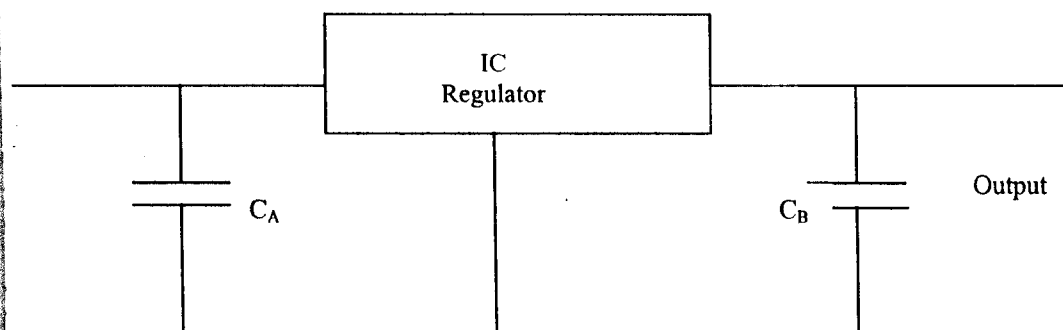
Fig. 2.3 IC Regulator Circuit Configuration.

2.6 TIMING CIRCUIT

In any electronics project where switching is required, it is very important to generate a pulse signal that will be able to change between two voltage levels (i.e. for digital circuits), so that one level will be for switching "off" (logic 0) and the other for switching "on" (logic 1), it could be vice-versa in the case of logic 0 and logic 1 depending on what is expected.

In this particular project, a continuous pulse is required for clocking the counter so it can change its output stage for each clock input, depending on whether the counter requires a negative going or positive going transition for its operation. The pulse will be generated using a 555 timer configured in an Astable manner.

2.6.1 The 555 Timer

The 555 is a monolithic circuit packaged in several ways. It has 8 pin-mini-DIP and has been found very useful in many electronics systems.

It is mostly used for timing circuits because of its high degree of accuracy and stability. It also exhibits a negligible drift with the supply voltage and its output current is about 200mA.

2.6.2 Configuration of a 555 Timer

    i.   Monostable or one shot multivibrator

    ii.   Astable or square wave clock multivibrator.

The mode of operation of the monostable 555 timer will not be discussed extensively as it irrelevant to this project designs, but the configuration,

the time width of the output to be at logic "1" and the output wave-form

will be given as show below in figure 2.4
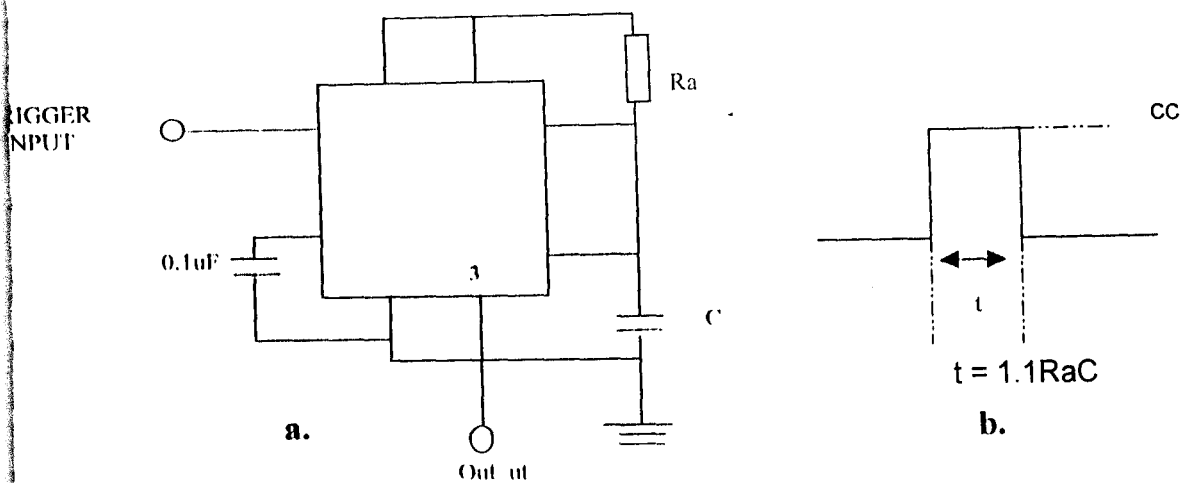
Fig. 2.4 (a) Monostable Multivibrator (b) Its Output Wave Form.

2.6.3 Astable Multivibrator

The astable or 'free-running' multivibrator is stable in neither state

(hence 'astable' which means not stable) but switches to and fro

from one state to the other to give a square-wave output, i.e. it is a

square-wave oscillator. It is also called a "clock" because of its use

to the various parts of a computer in step.

2.6.3.1   Astable Configuration of 555 Timer

In figure 2.5a and figure 2.5b, the configuration of a 555-timer astable

multivibrator is shown.
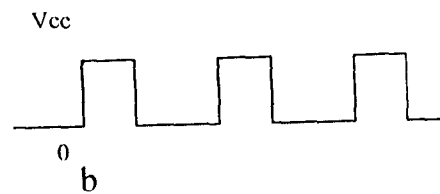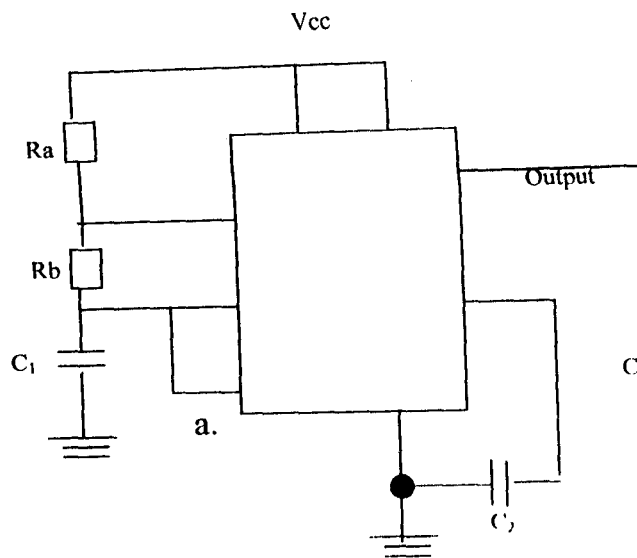
Fig. 2.5 (a) Astable 555 Timer   (b) Output Wave of an Astable 555 Timer.

A 555 timer configured as an Astable multivibrator is a continuous pulse generator for operating most digital circuits.

The operation of the 555 timer depends on the external resistors Ra and Rb and the capacitor C.

When there is supply voltage, the capacitor C charges through Ra and Rb to two-third (2/3) of the supply voltage and this effect makes the upper comparator inside the 555 timer to trigger the flip-flop which in turn causes the capacitor to start discharge through Rb. When the discharge researches one-third of supply voltage, the lower comparator is triggered and a new cycle is started.

2.6.3.2   Formulas

These are the formulas we used for the 555 timer to control the length of the pulse.

t_1 = charge time (how long the pulse is high)

$$= 0.693 \times (Ra + Rb) \times C \text{ -----------------------} 2.13$$

t_2 = discharge time (how long the pulse is low)

$$= 0.693 \times Rb \times C \text{ -------------------------------} 2.14$$

$$T = \text{period} = t_1 + t_2 = 0.693 \times (Ra + 2Rb) \times C \text{ ---------} 2.15$$

$$F = \text{frequency} = 1/T = 1.44/[(Ra + 2Rb) \times C] \text{ -----------------} 2.16$$

2.6.4 Duty Cycle

The duty cycle, D of a recurring pulses is defined as the ratio of the ON time to total cycle. It is the parameter that defines how the pulse shaping of the output pulse will look like.

$$D = \frac{t_1}{T} = \frac{Ra + Rb}{Ra + 2Rb} \text{ -------------------------------} 2.17$$

$$\% \text{ duty cycle} = \frac{Ra + Rb}{Ra + 2Rb} \times 100 \text{ --------------------} 2.18$$

When Rb is very large compared to Ra, then D= ½ × 100% = 50, this implies that the "ON" time t_1 is equal to "OFF" time t_2 and hence a symmetrical square wave is obtained. However, if Ra is made so large that it cannot be ignored, then we have a duty cycle higher than 50%, and this implies that the "ON" time, t_1 is greater than the "OFF" time t_2.

2.7 COUNTERS

A counter is a digital circuit that consists of n flip-flop connected in cascade whose function is to count the number of pulse applied to its input terminals. The maximum number of possible 1 and 0 state is known as the modules of the counter and these modules cannot be great than 2^n.

2.7.1 Types of Counters

Asynchronous or ripple counter is a counter of which the flip-flops are not in exact synchronism with the input pulse, this means that the first flip-flop is triggered by the clock and the output of which will trigger the second flip-flop etc.

Contrary to this, the synchronous or parallel counter is such that the output of the flip-flops change states immediately the pulse or clock is received. The advantage of this counter over a synchronous counters is that all the flip-flops change states simultaneously in parallel thereby reducing the propagation delay to an appreciable value.

2.7.2 Examples of Counters

Pure binary counter- It follows the normal binary counting sequence until $2^n - 1$ before it resets. Note that n is the number of flip-flops.

Decade counter- This is also known as BCD counters, when it counts in sequence from 0000 to 1001, it is a counter that has 10 distinct states no matter what the sequence is. In most cases, it consists of four flip-flops connected asynchronously or synchronously (depending on the maker and type) to count in binary from 0-9.

The mode of counting is as given in table 2.1 below

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Table 2.1 Output Sequence of a Decade Counter

Count	Output			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

2.7.3 IC DECADE COUNTERS

There are series of IC chips that can be configured to work as a decade counter. These include; DM74L590, TTL and HCC4017B CMOS IC, DM74L590 is a monolithic counter containing four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-five. It has a gated zero reset and gated set of nine inputs for use in BCD nine's complementent applications.

To use its maximum count length, the B input is connected to the QA outputs. The input count pulse are applied to input A and the outputs are as described in table 2.1 above.

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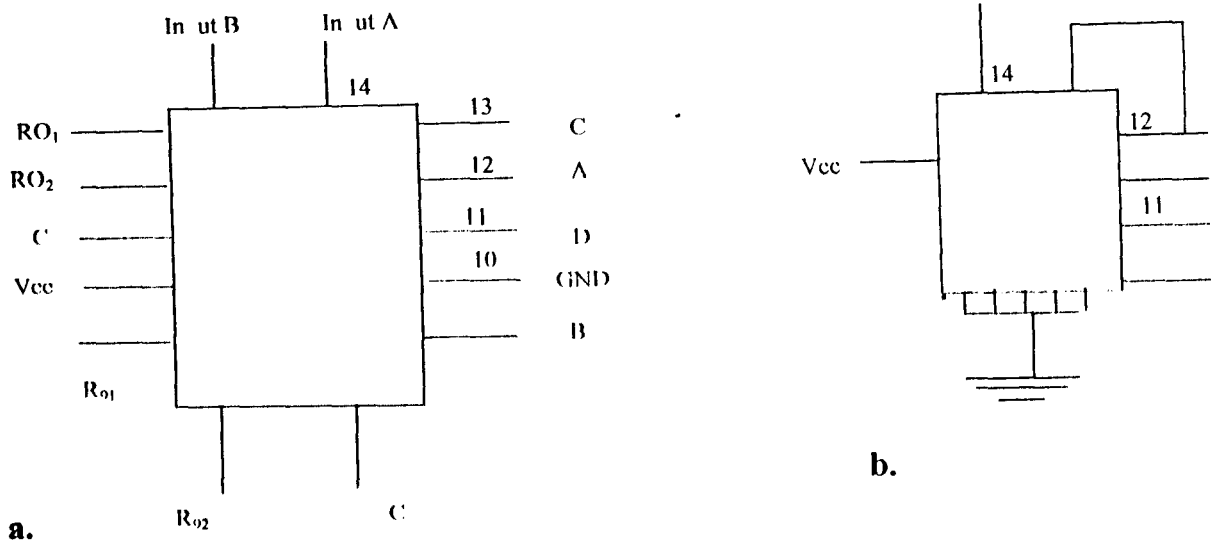
- Figure 2.6 (a) Pin Out of 7490 (b) Circuit Configuration of 7490

The power dissipation is 45mW with count frequency of 42MHzz and operating voltage between 3V and 9V dc.

2.8   DECODERS

A logic circuit that accepts a set of inputs that represents a binary and activates only the output that correspond to that input numbers is called a decoder.

Various types of decoders are available among which are:

   i.   Binary to octal or 3-line-to-8-line decoder

   ii.   BCD – to- decimal – decoder (1 of 10 decoder)

   iii.   BCD – to – Seven segment decoder.

Decoders are used whenever an output or a group of outputs is to be activated only on the occurrence of a specific combination of inputs. In BCD-to-decimal decoder, the input combinations from a counter i.e.

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74LS90 may be required to give a single output for each combination for use as a sequential counter in lighting display as the case is in this project.

2.9 CAPACITORS

A capacitor is a device that stores electrical energy in the form of an electrostatic field. They are widely used in filtering or to remove ac signals from a variety of circuits. In a dc circuit, they can be used to block the flow of direct current while allowing ac signals to pass.

Capacitors take a predictable time to charge or discharge and can be used in a variety of time-delay circuits.

The value of a smoothing (filtering) capacitor is determined by equation 2.19 below

$$C = \frac{IT}{V_{peak} - V_{reg}} \text{----------------------2.19}$$

Where

I = current drawn

T = period

V_{peak} = maximum voltage

V_{reg} = regulated voltage

Note that:

$$V_{ripple} = V_{peak} - V_{reg} \text{----------------------------------2.20}$$

2.10 RELAY

A relay is a coil with a specified inductance (LC, in Henry) that causes a contact to open or close when a specified current. I_{on} in Ampere charges it.

The magnetic relay can be used as a normally open or normally closed relay. It is activated when the current in the energising circuit exceeds the value of the switch-on current, I_{on}. During operation, the contact switches

from the normally closed terminals to the normally open terminals. The relay will remain on as long as the current in the circuit is greater than holding current, I_{hd}. The value of I_{hd} must be less than that of I_{on}.

The contact remains in the same position until the current falls below the holding value, I_{hd} in Ampere, at which point it returns to its original position.

The energizing coil of the relay is modelled as inductor, and the relay's switching contact is modelled as resistors. The circuit diagram of a relay is shown below.
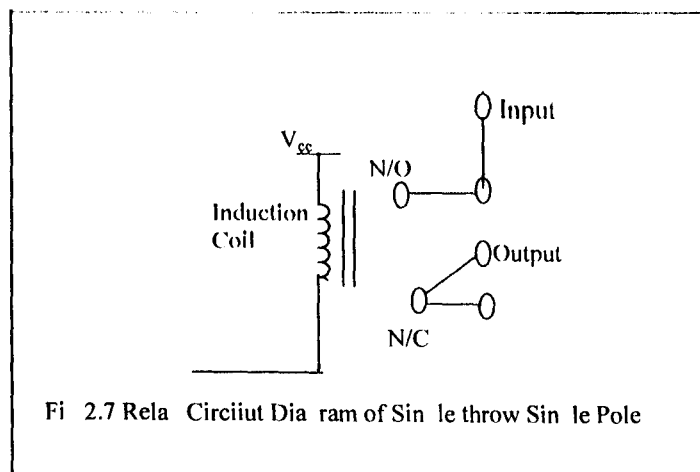
Fi 2.7 Rela Circiiut Dia ram of Sin le throw Sin le Pole

CHAPTER THREE

3.0 DESIGN AND CONSTRUCTION.
3.1 INTRODUCTION.

As it was stated in the previous chapter, the whole operation of the traffic control system is based on the sequential operation of a 4-bit decade counter and the output of 1 of 10 BCD decoder/driver.

The power supply unit consists of a transformer with two voltage regulators — 5 and 9 volts dc, except for the mains needed to run the incandescent lamps. The sequence of the changes of the light bulbs obtained by decoding the output of the 1 of 10 BCD decoder/driver. The outputs of this IC were then used to switch relays connected to the lamps fed from the domestic power supply.

3.2 DESIGN SPECIFICATION

It is expected that the traffic light control systems should meet the following general specification:

i. It should be powered by a 240 Volts AC mains supply, which is then converted to 5 volts and 9 volts by the use of voltage regulators after stepping it down by a transformer.

ii. In order to obtain the logical operation of load circuit, a pulse generator (in this case an astable configured 555 timer) should be used in the generation of train of pulses.

iii. The input of the decade counter should be fed by the output of the pulse generator.

iv. The output of the decade counter should be connected to the input of the 1 of 10 BCD decoder/driver.

v. The output from the 1 of 10 BCD decoder/driver should be capable of driving the relay circuit that consists of diodes, relays and electric bulbs

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rated 40 Watts each. Since the pulses from the decoder is active low, the use of transistors in the relay circuit was necessary.

The various stages of the traffic light control system (block diagram) is shown in figure 2.1

3.3 POWER SUPPLY

The power supply functions basically to provide the necessary dc voltage with low level of ac ripple and with good stability and regulation. It is important to state here that sometimes the source of this power supply could be a battery, but often power is obtained from a unit that converts the normal single-phase ac mains supply from local source (e.g. NEPA) 240 Volts to some different value of ac voltage. One of the various methods of achieving a stable dc voltage from ac mains is by the use of linear stabiliser.

In the case of this project, 240/12 volts centre tapped step-down transformer was used to step down the ac voltage. The desired 5volts and 9volts for the logic circuit and the relay circuit respectively were then realised using a full-wave bridge rectifier to steady dc voltage with respective voltage regulators connected in parallel to the output of the transformer.

The rectifier unit that converts the ac voltage into unidirectional current pulses as shown in figure 3.1 has four diodes – D1, D2, D3 and D4 with IC voltage regulators the principle of operation has been explained in section 2.4.2.

3.3.1 Component and Values

Transformer : one 240/ 12 volts dc output

Diodes: D1 = D2 = D3 = D4 = 1N4007

Capacitor : 220uF, 25 volts

IC1 : 7809 voltage regulator

IC2 : 7805 voltage regulator
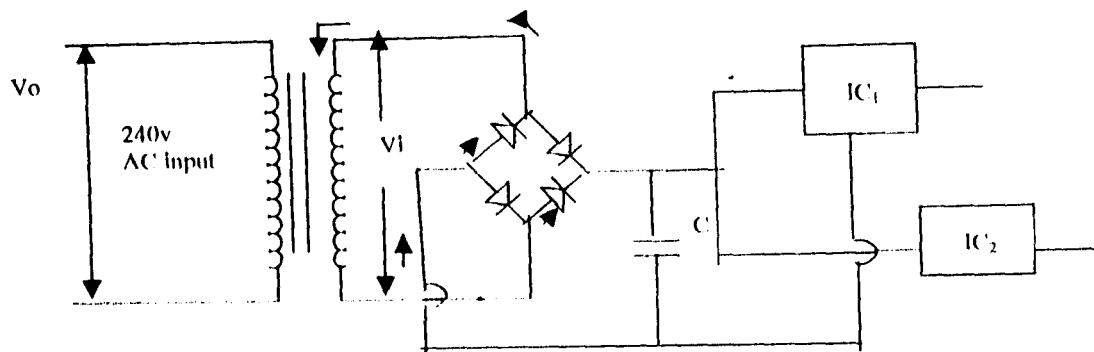
Fig 3.1 Regulated Power Supply For 5volts and 9volts dc Output

3.4   THE PULSE GENERATOR

The 555 timer configured in astable mode was used in this project work to generate pulses that drives the decade counter which consequently drives the decoder. The timer has voltage specification of 5 – 18 volts input and when operated from a 5volts supply as the case is here, it is compatible with integrated circuit, Transistor – Transistor Logic (TTL). The pin out and the diagram of 555 timer configured in astable mode is shown in figure 2.5a.

For this project, the period of each pulse was chosen to be five seconds, i.e. T = 5secs. To achieved this period, the values of an Ra and C were chosen to be 10k and 10uF respectively. from equation 2.16 we can now calculate the value of Rb.

i.e. $1/T$ = $1.44/[Ra + 2Rb) \times C]$

      T   = $[(Ra + 2Rb) C] / 1.44$

      5   = $[(10,000 + 2Rb) \times 10 \times 10^{-6}]/1.44$

     7.2   = $(10,000 + 2Rb) \times 10 \times 10^{-6}$

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$$10,000 + 2Rb \quad = \quad 720 \times 10^3$$

$$2Rb \quad = \quad 710 \times 10^3$$

$$Rb \quad = \quad 355K$$

A choice of 357KΩ resistor was chosen and a potentiometer of 470KΩ was used to vary out the needed value.

3.4.1 Components and Values

Resistor Ra = 10 K Ω

Resistor Rb = 375 K Ω

Capacitor C = 10μF, 16V.

555 timer = LM555IC

3.5 IC COUNTERS AND DECODER/DRIVER

3.5.1 The 74LS90 IC

This is a synchronous counter known as a decade counter. It is a counter packaged in Transistor-Transistor Logic (TTL) which contains parallel connections of four flip-flops. This counter counts from 0 to 9 in its binary equivalent i.e. 0000, 0001, etc to 1001. the table below shows the counting sequence of a 74LS90 decade counter. The outputs of this counter were decoded using logic gates. Logic gate is a device that performs a predetermined logic operation according to its logic function. For the purpose of this project, the choice of 74LS90 was made of which the outputs were to drive the BCD 1 of 10 decoder/driver.

Table 3.1 shows the true table of 74LS90 decade counter and the pin out is shown in figure 2.6a

3.5.2 The 74LS145 IC

This is the IC of which the outputs were used in driving the relays and subsequently the traffic lights. This is a BCD – to – decimal decoder/driver. It consists of eight inverters and then four input NAND

gates. These decoder feature high performance, n-p-n transistors designed as indicator/relay drivers or as open collector logic-circuit drivers.

Table 3.2 shows the truth table of the BCD to decimal decoder/driver. This IC was used in the design of this project.
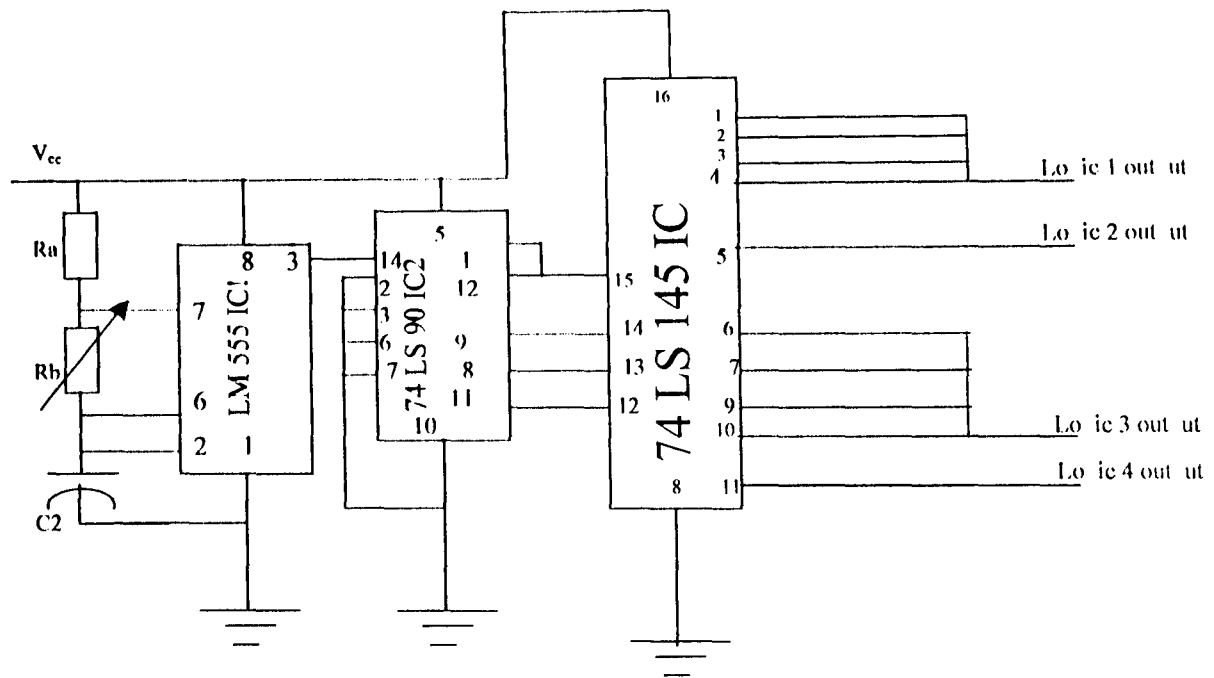
Fig 3.2 The Logic Circuit Diagram of Traffic Lights Control System

Table 3.2 Truth Table of BCD to Decimal Decoder/Driver IC

NO.	INPUTS				OUTPUTS										NO. OF PERIODS
	Q_D	Q_C	Q_B	Q_A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	0	0 1 1 1 1 1 1 1 1 1										Period 1
1	0	0	0	1	1 0 1 1 1 1 1 1 1 1										Period 2
2	0	0	1	0	1 1 0 1 1 1 1 1 1 1										Period 3
3	0	0	1	1	1 1 1 0 1 1 1 1 1 1										Period 4
4	0	1	0	0	1 1 1 1 0 1 1 1 1 1										Period 5
5	0	1	0	1	1 1 1 1 1 0 1 1 1 1										Period 6
6	0	1	1	0	1 1 1 1 1 1 0 1 1 1										Period 7
7	0	1	1	1	1 1 1 1 1 1 1 0 1 1										Period 8
8	1	0	0	0	1 1 1 1 1 1 1 1 0 1										Period 9
9	1	0	0	1	1 1 1 1 1 1 1 1 1 0										Period 10

It is important to note that the outputs of BCD to decimal decoder/driver are high at low state, i.e.

"0" = high

"1" = low

The decoded outputs of the 74LS145 were used to design the traffic lights control system. The function table below shows how this is used and the logic combinations that was obtained for the roads.

Table 3.3 Function Table Showing How Decoded Outputs of the Decoder was Applied to the Roads.

OUTPUT OF BCD TO DECIMAL DECODER/DRIVER										ROAD N			ROAD E			ROAD S			ROAD W			PULSE PERIOD (S)
0	1	2	3	4	5	6	7	8	9	R	A	G	R	A	G	R	A	G	R	A	G	
0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	1	1	5
1	0	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	1	1	5
1	1	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	1	1	5
1	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	1	1	5
1	1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	0	1	0	0	1	5
1	1	1	1	1	0	1	1	1	1	0	1	1	1	1	0	0	1	1	1	1	0	5
1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	0	0	1	1	1	1	0	5
1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	0	0	1	1	1	1	0	5
1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	0	0	1	1	1	1	0	5
1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1	0	0	1	1	0	1	5

From the function table of Table 3.3, R, A and G represents the Red, Amber and the Green lamps respectively. It can be observed from this function table that for periods 1,2,3 and 4, the green lamp of road N comes up indicating that road N vehicles can move. Likewise Road S, the same periods keep the green lamp of the road S on.

For period 5, as the vehicle on road N and road S are stopping, those on roads E and W are getting ready to move. We can observe that for periods 6,7,8 and 9 the green lamp of road E comes up and also the green lamp of road W indicating that vehicles on these roads can move.

For period 10, as the vehicles on roads E and W stop moving, those on roads N and S get ready to move.

From Table 3.2, the transition for each of the periods can be written in Boolean Algeria as shown below:

For period 1

$\bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{Q}_D$

For period 2

$Q_A \bar{Q}_B \bar{Q}_C \bar{Q}_D$

For period 3

$\bar{Q}_A Q_B \bar{Q}_C \bar{Q}_D$

For period 4

$Q_A Q_B \bar{Q}_C \bar{Q}_D$

For period 5

$\bar{Q}_A \bar{Q}_B Q_C \bar{Q}_D$

For period 6

$Q_A \bar{Q}_B Q_C \bar{Q}_D$

For period 7

$\bar{Q}_A Q_B Q_C \bar{Q}_D$

For period 8

$Q_A Q_B Q_C \bar{Q}_D$

For period 9

$\bar{Q}_A \bar{Q}_B \bar{Q}_C Q_D$

For period 10

$Q_A \bar{Q}_B \bar{Q}_C Q_D$

From the above logic transition we therefore proceed to show the transition of each road:

For road N green and red lamps

Period 1 + Period 2 + Period 3 + Period 4

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$$\overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, \overline{Q}_D + \overline{Q}_A \, Q_B \, \overline{Q}_C \, \overline{Q}_D + Q_A \, Q_B \, \overline{Q}_C \, \overline{Q}_D = \overline{Q}_C \, \overline{Q}_D$$

For road N amber lamp

Period 5 + Period 10

$$\overline{Q}_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

$$= \overline{Q}_B$$

For road E green and red lamps

Period 6 + Period 7 + Period 8 + Period 9

$$Q_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + \overline{Q}_A \, Q_B \, Q_C \, \overline{Q}_D + Q_A \, Q_B \, Q_C \, \overline{Q}_D + \overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

$$= \quad Q_A Q_C + \overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

For road E amber lamp

Period 5 + Period 10

$$\overline{Q}_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

$$= \overline{Q}_B$$

For road S green and red lamps

Period 1 + Period 2 + Period 3 + Period 4

$$\overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, \overline{Q}_D + \overline{Q}_A \, Q_B \, \overline{Q}_C \, Q_D + Q_A \, Q_B \, \overline{Q}_C \, \overline{Q}_D$$

$$= \quad \overline{Q}_C \overline{Q}_D$$

For road S amber lamp

Period 5 + Period 10

$$\overline{Q}_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

$$= \quad \overline{Q}_B$$

For road W green and red lamps

Period 6 + period 7 + period 8 + period 9

$$Q_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + \overline{Q}_A \, Q_B \, Q_C \, \overline{Q}_D + \overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D + Q_A \, Q_B \, Q_C \, \overline{Q}_D$$

$$= Q_A Q_C + \overline{Q}_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

For road W amber lamp

Period 5 + Period 10

$$\overline{Q}_A \, \overline{Q}_B \, Q_C \, \overline{Q}_D + Q_A \, \overline{Q}_B \, \overline{Q}_C \, Q_D$$

$$= \quad \overline{Q}_B$$

3.5.3 Components and Values

The 74LS145 BCD to decimal decoder/driver.

The 74LS90 Decade counter.

3.6 OUTPUT STAGE

An interfacing unit is required for this project to handle 240volts ac mains. This interfacing unit is what is called the output stage and it could be made of solid state using thyristors or triac networks or made electrochemically by using transistors and relays. For this project, the output stage is made up of switching diodes, relays and indicator lamps. Since the output of the decoder is high at low state, there is no need amplifying the circuit with transistors.

When the output of the logic circuit is high so that there is a complete circuit with the relay, about 6volts connected to the relay will appear across the relay coil. With this, the coil becomes energised and this consequently closes the normally open terminal thus closing the ac path through the lamp, the lamp then turns on. This lamp remains on for as long as the logic output is in the high state.

On the other hand, when the output of the logic gate turns to low, the coil of the relay is de-energised and this brings the contact to be open and the lamp goes off.

This explanation is for the normally open contact that was used in this project for the contact of the lamps. The relay used here is a single pole-single throw relay. The circuit diagram for a relay is shown in figure 2.7 above.

3.6.1 Components and Values

Relay coil resistance = 4.2 KΩ

Relay voltage Vr = 6 Volts

Diodes D5-D10 = IN4007

3.7 CONSTRUCTION

The project or bread board was first used to build and wire the complete circuit of this project. The relay contacts were confirmed to be behaving as expected on the board. On achieving this positive response, the circuit was then carefully built on the Vero board. IC sockets were first inserted where it was necessary on the board and then soldered. Similarly, other components were carefully soldered on the board. Finally, the ICs were then placed into the IC sockets where the provision has been made.

3.7.1 Coupling and Testing

The circuit was assembled together to give a complete traffic control system for a 4-way junction. The signal indicators were made of three colours of lamps for each signal head for the roads. These colours consists of the red lamp on top, amber in the middle and the green lamp at the bottom.

The bulbs rated 40-watts each were connected to the mains supply with relay contact as switches. After ensuring that the coupling was done neatly and properly, the overall circuit was tested and found in good working condition.

The circuit design diagram is enclosed in this project book.

3.8 RESULTS AND ANALYSIS

In Table 3.3 of this project work, the result of this project has been elaborately tabulated. The clock pulse whose period depends on the duration desired was produced by the pulse generator (555 timer). It can be seen also that the Table 3.3 shows the sequence and periods for each of the lamps. We see from this table that each state represents a clock

pulse and the combination of these pulses were used in the operations of the different time length of the lamps.

Table 3.2 shows how these states have been separated into periods, i.e. periods 1 to 10. We observe that the green lamp of road N and the red lamp at road E come up for the first four periods, likewise the green lamps and the red lamp of roads S and W respectively.

In period 5, the amber lamps come up and this is followed by the green lamps of roads E and W and red lamps of roads N and S for period 6,7,8 and 9.

Finally, period 10 turns on the second sequence of the amber lamps. It is important to note here that the red lamps follows the amber when amber has been on by itself alone.

3.9   SUMMARY OF OPERATION

The power supply is from ac mains, 5 and 9 volts DC were regulated out using voltage regulators after stepping down with a 240/12 volts transformer which was rectified using bridge rectification.

The 5volts dc supply provides the source for the pulse generator (555 timer) to operate and it subsequently serves as the source for the logic circuit. The relay switches were activated by the 9 volts dc supply.

The pulse generator provides clock pulses which were used to trigger the decade counter. The output of the decade counter were then decoded using the BCD to decimal decoder/driver. The output of this decoder is connected to the final stage of this project work. As mention earlier, the final stage consists of relays, switching diodes and lamps. Depending on the state of these relays, the lamps were turned on or off as the case may be.
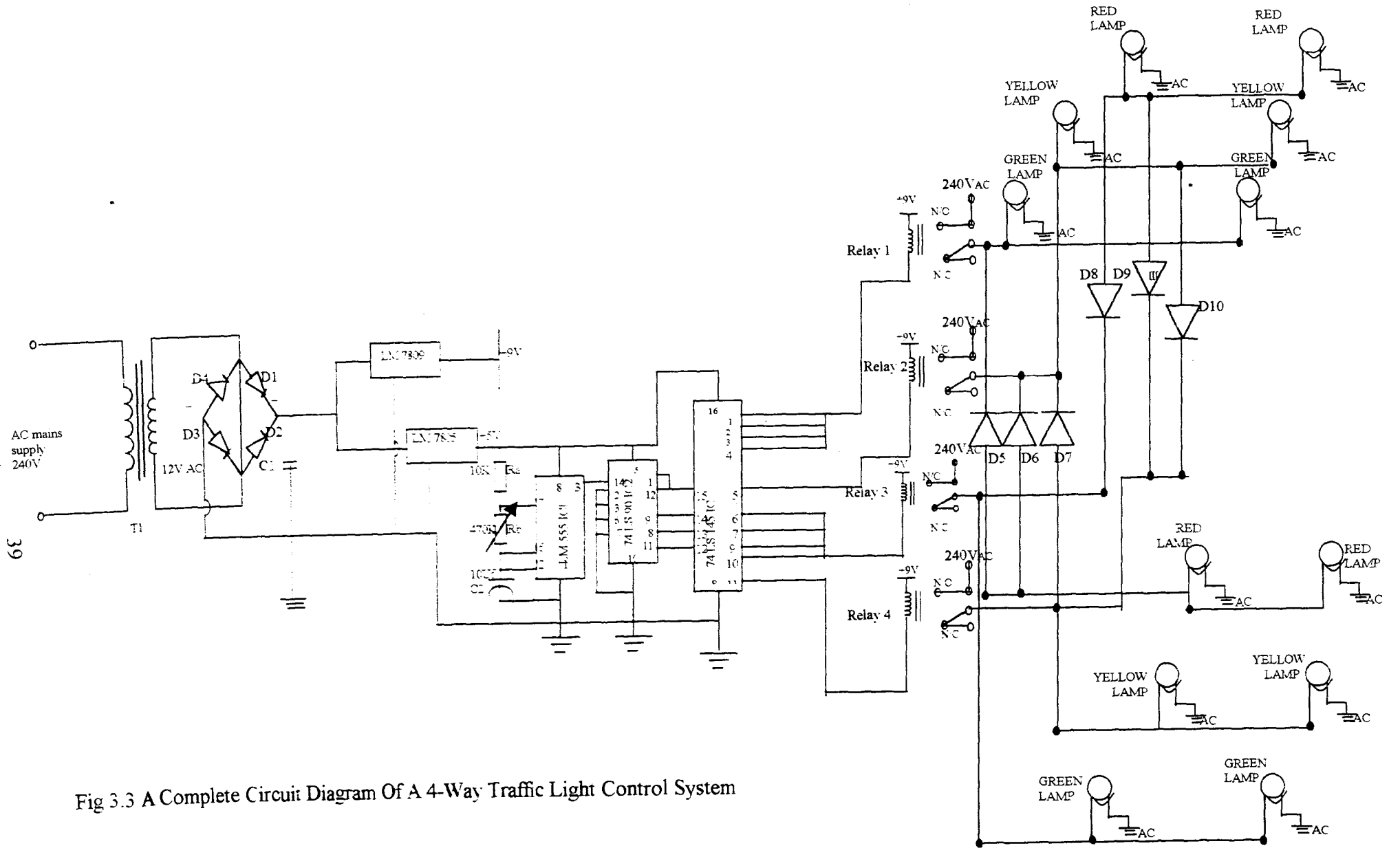
Fig 3.3 A Complete Circuit Diagram Of A 4-Way Traffic Light Control System

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CHAPTER FOUR

4.0 CONCLUSION AND RECOMMENDATION

4.1 CONCLUSION

It can be concluded that a pre-timed traffic control system for a 4-way junction has been designed and constructed. With careful combination of this logic circuit of this control system, other sequence can be achieved which can be used for traffic control of similar junctions.

4.2 RECOMMENDATION

I recommend the following based on the above mentioned problems:

i. The electrical laboratory should be equipped with testing equipment such as IC test equipment

ii. Books that contain information like the traffic codebook should be made available in the University Library.

iii. An advance project books on the use of EPROM for traffic control system should be made available also in the University Library.

4.3 PROBLEMS ENCOUNTERED

In the cause of designing and constructing this project work, the major problems problem encountered include:

i. The difficulty in combining the lamps in logic sequence with the logic combination. Nevertheless browsing through the internet helped greatly.

ii. There was no means of verifying if an IC is functioning normally or not, so trouble shooting was hectic.

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APPENDIX

Advantages of CMOS over TTL ICs

i. Low power dissipation, typically 10nW per gate.

ii. Wide operating temperature range, - 40 C to +85 C.

iii. High D.C fan-out.

iv. Wide operating supply voltage range, +5V to +15V.

v. Excellent noise immunity.

vi. Inputs and outputs are protected against electrostatic voltages.

vii. Buffered outputs on all circuits.

Advantages of TTL over CMOS ICs

TTL IC's can withstand rough handling to a greater extent.

Basic characteristics of TTL ICs

Power dissipation ---------10nW

Propagation delay ----------10nS

Noise margin ----------------0.4V

Fan – out ---------------------10

Supply voltage ------------5V +/- 0.25V

In addition to the normal supply

connected as

generated as

A2

nnected, about 1mA of current must be drawn out to hold them at

0. The output can sink up to 16mA (enough to light an LED), but

source only about 2mA. To switch larger currents, they are

appropriate transistors. The frequency of TTL ICs is about

(the right conditions).