DESIGN AND CONSTRUCTION OF DIGITAL DOOR LOCK WITH AUDIO ALARM

BY

FAYOMI GODWIN DELE
99/8169EE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING.

SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY.

FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA
NIGER STATE, NIGERIA.

NOVEMBER 2005.

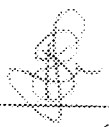
ATTESTATION

This is to attest that this project work titled "Design and construction of digital door with audio alarm" was carried out by Fayomi Godwin Dele {99/8169EE} for the award of bachelor of engineering (B.Eng) degree in electrical/computer engineering Federal university of technology, Minna.

Project supervisor (Mr. E. M Eromu)	sign and date
H.O.D (Engr. M. D Abdullahi)	sign and date
External examiner	sign and date

DECLARATION

I hereby declare that the project was wholly designed and constructed by me under the supervision of Mr. E. M Eronu, department of electrical and computer engineering, Federal university of technology, Minna.



(Signature of student)

06 - 10 - 2015

Date

ACKNOWLEDGEMENT

Let me begin by acknowledging the undying mercies of God who was the ackbone of my studies in this institution and for sparing my life and for the grace He has iven me.

I wish to express my profound gratitude to my project supervisor, Mr. E M Eronu or painstakingly going through my work and his guidance.

I do also owe great thanks to my head of department, Engr. M. D Abdullahi, level dvisers and the entire staff of the department for their fatherly advice throughout my ears on this course.

I whole heartedly appreciate the love, care, prayers and support given to me by y dear parents; Reverend and Mrs. Paul Obamudi, you are one of parents.

I am not going to forget my uncles and aunties who were like angels sent to my ay. Auty Yemi, you are a mother indeed, uncle Zachaeus Fayomi, thanks for your nancial support, uncle Kola and Tom. I do appreciate your kind gestures extended to me uring this period. I thank aunty Comfort and Elizabeth for their support. I equally thank y grand parents; Mr. and Mrs. Fayomi for their prayers and support.

I indeed want to thank my mother; Mrs. Oke for her moral support. What will I ay of my ever loving younger ones; Judith, Joy, Tolu; thanks for being there for me. People die but memories don't" the family of late elder Idris is God-sent.

I will not stop until I acknowledge the love and care given to me by these sisters: hristy Solomon, Vivian Solomon, Lydia Solomon, if blood sisters are to be chosen, I ill choose you all.

I appreciate the entire family of the word of hope church for their prayers and upport. Lastly, I appreciate my friends, Bulebu, Ngbede, Sir peelo, Chikezie, Asuquo, nnocent, Oshopee and a host of good people I ran into during the course of this program. hank you all.

DEDICATION

I dedicate this work first to the almighty God and then to my father; Rev. Paul Obamudi and late elder Idris Simon.

ABSTRACT

This project was aimed at designing and constructing a digital door lock with audio alarm.

There are traditional ways of locking doors, security posts, gates e.t c. the safety of these methods is not guaranteed. Burglars or intruders can easily manipulate their way through this means of locking systems. These systems stand the risk of key forgery and the use of the so-called "master key". Hence the introduction of a digital door lock with an audio alarm can put a check to all the above stated problems associated with the traditional ways of locking.

This access control system has been designed in such a way that a code has to be used to unlock and lock the door. If three incorrect codes are entered through the keypad to the circuit, the alarm unit will be triggered on and this will alert the security men around. Access can only be granted when the right code is entered into the circuit.
For this aim to be properly achieved, several CMOS ICs used are, CD4017BC, CD4063B, MC 14060B, CD4013, CD4076B, IN9149 and other associated components are used.
The CD4017 acts as a counter, CD4076 and CD4013 act as registers for code storage. The CD4063B was being used as a comparator to compare inputted codes or password with the default code. The circuit is powered by a 220/9V step down transformer.

TABLE OF CONTENT

'ONTENT **PAGES**

TLE PAGE i

TTESTATION ii

ECLARATION iii

CKNOWLEDGEMENT iv

EDICATION vi

BSTRACT vii

ABLE OF CONTENT viii

HAPTER ONE 1

0 INTRODUCTION 1

1 BACKGROUND 1

2 AIM AND OBJECTIVE 2

HAPTER TWO 3

0 LITERATURE REVIEW 3

1 DEVELOPMENT OF LOCKS 3

1.1 INVENTIVE INGENUITY 4

HAPTER THREE 6

ATERIALS AND METHODS 6

1 BLOCK DIAGRAM 6

2 DESIGN ANALYSIS 6

3 CIRCUIT DIAGRAM 9

3.4 THEORY OF OPERATION.....9

3.5 COMPONENTS AND COMPONENTS DESIGN.....13

CHAPTER FOUR.....36

CONSTRUCTION, TESTING AND RESULTS.....36

4.1 CONSTRUCTION.....37

4.2 TESTING.....37

4.3 RESULTS.....37

4.4 DISCUSSION OF RESULTS.....38

CHAPTER FIVE.....38

CONCLUSION AND RECOMMENDATIONS.....38

5.1 CONCLUSION.....38

5.2 RECOMMENDATIONS.....38

REFERENCES.....39

CHAPTER ONE

1.0 INTRODUCTION

In this modern age where science and technology is rapidly advancing and improving, the use of key locks for doors and for security posts can no longer be said to be reliable. Today, with the use of the so-called "master key", intruders and unauthorized persons can easily gain access to secured places through barriers with key locks. Many houses, banks, supermarkets, industries e.t.c have been illegally broken into due to the fact that owners of the above mentioned secured places employed the use of key locks in their access control systems.

Consequently, there has been a need to construct a lock mechanism that will be almost absolutely reliable and serves as a check for unauthorized users. So, this access control device- digital door lock with audio alarm- is user friendly and does not require any technical knowledge for its usage.

1.1 BACKGROUND

The circuit of this project-digital door lock with audio alarm- is designed for locking and unlocking door/doors. It is incorporated with low power consumption complementary metallic oxide semiconductors (CMOS) integrated circuits (ICs).

It is equally designed with a security audio alarm which is triggered on when ever three incorrect numbers (codes) are entered through the keypad into the circuit to get the door opened.

The locking and the unlocking code can be altered, which creates room for flexibility and safety of the locking system.

1.2 AIM AND OBJECTIVE

The purpose of this project is aimed at providing the following:

- a more reliable security system in houses, supermarkets, security posts e.t.c
- Elimination of the risk of key misplacement.
- Elimination of the inconvenience of walking about with keys and
- Frustration of the use of forged keys by burglars.

CHAPTER TWO

2.0 LITERATURE REVIEW

A lock is a mechanical device used for fastening doors, chests and lids consisting essentially of a bolt guarded by a mechanism which can be released by a mechanical, hydraulic or electrical/ electronic (actuator) .

Locks and key were known long before the birth of Christ – about 445BC. At this time, locks were made of wood. They were large and crude in design, yet their principle of operation was the forerunner of the modern pin- tumbler locks of today. As locksmiths and metal workers became proficient in their craft, they were invited to make locks and keys for the royal courts and for the churches and cathedrals of Europe.

2.1 DEVELOPMENT OF LOCKS

The first mechanical locks, made of wood, were probably created by a number of civilizations at the same time. Records show them in use some 4,000 years ago in Egypt. Fastened vertically on the door post, the wooden lock contained moveable pins or "pin tumblers," that dropped by gravity into openings in the cross piece or "bolt," and locked the door. It was operated by a wooden key with pegs or prongs that raised the number of tumblers sufficiently to clear the bolt so that it could be pulled back.

The first all-metal locks appeared between the years 870 and 900, and are attributed to the English craftsmen. (Robert Barson and Linus Yale Jr.) They were simple bolts, made of iron with wards (obstructions) fitted around the keyholes to prevent tampering.

The first use of wards (fixed projections in a lock) was introduced by the Romans who

devised obstructions to "ward off" the entry or turning of the wrong key. Wards were notched and cut into decorative designs, and warding became a basic locking mechanism for more than a thousand years.

New concepts for locking devices were developed in Europe in the 17th century. Early Bramah locks utilized a series of sliders in a circular pattern to provide exceptional security. Bramah is the oldest lock company in the world and is continuing to manufacture its famous mechanism 200 years later.

2.1.1 INVENTIVE INGENUITY

As lock-picking became an art in the 18th century, the inventor met the challenge of the burglar with increasingly complicated locking mechanisms. Among the new improvements were keys with changeable bits, "curtain closed-out" around keyholes to prevent tampering, alarm bells combined with the action of the bolt, and "puzzle" or ring padlocks, with this principle developing into dial face and bank vault locks, operating without keys and known as combination locks.

The early puzzle padlocks were Oriental with from three to seven rings of characters or letters which released the hasp when properly aligned. The dial locks were similar in operation, and both types were culminated to unlock to words or patterns of numbers known only to the owners or responsible persons.

At the left is the Eureka, a manipulation-proof combination lock with five tumblers. For a faithful bank vault used at one time in the U.S. Treasury Department. Patented in 1862 by Dodds, MacNeal, and Urban of Canton, Ohio. The operating dial is a combination of

letters and numbers and affords 1,073,741,824 combinations, to run through them all without interruption would take 2,042 years, 324 days, and 1 hour.

In the 19th century, ward locks were improved and tumbler locks, cylinder locks and keyless locks were invented.

Many and different kinds of locks were in parade in the 20th century. Today, locks can either be key operated or keyless. In automobile ignition, electromechanical locks were developed to trip electrical circuit. Unfortunately, being in the 20th century, the uses of locks with keys are completely unreliable.

The keyless types are the most modern locks. They came into existence in the late 20th century. They are often remote controlled, security card operated and electronic in nature.

The exciting part of this project is that aside the fact that it is designed to respond to an electronic logic signal with a digit sequence counter performing the function of the key; it equally has an audio alarm to alert security men or authorized users when ever there is an intrusion from unauthorized persons.

CHAPTER THREE

MATERIALS AND METHODS

3.1 BLOCK DIAGRAM

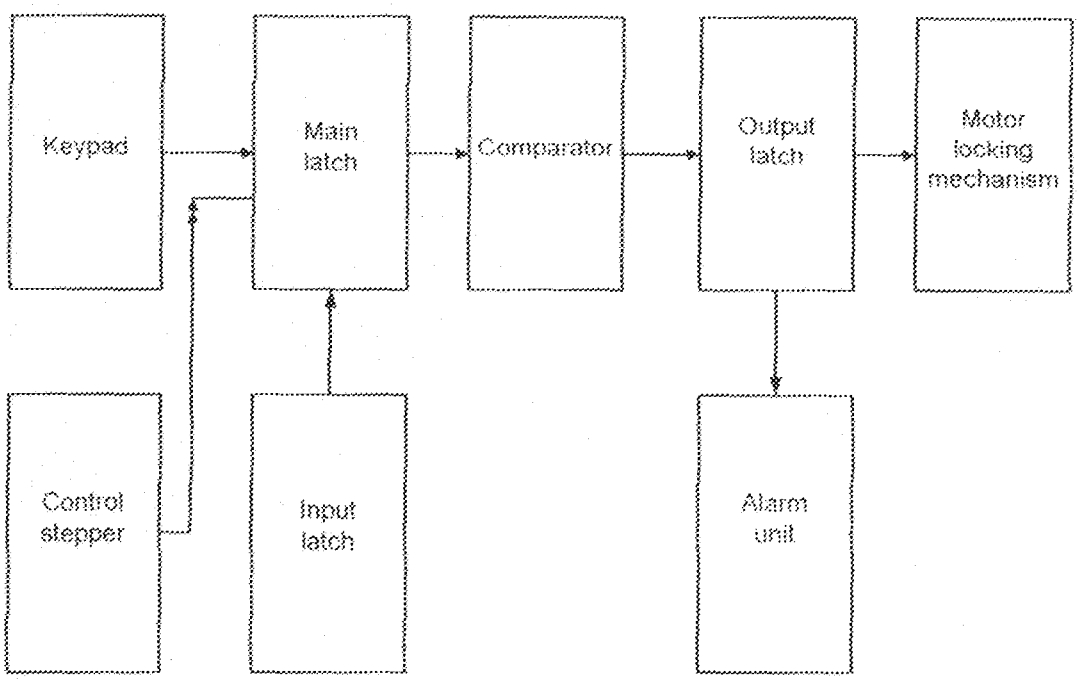


Fig. 3.0 The block diagram

3.2 DESIGN ANALYSIS

KEYPAD

Codes or numbers are entered into the circuit via the keypad. The code is meant to lock and unlock the digital door lock.

CONTROL STEPPER

The control stepper (4017 IC) being a counter controls the accessing of the latches (input and the main latch) so that numbers entered into the circuit via the keypad can be processed sequentially.

MAIN LATCH

The main latch is made up of three CD4076B ICs. The CD4076B is a register- four bit-. Each of this store one digit of the three-digit code that is sequentially entered through the keypad to the circuit.

INPUT LATCH

The input latch is made up of a CD 4013B IC (CMOS dual 'D'- type flip-flop). In this design, it acts as a shift register. It registers all the inputs (numbers) and then transfers them to the main latch.

COMPARATOR

The comparator compares the already stored code with the newly inputted one. The comparator- CD4063B IC- is a CMOS 4-Bit magnitude comparator. The result of the comparison is then sent to the input latch.

OUTPUT LATCH

The output latch is made up of a CD 4013B IC (CMOS dual 'D' type flip-flop). This activates the motor locking mechanism if the right code is detected. It also activates the audio alarm if three incorrect codes are entered successively into the circuit with the door still closed.

ALARM UNIT

This unit is made up of a counter – CD4017B IC an alarm oscillator- CD4060B IC and an audio alarm speaker (1 W, 8ohm). The counter counts the number of incorrect codes inputted into the circuit while the oscillator triggers the audio alarm on if successive incorrect codes are entered into the circuit.

MOTOR LOCKING MECHANISM

This unit is made up of a mechanical device responsible for the locking. It automatically locks when the right code is detected or entered into the mechanism via the output latch. This device is metallic in nature so that it will be able to withstand burglar's attack.

3.3 CIRCUIT DIAGRAM

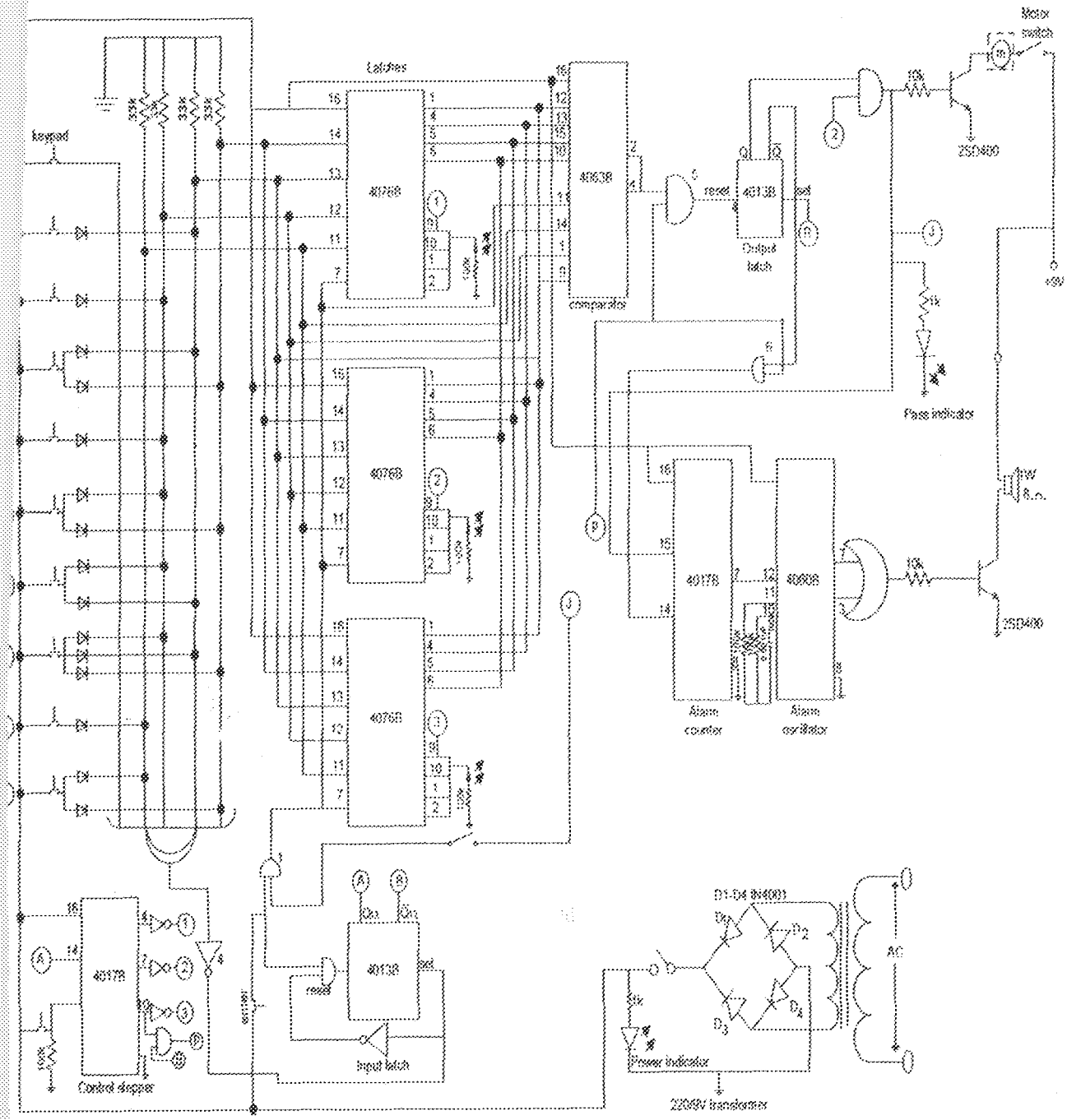


Fig. 3.0 the circuits diagram

3.4 THEORY OF OPERATION

The control stepper functions like a small processor that coordinates the whole circuit. The five input OR gate (OR 1) is designed to sum up the output from the keypad so that whenever any key is pressed, the output through the OR gate will be HIGH. There is always a HIGH logical level in every input code and the OR gate is there to detect that. This output is connected to the set input of the SR latch through an investor. (NOT 4).

The initial state of the SR latch is Q HIGH and $\overline{Q}$ LOW so that a HIGH logical level at the output of the OR gate makes the set terminal low. This makes the reset to be operational.

Moreover, to store a code in the set of latches, the numbers must be pressed down while the enter button is being pressed successively. The first number will be automatically stored in the first latch.

Terminal (A) is connected to the clock input of the control stepper so that when a number is entered into the latch, the SR input latch will be reset and Q will now be of LOW logical level while $\overline{Q}$ will be HIGH. When the number and the enter button are released, the situation becomes reversed; Q changes to HIGH and $\overline{Q}$ turns LOW. This logical transition automatically set a clock pulse into the control stepper and the second latch will be enabled i.e. ready for input while the other two will be disabled.

Furthermore, three of such procedures make the three latches full, in other words three numbers are stored in the latches. The storage is only possible whenever (5) terminal is HIGH because the terminal enables AND 1 gate which is connected to the clock of the latches. Terminal (1) will only be HIGH whenever the input or the password of the lock is correctly entered into the circuit.

The comparator compares the input code with the password. If there is a difference, the output of the comparator (pin 4 and 2) will be HIGH.

Whenever the door is locked or active, the output SR latch holds a HIGH logical at Q output and $\overline{Q}$ is LOW. This condition is necessary for the lock to be opened after imputing the correct code that match the password. Any wrong input results in changing Q from HIGH to LOW logical level because the comparator identifies the difference with a HIGH logical level at the output and this enable AND gate 5 which resets the output latch. The output (5) which is responsible for unlocking the lock now becomes LOW. The door can only be unlocked if the output SR latch i.e Q is HIGH.

The password can be altered by pressing reset and inputing a set of three numbers. These numbers serve as the new password. Also, whenever the reset button is pressed, the system will be at ground state.

For changes to be made to the password the initial code must be input correctly and then new set of numbers entered into the circuit. The circuit incorporates a mechanism for detecting an intruder. There is a section in the design that counts the number of wrong

entries into the system and it triggers on an audio alarm whenever the count is three. This circuit holds on 4017B and 4060B, the former is the alarm counter while the later is an oscillator. The oscillator requires a LOW logical level at pin 12 for proper operation or enabling mode.

Whenever the input is wrong, the AND gate 6 output becomes HIGH, this is due to the fact that terminal (P) becomes HIGH while the output of the comparator is HIGH too. This results into a sharp pulse from the output of AND gate 6 and it clocks the alarm counter. The Pin 7 of the 4017B becomes HIGH after three different pulse are directed to the lock input (Pin 15). The investor changes it to a LOW logical level. This, consequently results to the oscillation of the alarm oscillator.

The oscillator produces two different frequencies; one is LOW and the other is HIGH. The frequencies of these pins can be calculated thus;

$$F = \frac{1}{2.3 \times R_m \times C_m} \quad \text{.....Eqn. 3.0}$$

$$F_{pin}3 = \left(\frac{1}{2.3 \times 33 \times 10^{3} \times 0.001 \times 10^{-6}}\right) \times \frac{1}{2^{3}} = 1.65\text{KH}_z$$

$$F_{pin}7 = \left(\frac{1}{2.3 \times 33 \times 10^{3} \times 0.001 \times 10^{-6}}\right) \times \frac{1}{2^{7}} = 102.97\text{H}_z$$

The two frequencies are attributed to audio range. They are mixed together by an OR gate 2 and the output is fed to a 2SD400 NPN transistor for amplification so that a loud audio alarm sound can be heard. Moreover, the audio alarm can only be turned OFF by inputting the correct password.

The control stepper controls the latches through their Pin 9, 10, 1 and 2. The control stepper is active LOW because a LOW logical level is required at the points for operation.

The circuit is in cooperated with a number of LEDs (light emitting diodes). The three white LEDs indicates – successively that a number has been stored in one of the latches. After the third number has been entered, the green LED indicates whether the code has been accepted or not. If the green LED comes on, it implies the code has been accepted but if otherwise, a wrong code has been entered

There is equally a yellow LED which indicates that the circuit is ready for new inputs by being high and it does goes low if a wrong input is entered through the keypad.

3.5 COMPONENTS AND COMPONENTS DESIGN

3.5.1 RESISTORS

Resistors are electrical components used to limit the flow of electric current in a circuit. Three factors must be put into consideration before choosing a resistor. These are:

1. **THE TOLERANCE:** The exact value of any resistor cannot be guaranteed though, this is not a disadvantage because in a circuit, the value of resistors are not critical. A resistor with a stated value 100Ω and a tolerance of ± 10% could have any value between 90-100Ω.
2. POWER RATING: – This is the maximum current which can be developed in a resistor without damage occurring by healing for most of electronic circuit 0.25 – 5W rating is good enough.

3. STABILITY: - This is the ability of the resistor to keep the value with change of temperature and age.

3.5.2 CAPACITOR

Capacitors store electronic charges. It essentially consists of two conducting surfaces separated by a layer of an insulating medium called dielectric.

CHARGING

When the two ends of a capacitor are connected to a battery, the positive end of the battery attracts electrons from one plate end of the capacitor and the negative end of the battery repels electrons to the other plate. Positive charges (deficit of electron) build up around one plate end of the capacitor and negative charges (excess of electrons) build around the other plate of the capacitor.

During the period of charging, there is a flow of electron round the circuit between the two plates of the capacitor. Full charging is achieved when the potential difference (PD) between the two plates is equal to the E.M.F. of the battery. This process is gradual and it takes time.

Apart from its value and tolerance, two factors are to be considered when choosing a capacitor. These are:

1. The working voltage:- This is the maximum voltage the capacitor can withstand before the dielectric breaks down (it is always indicated) and
2. The leakage, though it should be small.

3.5.3 BATTERY

An electric battery consists of a number of electro-chemical cells, connected either in series or parallel. A cell, which is a basis unit of a battery, may be defined as a power generating device, which is capable of converting stored chemical energy into electrical energy.

Each cell has positive and negative plates, separators and electrolyte, all contained in one of the many compartments of a battery container.

When the cell is operated, the negative electrode oxidizes and the positive electrode becomes reduced. The negative electrode yield electrons to an external circuit and the positive electrode accept electrons from this circuit.

There are two types of electric cell:-

a. **Primary cells:** - This is also called non-rechargeable cell. It is called so because the stored energy is inherently present in the electrolyte. E.g Leclanche cell, Zinc-chlorine cell, alkaline manganese cell etc.

b. **Secondary cells:** - These types of cells are rechargeable. The energy in this cell is induced into the electrolyte by applying an external source examples include; lead-acid cell, nickel-iron cell, silver zinc cell etc.

CARE AND OPERATION OF BATTERIES

There are three major ways in which batteries can be effectively taken care of. These are;

a Water should be added from time to time to keep the electrolyte always in optimum level.

b. Do not add electrolyte except to replace the lost ones and,

c. Always keep the battery dry and clean.

3.5.4 DIODES

A diode is a two-terminal semiconductor device which consists of a P-N junction formed from either silicon or a Germanium crystal. Its circuit symbol is shown below in fig. 3.1

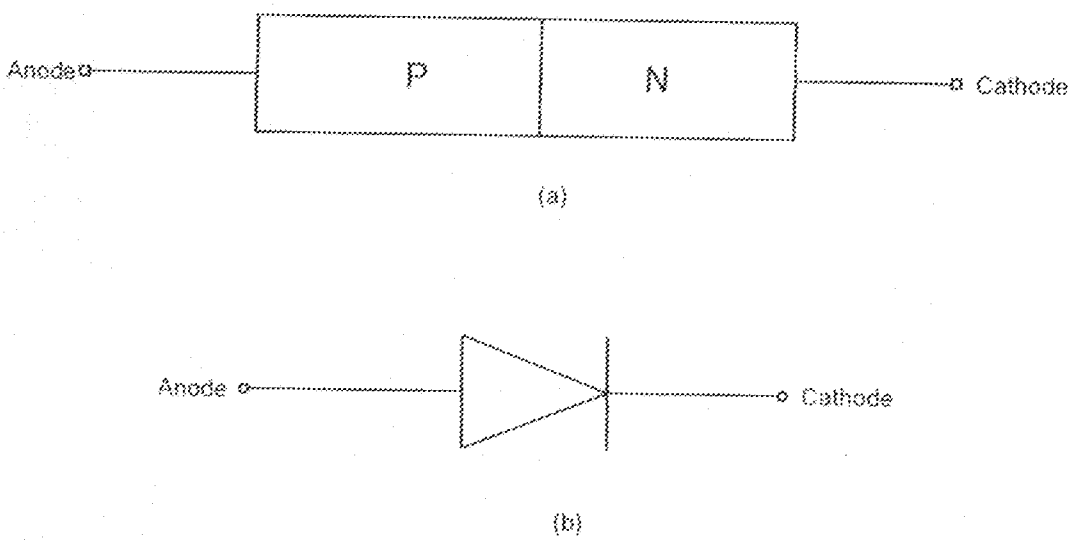


Fig. 3.2 (a) A diode symbol (b) The circuit symbol of a diode.

The P-and N-type regions are referred to as anode and cathode respectively. In Fig. 3.2 (b), the arrow head indicates the conventional direction of current flow when forward biased.

A P-N junction diode is a one way device offering low resistance when forward biased and behaving low resistance when forward biased and behaving almost as an insulator when reverse – biased They are mostly used as rectifiers and switches in industrial applications. We have different types of diodes depending on their

applications; small signal diode, Gunn diode, photo diode, light emitting diode, schottky diode e.t.c.

APPLICATIONS OF DIODES

i. Are used as logic circuits

ii. As zener diodes – in voltage stabilizing circuits

iii. As power rectifier diodes. Conversion of a c (alternating current) into d.c (direct current) for d.c. power supplies in electronic circuits 6v) As varactor diodes – for use in voltage controlled tuning circuits as may be found in radio and T.V receivers. For this purpose, the diode is deliberately made to have a certain range of junction capacitance.

HIGH – SPEED DIODE (IN 914)

The IN914 diode is of two types; the IN914A and IN914B. These are high speed switching diodes fabricated in planar technology and encapsulated in a hermetically sealed lead glass. Any of the two can be used for this project

FEATURES

i. High switching speed {maximum of 4ns}

ii. Continuous reverse voltage {maximum of 75v}

iii. Repetitive peak forward current {maximum of 225m A}

iv. Repetitive peak reverse voltage {maximum of 100V}

v. Hermetically sealed leaded glass SOD 27 (DO-35) package.

APPLICATIONS

- High speed switching

LIMITING VALUES

The limiting values stated are in accordance with the absolute maximum rating system (IEC 65 134)

Table 3.0 Limiting values of high speed diode

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
VRRM	Repetitive peak reverse voltage		-	100	V
If	Continous forward voltage		-	75	mA
VR	Continous reverse voltage			75	V
IFRm	Repetitive peak forward current		-	225	MA
Ifsm	Non-repetitive forward current	Square wave, T; 25^{0}C t-iNS, times	-	4.1 & 0.5	A
Pt.t	Total power dissipation	Temp = 25^{0}C	-	250	MW
Tgtg	Storage temperature		-65	+200	^{0}C
Tj	Junction temperature		-	175	^{0}C

Symbol	Parameter	Conditions	Value	Unit
Rth-j-tp	Thermal resistance to lie point	Lead length 10mm	240	K/W
Rth-j-n	Thermal resistance from function to ambient	Lead length 10mm	500	K/W

3.5.5 25C945 NPN TRANSISTOR

The 25C945 is a semi conductor three layer bipolar junction transistor (BJT) with enutter (E), base (B) and collector regions. The term bipolar indicates that current flow consists of a movement of both positive and negative charges i.e holes and electrons. See figure 3.2 below.

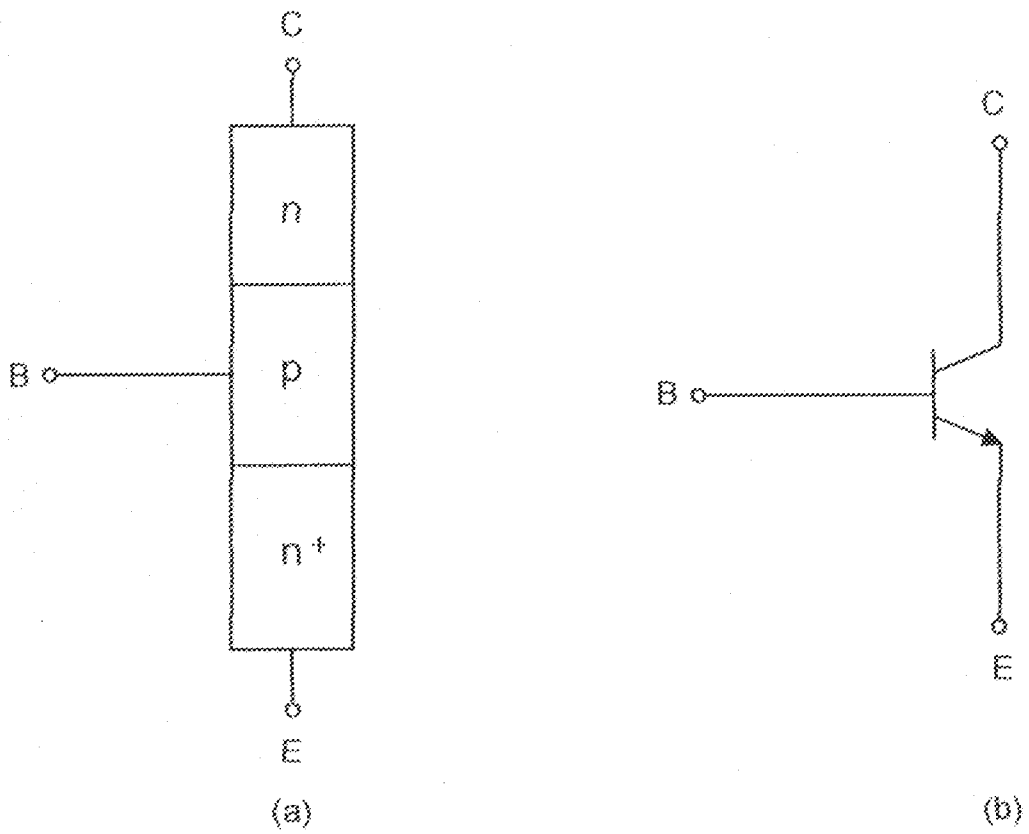


Fig. 3.3 (a) Simplified structure of an n-p-n transistor (b) circuit symbol of n-p-n transistor

As shown in the figures above, the base and the emitter form the p-n junction that conducts like a diode in the direction indicated by the arrow head.

For a normal transistor operation, the base emitter acts as source of mobile carrier which enter the base region. These carries are electrons.

TRANSISTOR CURRENTS

The three primary currents which flow in a properly based transistor are I_B, I_E and I_C. See figure 3.3 below

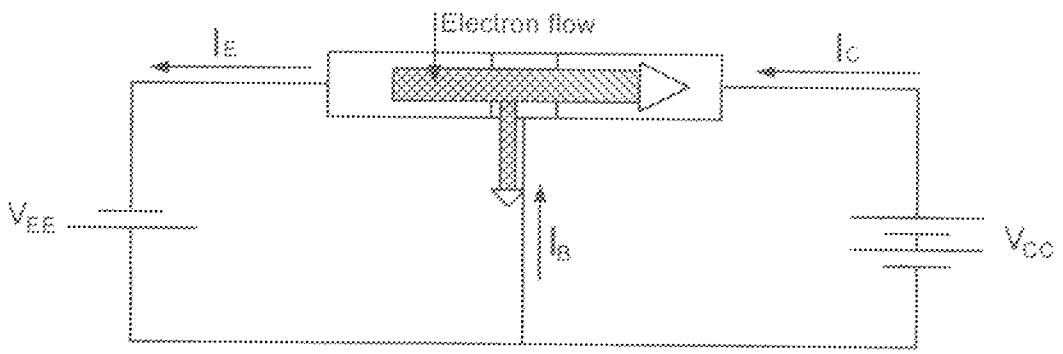


Fig. 3.3 Electron flow in an n-p-n transistor

From figure 3.3 above, we can see that

$I_B = I_E - I_C$

This connotes that about 1-2% of I_E goes to supply the base current and the remaining (about 98-99%) part of the current goes to supply collector current. I_E (emitter current) flows into the transistor and I_B (base current) and Ic (collector current) flows out

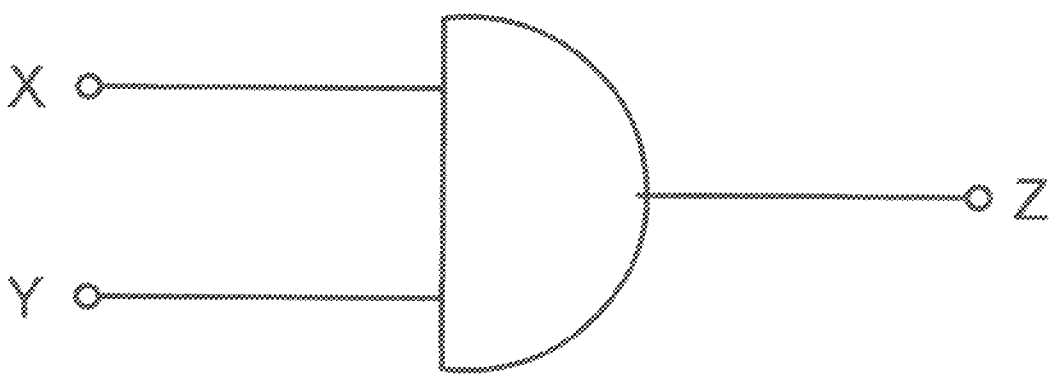
of it. The ratio of the collector current to the emitter current is defined as the forward current gain,

$$\alpha = \frac{I_C}{I_E}$$

α is typically in the range of 0.95 to 0.99.

3.5.6 THE AND GATE

The AND logic gate is sometimes called the "all or nothing gate". The electronic (or logic) symbol for a 2 input AND gate is shown below fig. 3.4



$$X \cdot Y = Z$$

Fig. 3.4 The electronic symbol of an AND gate.

LOGIC OPERATION

- The AND gate gives an output only when all inputs (X and Y) are enabled
- The AND logic gate has one output and two input lines.

Table 3.1 truth table

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

THE INVETER (NOT CIRCUIT)

The inverter (or not circuit) is a logic circuit that has only one input and output that is not the same as the input. The logic symbol for the inverter is shown in the figure below.

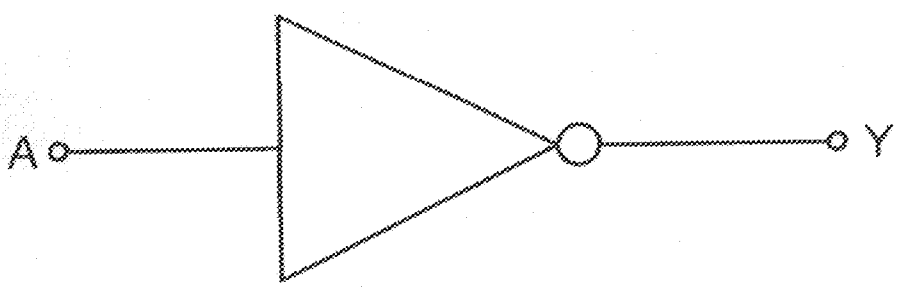


Fig. 3.6 Logic symbol of an inverter

If we were to put-in a logic at input A in the figure 3.6 above, we would get out the opposite or logic 0 at output Y.

i.e. $Y = \overline{A}$

Where $\overline{A}$ denotes the complement of A

Table 3.2 Truth table for an inverter.

INPUT A		OUTPUT Y	
Voltages	Binary	Voltage	Binary
LOW	0	HIGH	1
HIGH	1	LOW	0

3.5.8 TRANSFORMER

A transformer is a static piece of an electrical device through which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It has the ability to raise or lower the voltage in circuit depending on the type in use. In this project, the type used is the step down (220/9V) type of transformer. The basis of operation is mutual induction between two circuits linked by a common magnetic flux. It consists of two inductive costs which are electrically separated but magnetically linked through a path of low reluctance. The principle of operation is guided by some basic laws; Faraday's laws of Electromagnetic induction e = nd1/dt.

The first coil, in which electric energy is fed from the a.c. (alternating current) supply mains, is called primary winding and the other from which energy is drawn out, is called secondary winding.

VOLTAGE TRANSFORMATION RATIO

The ratio, $X = \frac{E_2}{E_1} = \frac{N_2}{N_1}$

Where,

E_2 = voltage drop in the secondary winding (coil)

E_1 = voltage drop in the primary coil (winding)

N_2 = Number of turns of the secondary coil

N_1 = November of turns of the primary coil

(i). If $N_2 > N1$ i.e. $K > 1$ then the transformer is called a step – up transformer.

(ii) If N_2 N_1 i.e. $K < 1$ then the transformer is called a step - down transformer.

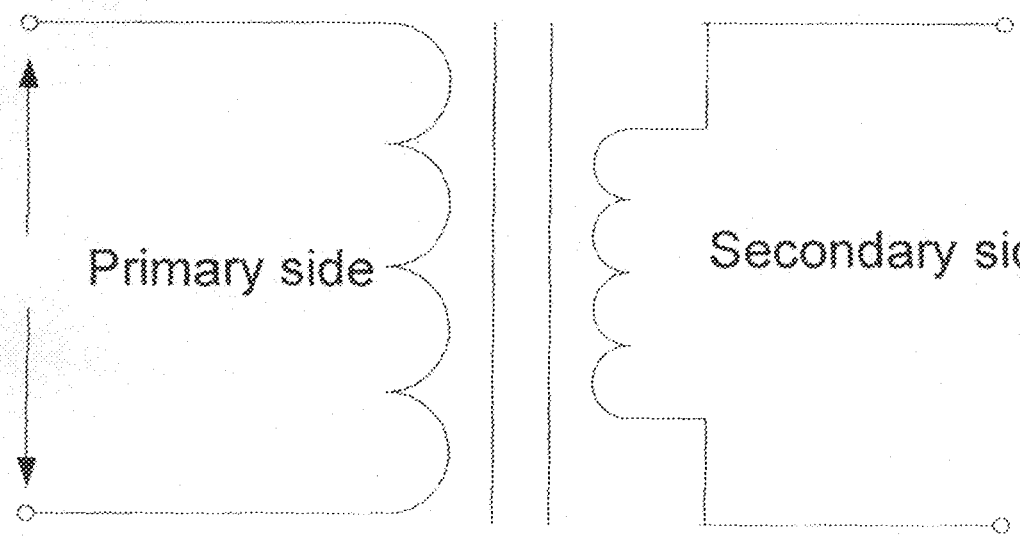


Fig. 3.7 The circuit symbol of a step-down transformer

3.5.9 FULL-WAVE BRIDGE RECTIFIER

The full-wave bridge rectifier is the most frequently used circuit for d.c (direct current) supplies. This type of rectifier is often inco-operated with a transformer in a circuit because of its function i.e. turning an alternating current into direct current. The full ware bridge rectifier has four diodes as shown in figure 3.7 (a) below.

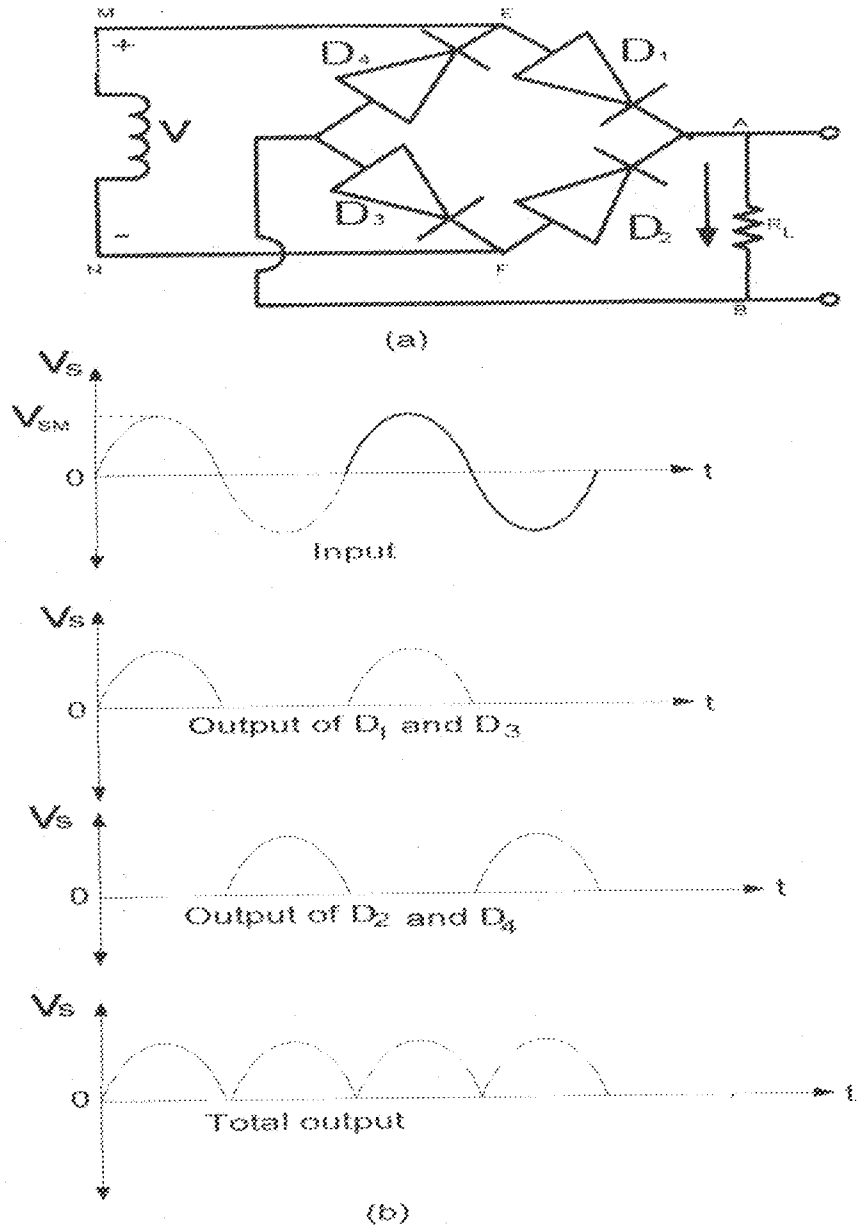


Fig. 3.8 A full wave bridge rectifier

PRINCIPLE OF OPERATION

During the positive input half-cycle, terminal M of the secondary is positive and N is negative as shown in figure 3.9 (a). Diodes D1 and D3 conduct whereas D2 and D4 are reversed biased i.e. OFF. Therefore, current flows in the path MEABCFN producing a drop across RL.

So also, in the negative input half cycle, D2 and D4 conduct whereas D1 and D3 are OFF. The circuit current flows along NFABCEM. In both input half cycle, we discover that current flows through the load resistance RL in the same direction – AB. Figure 3.9 (b) shows the input signal and the corresponding output signals in both cases.

3.6.0 INTEGRATED CIRCUITS (ICs)

Integrated circuits are the most widely used electronic component today. They are made up of a combination of discrete components such as resistors, capacitors with semi conductor "clips" in which transistors and diodes are fabricated.

There are two groups of integrated circuits; hybrid and the monolithic type.

Hybrid integrated circuits:- These are constructed by the use of printing circuit board instead of wire to effect connection between the various passive and active components.

Monolithic integrated circuit:- The entire fabrication of this type is done within a single block of silicon crystal.

The most common type of integrated circuit package is the dual-in-line type, which consist of a plastic bar in which the integrated circuit is embedded. The bar is often almost 20mm long about 5mm wide and barely 2.5mm thick, with the leads protruding out of the two sides.

CD 4017BC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

GENERAL DESCRIPTION

The CD 4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit. This counter is cleared to zero count by a logical "1" on their reset line.

This counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "O" state.

The configuration of the CD 4017BC permits medium speed operation and assures a hazard free counting Sequences. The 10 decoded outputs are normally in the logical "O" state and 80 to logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10 input cycles and is used as a ripple carry signal to any succeeding stages.

FEATURES

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45V_{DD}$
- Low power {10mW type}
- Fully static operation
- Medium speed operation {5mHz (type) with 10V V_{DD}}
- Low power TTL compatibility [fan out of driving 74L or 1 driving 74 LS]

APPLICATIONS

- Alarm systems
- Industrial electronics
- Instrumentation
- Automotive

CONNECTION DIAGRAM

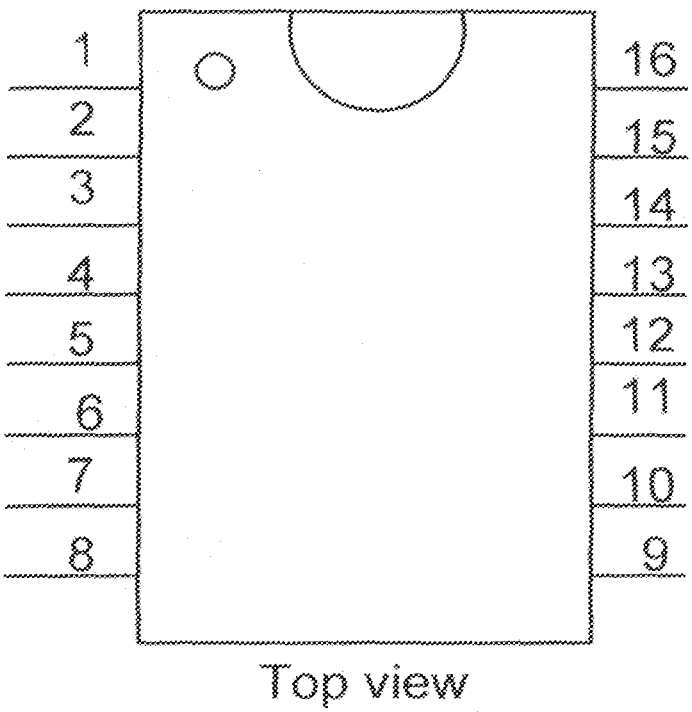


Fig. 3.8 Connection diagram of a CD 4017BC IC.

Legend:

1	=	Decoded output	"5"
2	=	Decoded output	"1"
3	=	Decoded output	"0"
4	=	Decoded output	"2"
5	=	Decoded output	"6"
6	=	Decoded output	"7"
7	=	Decoded output	"3"
8	=	VSS	
9	=	Decoded output	"8"
10	=	Decoded output	"4"
11	=	Decoded output	"9"

12 = Carry out

13 = clock enable

14 = Clock

15 = Reset

16 = V_{DD}

CD4063B CMOS 4-BIT MAGNITUDE COMPARATOR

The CD 4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of 4-bit words. The logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or greater than" a second 4 bit word.

The CD 4063B has eight comparing inputs (A3, B3, through AO, BO), three outputs (A< B, A=B, A> B) and three cascading inputs (A<B, A = B, A>B) that permit system designers to expand the comparator function to 8, 12, 16----4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A<B) = low, (A = B) = high, (A>B0 = low

For words longer than 4bits, CD 4063B devices may be cascaded y connecting the outputs of the less significant comparator to the corresponding cascading inputs of the more significant comparator. Cascading inputs (A<B, A = B, and A>B) on the least significant comparator are connected to a LOW, a high and a low level, respectively.

The CD 4063B types are supplied in 16-lead hermetic dual-in-line plastic package (E suffix), and in chip form (H suffix).

APPLICATIONS

- Serve motor control
- Process controllers

FUNCTIONAL DIAGRAM

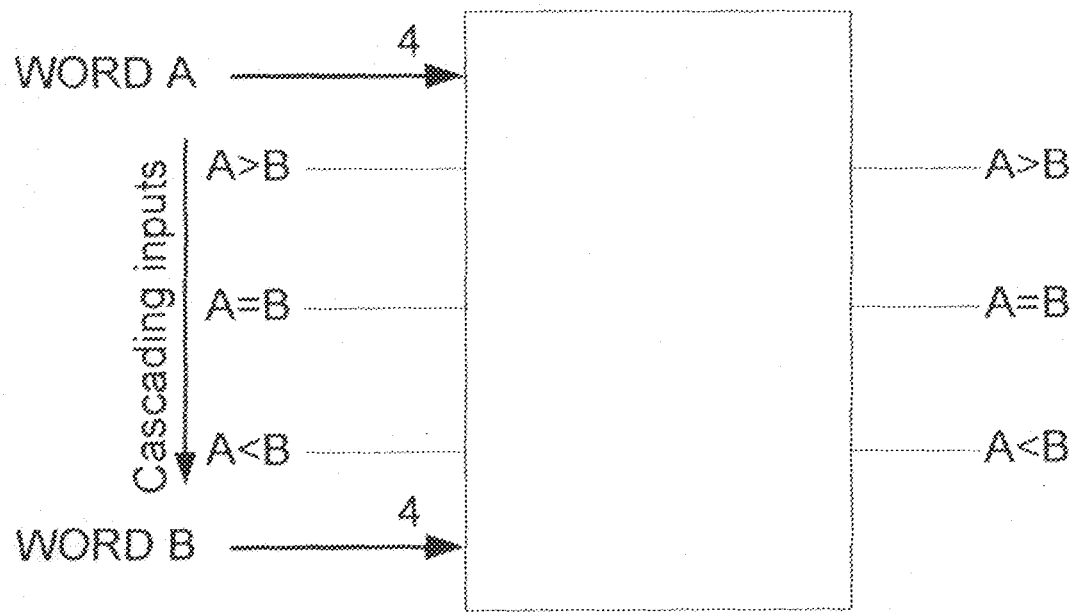


Fig 3.9 Functional diagram of CD 4063B

TERMINAL ASSIGNMENT

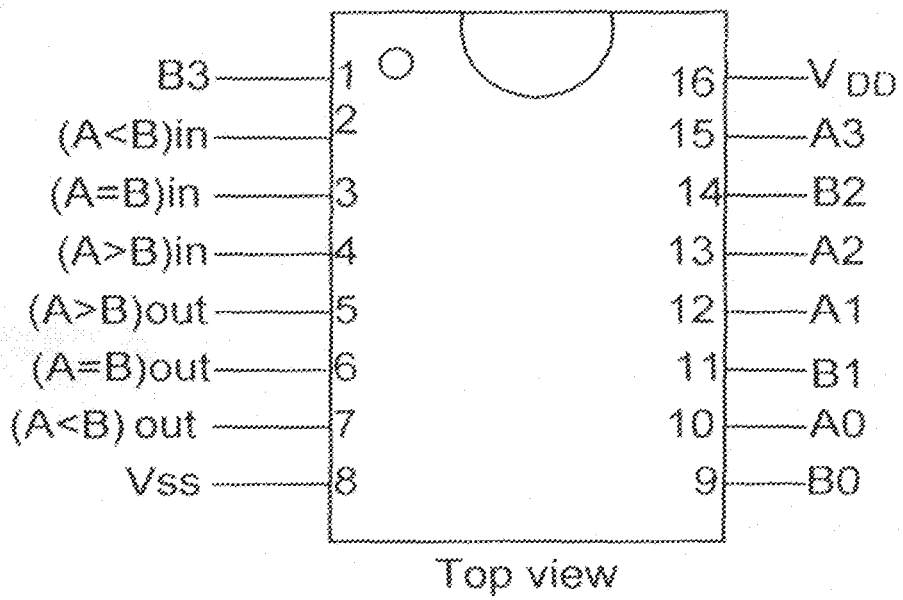


Fig. 3.10 Terminal assignment of CD4063B IC.

MC14060B 14-BIT BINARY COUNTER AND OSCILLATOR

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator bugger. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which placed all outputs into the zero state and disables the oscillator. A negative transition on clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

Table 3.3 Truth table of MC14060B

CLOCK	RESET	OUTPUT STATE
⌐¯	L	No change
¯⌐	L	Advance to next stage
Z	H	All outputs are

PIN ASSIGNMENT

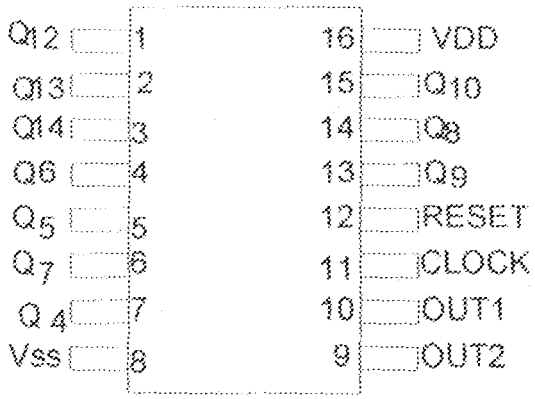


Fig.3.11 Pin assignment of MC14060B

CD4013B CMOS DUAL 'D' – TYPE FLIP – FLOP

The CD4013B consists of two identical, independent data-type flip flips. Each flip flop has independent data, set, reset and clock inputs and Q and Q outputs. There devices can be used for shift register applications and by connecting Q output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive going transition of the clock pulse, setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

FUNCTIONAL DIAGRAM

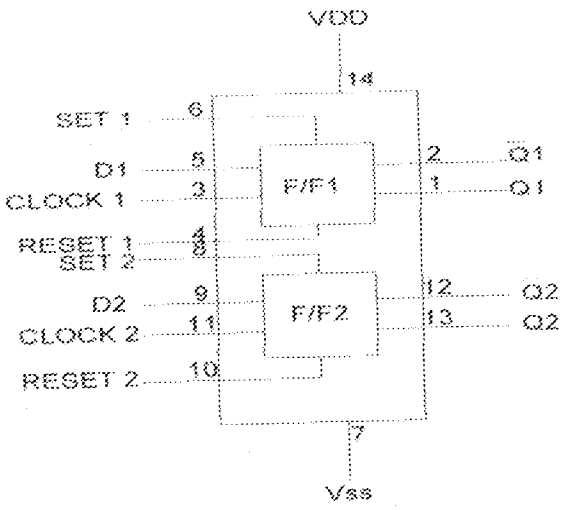


Fig.3.12 Functional diagram of CD4013B

TERMINAL ASSIGNMENT

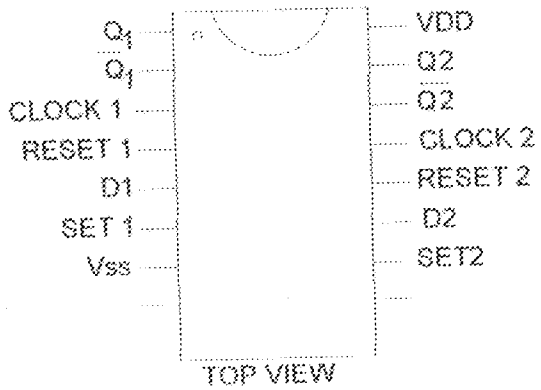


Fig.3.13 Terminal assignment of CD4013

Table 3.4 truth table of CD 4013B

CL	D	R	S	Q	Q
⌐	0	0	0	0	1
⌐	1	0	0	1	0
¬	X	0	0	Q	Q
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

LOGIC 0 = LOW,

LOGIC 1 = HIGH

X = DON'T CARE

APPLICATIONS

- Registers
- Counters and
- Control circuits

CD 4076B CMOS 4-BIT D-TYPE REGISTERS

The CD 4076B type is a four-bit registers consisting of D-type flip flops that feature three state outputs. Data disable inputs are provided to control the entry of data into the flip flops. When both data disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output disable inputs are both low, the normal logic states of the four outputs are available to the load.

The outputs are disabled independently of the clock by a high logic level at either. Output disables input, and present high impedance.

TERMINAL ASSIGNMENT

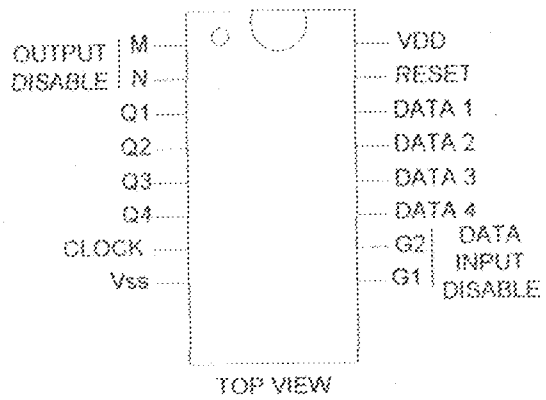


Fig. 3.14 Terminal assignment of CD 4076B

CHAPTER FOUR

4.0 CONSTRUCTION, TESTING AND RESULT

4.1 CONSTRUCTIONS

The construction involves three segments:

1. THE KEY BOARD

The keyboard's pad was made from an office calculator button pad. The switches were placed on the Calculator's buttonholes and with the aid of gum; the numbers were gummed into the switches.

2. THE DOOR

The door being the model was made from plywood due to its high weight and ease of modification. A small hole was drilled on the door where the keyboard pad is bolted through.

3. THE CIRCUIT (CONTROL BOARD)

Taking a look at the circuit diagram, a good layout was properly mapped – out to ensure component clearance, spacing and proximity. The soldering of the components was made and were properly aligned on the design. To avoid short circuits, unused or extended copper strips of wire were scrapped. The assembly of the components was now done as described by the circuit diagram

4.2 TESTING

The procedure for the testing is as follows:

1. When not connected to the power supply means.
2. When connected to the power supply and a wrong code entered and
3. When connected to the power supply and the right code entered.

4.3 RESULT

1 The door is always locked when not connected to the power source

2. When a wrong code was entered, as at the time the power supply was initiated, the door remained locked and at the exhaustion of three wrong codes, the alarm stopped after the right code was entered.

3. The door turned unlocked when the right code was entered.

4.4 DISCUSSION OF RESULT

The electronic configuration is quite suitable for the locking application. The keypad was able to input the specific binary codes in to the latches so that an input codes is retained in the latches as long as the power supply circuit is active. Equally, the audio alarm works with three wrong input coeds.

CHAPTER FIVE

5.0 CONCLUSION AND RECOMMENDATIONS

5.1 CONCLUSION

The design and construction of a digital door lock with an audio alarm was successfully carried out. Based on the scope of this project, the set objectives of the design as desired such as the reliability, user friendliness, systems accessibility and most importantly security have been achieved.

5.2 RECOMMENDATION S

1. I hereby recommend that this design be used in houses, bank, industries and farms where are an automatic stand – by generator as the code could be lost if there is power failure.
2. For domestic and office installation, a stand-by switch could be made and positioned in and their safe room incase of system failure.

REFERENCES

[1.] Microsoft Encarta Dictionary/ encyclopedia (200) Microsoft Corporation

[2.] B. L Theraja and A.K. Theraja, Text Book of Electrical Technology, S Chand and company, Ram Nagar, New Delhi-India, 2002, pp 919 –921,pp 1651 – 1660, pp 1742 – 1745,pp 2034 – 2036.

[3.] Roger L. Tohkeim, Digital electronics, principles and Applications, 5th Edition,1999,pp.33, pp 154.

[4.] National semiconductor Corporation, on line data sheets http //www.national.com