DESIGN AND CONSTRUCTION OF ELECTRONIC DIGITAL CLOCK

By

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A project submitted to the Department of Electrical and Computer Engineering, School of Engineering and Engineering Technology,
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In Partial Fulfilment of the requirement for the award of Bachelor of Engineering (B.Eng) Degree in Electrical and Computer Engineering.

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DECLARATION

I here by declare that this project was wholly designed & constructed by me under the supervision of Dr. Y.A. ADEDIRAN of electrical/electronics department,
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DATE

CERTIFICATION

I certify that this project was carried out by Abaniwo T.E. Peter under my supervision of my supervisor Dr. Y. A Adediran of Electrical and Computer Engineering Department Federal University of Technology, Minna, Niger State.

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External Examiner's — Signature/Date

DEDICATION

Dedicated to the Lord God Almighty for seeing me through and making it a great success. I am also dedicating this project to my:

Dad: Late Mr. J.A. Abaniwo

Mum: Mrs F.T. Abaniwo

Brother: Engr. Godwin Abaniwo

Dr. Sanuel Abaniwo

Mr. Isaiah Abaniwo

Mr. Femi Adeyi

Sisters:- Mrs. Grace Abaniwo

Mrs. Gloria Abaniwo

Mrs Comfort Abaniwo

Mrs. Blessing Kika

And my beloved wife to be: Miss Twaki S.L. Lydia.

ACKNOWLEDGEMENT

Appreciations to my co-project partner Mr. Idris Abdulrahim for his consistency and support.

My appreciation goes to Engr. Adediran H.O.D. of Electrical/Electronics /Computer Department, Federal University of Technology, Minna, Niger State fo approving this project for me.

Also Mr Sheun Wale who also help in the designing of the project and Mr. Rumala for he's indirect moral support.

Finally my appreciation to my family for their financial support in sponsoring my project.

T.E.A. ABANIWO

ABSTRACT

The importance of the right thing at the right time is vital to human existence and therefore, the issue of telling the time of the day becomes veyr necessary and important.

The earliest time keeping divice which indicate the time of the day by the position of the shadow of some object on which the sun ray fall's is no longer in us today, but a machine in which a device that performs regular movements in equal intervals of time is linked to a counting mechanism that records the number is now in use, therefore, in order to realize a better telling time of the day this project, DIGITAL CLOCK, are made on this principle.

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CHAPTER ONE

1.0 INTRODUCTION

There are three types of telling time of the day: Clocks, watches and sundials.

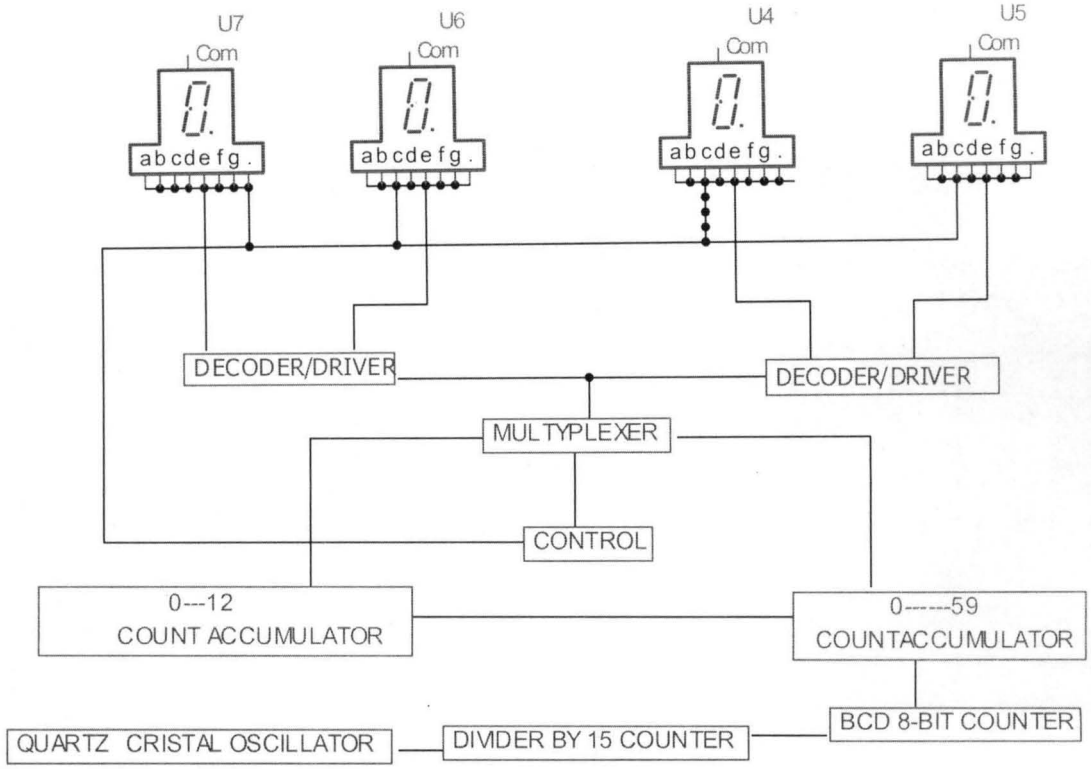
Sundials or shadow clocks, earliest of the three types of time keeping devices, indicates the time of the day by the position of the shadow of some object on which the sun's ray fall. As the day progresses, the sun moves across the sky, causing the shadow of the object to move.

Clocks are devices used to record or indicate the time of the day. Clocks are machines in which a device that performs regular movements in equal interval of time is linked to a counting mechanism that records the number of movements. All clocks of what ever form are made on this principle.

A watch is a portable time piece, the general horology, used to describe the art of measuring time or making clocks is derived from the Greek word hora ("time") and Logos ("telling").The telling of the time of the day is needful in most cases and as such should be mounted-up in strategies places such as school libraries, offices to mention but few.

The design circuitory consist of mainly six basic section,This sections are: Display section, Decoder/Driver section, buttering section, count accumulator section, control section, oscillation/ divider section.

Fig. 1.0.0 Explain the basic flow of the design of this project which are in block diagram.



In order to construct an accurate digital clock, a very closely controlled frequently is required. For battery operated digital clocks, the basic frequency is normally obtained firm a quartz crystal oscillator.

Digital clocks operated from the a.c. power line can use the 50Hz power as the basic clock frequently. But in either case the basic frequency has to be divided down to a frequency of 1Hz or 1 purse per second (1pps).

The Digital clock uses counters as frequency dividers. In fig. 1.0.0 in the lower section, the counter are also used as count accumulator's job is to count the input pulses and serve as a temporary memory while passing the current time through the decoders into the time displays the clock diagram in figure 1.0.0 represents a 4 - digit, 24 hours digital clocks.

The 32.786 KHz signal is sent through a shaping circuit (pulse generator) to produce square pulses a the rate of 15pps. This 15pps wave from is fed into a divider by 15 counter which is used to divide the 15pps down to 1pps. The 1pps signals is fed into the second section, count accumulator, which is used to count seconds from 0 through 59 . (The count accumulator of the digital clock are usually or actually two counters. A decade counter and MOD 6/3 counters. The decade counter advances one count per second. After 9 seconds. The decade counter recycles to 0, which triggers the MOD - 6 counter and causes it to advance one count. This continues for 59 seconds when the MOD-6 counter is at the 101(5) count and the decade counter is at 1001 (9); so the counter reads 59 seconds the next pulse recycles the decade counter to 0, which in turn recycles the MOD - 6 counter to 0. The output of MOD-6 counter in the second section has a frequency of 1 pulse per minutes (MOD -6 recycles every 60 seconds). This signal is fed to the minutes Section which counts and displays minutes from 0 through 59

the minutes section is identical to the seconds section and operates in the same manner.

The decoder/driver serve to decode the BCD to seven segment display output the output of the MOD - 6 counter in the minute section has a frequency of 1 pulse per hours (the MOD - 6 recycles every 60 minutes). This signal is fed to the hours section.

LITERATURE REVIEW

1.1 TIME KEEPERS EXISTING CLOCKS

SHADOW CLOCKS OR SUNDIALS

The first device for indicating the time of the day was probably the gnomon. It consisted of a vertical stick or pillar; the length of the shadow that it cast gave an indication of the time of the day.

SAND GLASSES

Along with the development of shadow clocks, sand glasses which measured time by means of sand running from one glass vessels to another through a narrow passage, were introduced.

The sand glass was pivoted in the middle (centre) so that it could be swindled to start the sand pouring downward there exist a leather case with four sand glasses fitted so that all are visible and made to run for a quarter, halt, three quarters and one full hour.

CANDLE AND LAMPS CLOCKS

These devices looked much live a candle stick with a glass bottle at their top and a horizontal projection at the side to hold the wick oil would drain from the glass bottle into a small tube into which a small wick was inserted; as the oil burns away, the level of oil in the glass reservoir would indicate the hour.

WATER CLOCKS

Simple water clocks were used to record time at night or when the sun was obscured these bucket shaped vessels from which water was allowed to escape by a small hole at the same hole at the base uniform scale of time were marked on the inside. By the end of the first hour, water filled to the brin would have fallen to the first mark of the scale the difficulty of regulating the pressure of outflow of this clocks (water) and the variations in viscosity of water, according to the temperature, rendered them in accurate.

MECHANICAL AND ELECTRICAL CLOCKS

The mechanisms of a modern mechanical clock the wheelwork or train of a clock is the series of moving parts (gear) that transmits motion from a weight or spring to the minute and hour hands. The wheels and pinions must be made accurately and the tooth form designed so that the transference of power takes place as steadily as possible.

Electrical clocks in a master clock system, electricity is used to give direct impulse to the pendulum that in turn causes the clock's gear train to move, or to lift a lever after it has imparted an impulse to the pendulum.

THE WATCH

The system mechanism of a modern watch performance depends on the uniformity of the period of oscillation of the balance the balance takes the form of a wheel with a heavy rim, while the spring couple to it provides the restoring torque. The balance possesses inertia dependent on its mass and configuration the spring should ideally provide a restoring force directly proportional to the displacement from its unstressed or zero position.

DIGITAL CLOCK

Digital clocks operated from the a.c. power supply can use the 50Kz frequency as the basis clock frequency, but the basic frequency has to be divided down to a frequency of 1HZ. The digital clock uses counters as a frequency divider and also use it as count accumulator which count the input pulses and serve as a temporary memory while passing the current time through the decoder into the time displays.

Of all the devices for indicating the time of the day, digital clock is the most accurate of them and a such, chosen for the design and construction using counters.

CHAPTER TWO

DESIGN OF COMPONENTS

2.0 INTRODUCTION

The block representation of a digital clock is as shown in figure 1.0.0. Each block represents a stage in the whole circuit arrangement. There are six stages. The power supply, the time (pulse generator), the divider by 15 counter, the count accumulator, drivers and display state.

The states are arranged in such as way that the output of one stage serves as the input to the other stages. This chapter covers all the design specification of each stage.

2.1 THE POWER SUPPLY

INTRODUCTION

There are two (2) modes of power supply to the digital clock which are (a) Direct current power supply by using batteries (b) Direct current power supply by rectifying an input A - C voltage.

However through both of this modes have their advantages and disadvantages which are stated in the table 2.1 a & b given below:

Advantages of An A - C	Disadvantages of an A - C
- It is very effective under consistent supply of energy and also under stable condition	- Irregular power supply in Nigeria - Supply of over voltages in faulty situations which can destroy the clock - Low voltage generation under faulty conditions - It is more expensive etc.

Table 2.1 a

Advantages of An A - C	Disadvantages of an A - C
- It is very cheap - It is very easy to maintain - It is stable - It makes the devices small (more portable) - It makes the devices lighter etc.	When there is low power supply another clock will be required for resting,

Table 2.1b

In proper consideration of both advantages and disadvantages I decided to use the D.C. power supply (by using the battery to supply the 9u required).

However for the purpose of those that might still want to use the a.c. supply for driving their clocks an explicit explanation is given below.

For an alternating input voltage there are, in general, three basic components of a de supply these are shown in the block diagram of figure 2.1.0.

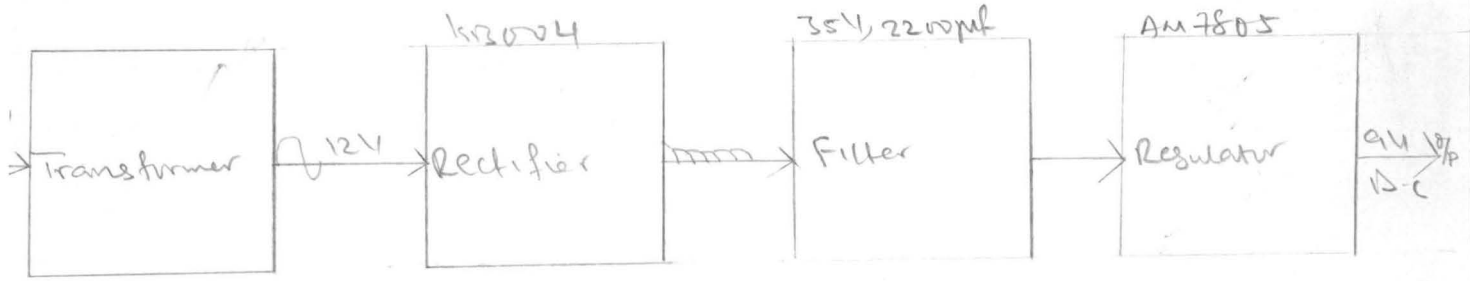


FIGURE: 2.1.0: Basic component of a power supply.

The rectifier converts the a-c input into pulsating wave form with both a - c and d.c components. In certain applications such as battery charging, this output may be adequate, but for the purpose of the digital clock, filtering to remove the a - c components. For proper operation of digital clock, it is usually essential to have a well regulated supplies.

RECTIFICATION

A number of different circuits exist that are capable of converting an a - c supply into pulsating d.c current and they may be broadly divided into one of two classes, half-wave rectifiers and full wave rectifiers.

HALF WAVE RECTIFICATION:- In its simplest form, HALF WAVE RECTIFICATION consist merely in the connection of a diode in series with the a.c supply and the load. The disadvantage of this simple rectifying circuit is very clear; the load voltage, although unidirectional, various considerably and is indeed zero for half the time such as wave is only suitable for simple applications, such as battery charging, since the variations will appear as noise at the out put of any equipment fed by the supply.

FULL WAVE RECTIFICATION: With full wave rectification of an a.c source, both half cycles of the input wave form are utilized and alternate half cycles are invested to give a unidirectional load current the disadvantage of the circuit at the need for a centre tapped transformer and for the (25 two diodes required.

An alternative method of full wave rectification is the use of a bride network which is chosen for this project because it requires no centre - tapped transformer which is difficult to come by.

BRIDGE RECTIFICATION:- Circuit requires four diodes instead of two but could be replace with a single bridge rectifier, kis po4 which is chosen the circuit of a full-wave bridge rectifier is shown in figure 2.1 1a.

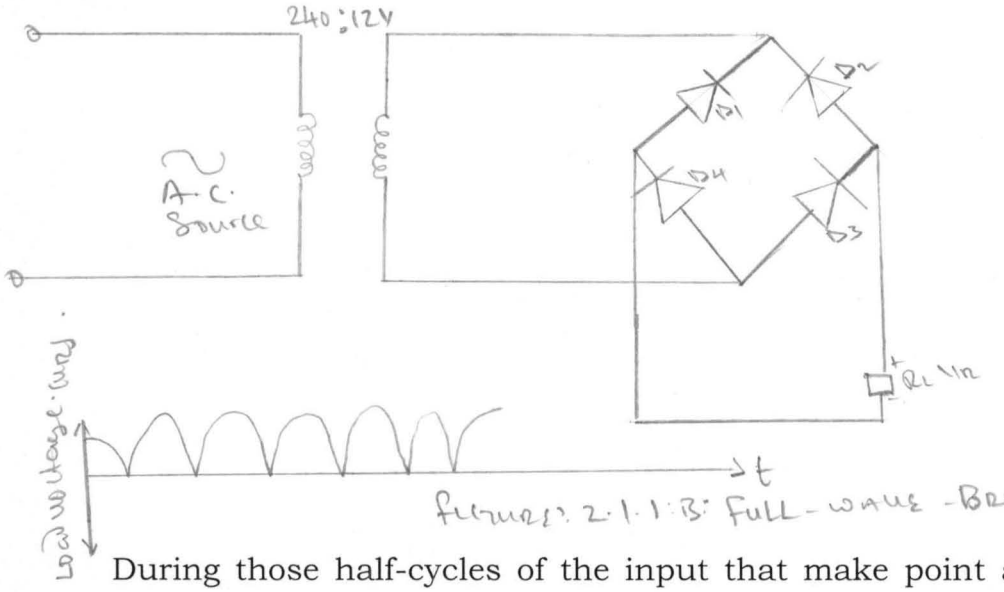


figure 2.1.1.B: FULL-WAVE BRIDGE RECTIFIER.

During those half-cycles of the input that make point a positive with respect to point b, diodes D2 and D4 are conducting; current therefore flows from point A is negative relative to point B, D1 and D3 are conducting and D2 and D4 are non conductives; current then flows from

point B to point A via D3, the load RL and D1. Both currents pass through the load in the same directions and so a fluctuating unidirectional voltage is developed across the load having the wave form of figure 2.1.1b.

FILTER CIRCUITS

The a.c ripple in the output of a rectifier is smoothed out by filter circuit. An elementary widely used type is the capacity input filter shown in the bride circuit of figure 2.1.2a the capacity makes the output wave form quite different from that of the full -wave rectifier with reference to figure 2.1.2 diodes D2 and D4 conducts from time t1 to t2, charging the capacitory c to the peak value of the voltage across the transformer secondary. At t2 the voltage at point A of the circuit has dropped below v. and these diodes turn off. From t2 to t3 all diodes are of current to the load is supplied by the energy stored in c, which slowly discharged. At t3, the voltage at B has risen to a sufficiently high values to turn on diode D3 and D1. A current pulse charges c back to the peak value from t4 tots the diodes are off and the cycle starts again at t5 the value of is made large in this project so as to reduce the ripple voltage to a low levels,

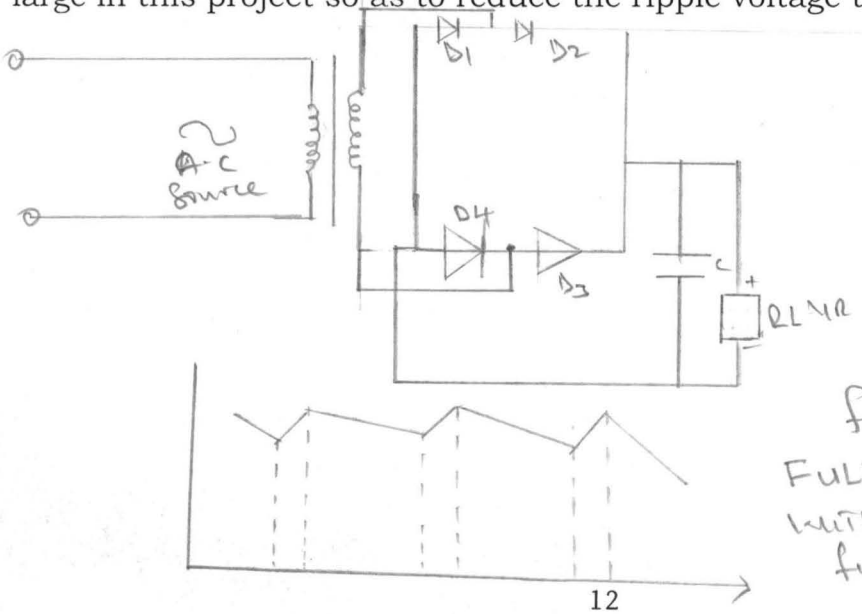


FIGURE:- 2.1.2B
FULL-WAVE RECTIFICATION WITH CAPACITOR - INPUT FILTER.

VOLTAGE REGULATIONS

Line voltages at the input of a power supply often fluctuate by as much as 10 to 20%, causing the output voltage, of the filter to vary. Current drawn by the power supply load may have a wide range of values. These effects tend to change the output voltage. A regulator is normally connected between the filter and the load, designed to maintain a nearly constant output voltage for anticipated variations in the input voltage and the temperature.

Digital and analyze integrated circuits typically require voltage supplies with a regulation of 1% or less, but for the purpose of this project t9v regulations is used.

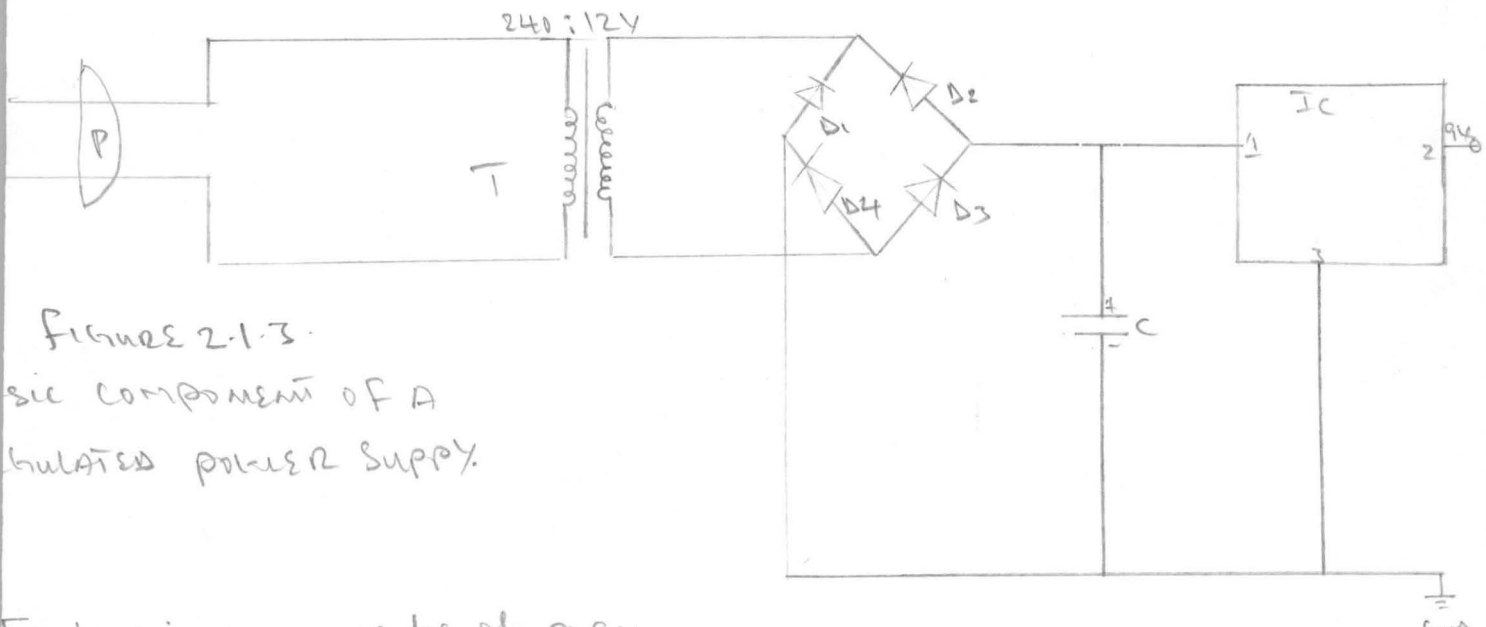


FIGURE 2.1.3.
SIC COMPONENTS OF A
GULATED POWER SUPPY.

he basic components of a 9V
er supply is shown above in figure 2.1.3

= 2-pronged a.c plug.
= Transformer (240V: 12-0-12V, 500mA)
= Through D4 : KBP04
C: 2200μF, 35V
IC: 7805

2.2 THE TIMER (PULSE GENERATOR)

The function of the timer is to generate timed pulses that are counted by the counter there are several types of astable muitilubrators that are in common but a quartz crystal oscillator was chosen for this project.

QUATZ CRYSTAL OSCILLATOR.

A quartz crystal controls the oscillation of an electric current the freguency of which is reduced to compute time.. The maximum error of the must accurate quarts crystal clocks is plus or minus one second in ten years. how our they are made from CMOS.

CMOS in computer science, acronym for complementary metal oxid semi conductor.A Semiconductor device that consist of two metal oxid, semi conductor field effect transistors (MOS FET One N- Type and one type integrated on a single silicon chip. Generally used for switching applications there device deuie have extremely low power consumption at some cost in speed. They are how ever easily damaged by static electricity.

A Phenomenon there by a potential Difference is developed across the opposite phases of a quarts crystal when a mechanical stresses are applied to it is called piezoelectric effects.

The extremely high quality factor or quarts crystals applied to osicllators Led to very stable frequency values such as used in timing circuits and clock signal generator. When a crystal is not vibrating it is

2.30 THE COUNTER SEQUENTIAL CIRCUIT

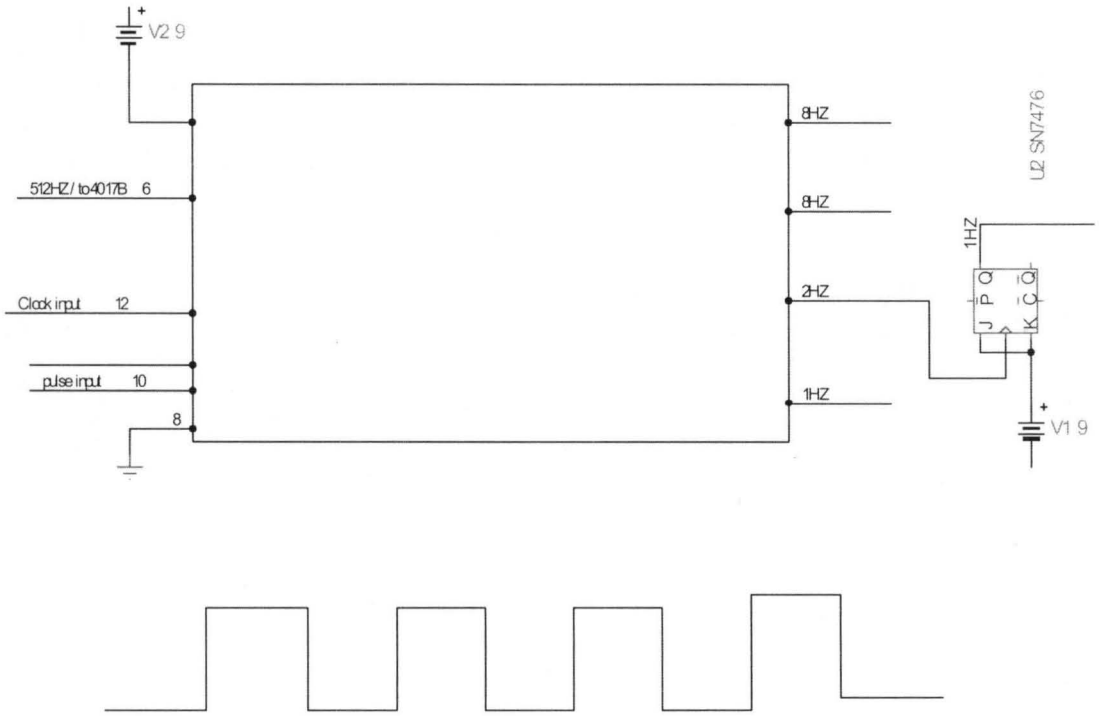
Counters are divided into 2 - main groups: asynehronous or ripple counter and synehronous counter despite the problem encountered with the ripple counters the simplicity of syrehronous counter makes them useful for application where their frequency limitation is not critical an there for synchronous counter has been chosen for this project.

DIVIDER BY 15- COUNTER

Many application of counter as frequency dividers digital clock fro example) require some other modulo but for this project me decided to use (CD 4060 B) Which is an oscillator divider. It has 14 fhip flops in side as component which divides are input frequently which is 32.7 86 by time.

However is flip flop is needed for the division to have second pulse period) but 40060B can only divide times to have a frequently of 243 which MOTT =seconds then an external J.K flip flop at toggle state is required which has 2Jla Fhip Flop inside one of them is used after the addition the frequently out put is I second. how ever the 2Jla flip flop IC used is 4027B.

The circuit disgram of the divider by is counter is shown below in figure 2.30.



the first state of the design Process is to set down the desire sequence and to examine it to see which state must change state at each step and what signal are available to initiate these changes. But J.la change state when its clock input goes from to o for any given present state of the output the flip flop may be required to keep up any particular next state and the table sets out the necessary inputs at J and la for each of the four possibilities shown in the table below.

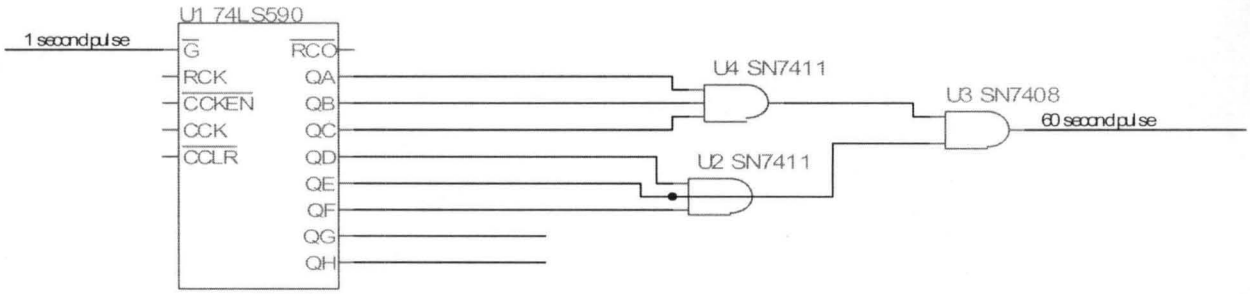
Present out put	Desired next out put	Required input	
Q	Q	J	K
0	0	0	x
0	1	1	x
1	0	X	1
1	1	X	o

Transition table for J - k flip flops

FOR MINUTE DIVISION.

Component CP4520 13 is used it is an 8- bit counter the counter starts counting from using the one below pulse the Jla counter resets itself back to OOOOOO(O) however an AmD gate decodes the binary (80) before reset so as o have a pulse during the period of the binary codes. The pulse share is give below in figure 2.31.

60 seconds



THE TRUTH TABLE FOR THE 8-BIT COUNTER

INPUTS	A	B	C	D	E	F	G	H	OUTPUTS
0	0	0	0	0	0	0	x	x	0
1	0	0	0	0	0	1	x	x	0
2	0	0	0	0	1	0	x	x	0
3	0	0	0	0	1	1	x	x	0
4	0	0	0	1	0	0	x	x	0
5	0	0	0	1	0	1	x	x	0
6	0	0	0	1	1	0	x	x	
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
59	0	0	0	1	1	1	x	x	1

We can deduce from the diagram that only 6 bits out of the 8- bit that are only function due to the fact that only 11110 (60) is required.

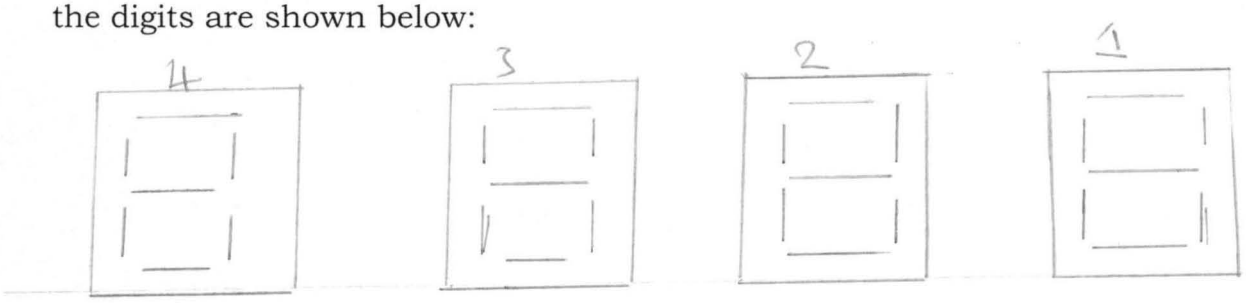
2.4 THE COUNT ACCUMULATORS.

The count accumulation job is to count the input pulses and to serve as a temporary among while passing the current time through the deode into the time displays.

The clock has four naira counter which are grouped into 2 group two for minute and the other two for reading hours

COUNT 1

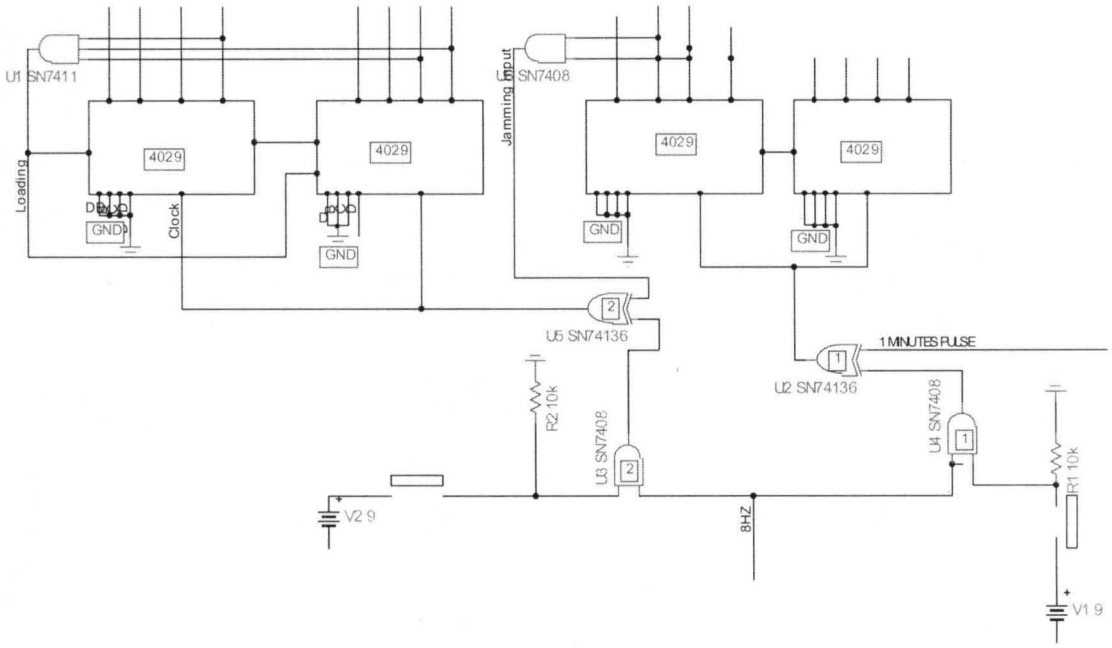
Counter number 1 serves digit one (1) and counter 2 serves for digit 2 the digits are shown below:



Counter 1 counts from 0 9, but counter 2 counts fro 0 - 5 so that on combining the counts, number 59 will be formed, Remembering that 60 seconds is feed into the next group that is for hours.

However, it is important to note that as counter 2 start from 0 - 5, at that moment that we have 59 going to 60, And gate 1 decodes 6.030 as to reset the jump back to 00: We have a count from 00 - 59, at 60 the whole counter starts from 00, the and gate out put now a cent every 60 minutes and operates the hour counter, the output passes through Or gate 2 before it can be used as a clock for the hour counter.

Its schematic diagram is shown in figure 2.40



HOURS GROUP

Hour counters consist of two (2) counters counting from 01 - 12. The counter 3 is a decade type counting from 0 - 9 9, but counter 4 is very different, it counts from 0 - 1. When the combine counter starts from 01 ---------- of ---------- 09 ----------10 ---------- 11----------12 13 the and gate 2 decoder decodes binary code 12 which in turn sets the whole count to 01 the output of the AND gate is connected to the preset input of the two counters involved. When the preset is high counter 3 loades 0001 (which is already at its heading input) and counter 40000 (which is already at its loading input).

However, "3" won't show because it turns to 01 at micro seconds so fast that it will not be noticeable, this effects gives a count of 01 - 12 periodically.

Furthermore, or gate and 2 are used to set hours and minutes respectively. Whenever set botton 1 or 2 are pressed logic 1 enters through the selected or gate and behaves as it the required check to counter advance the counter.

Or gates jump up input logic towards its inputs the truth table of an AND gate is show below:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Note: The output of the counters are connected to a group of butters (4 in number) one fore each counters.

2.5.0 MULTIPLEXERS (4503)

BUFFER

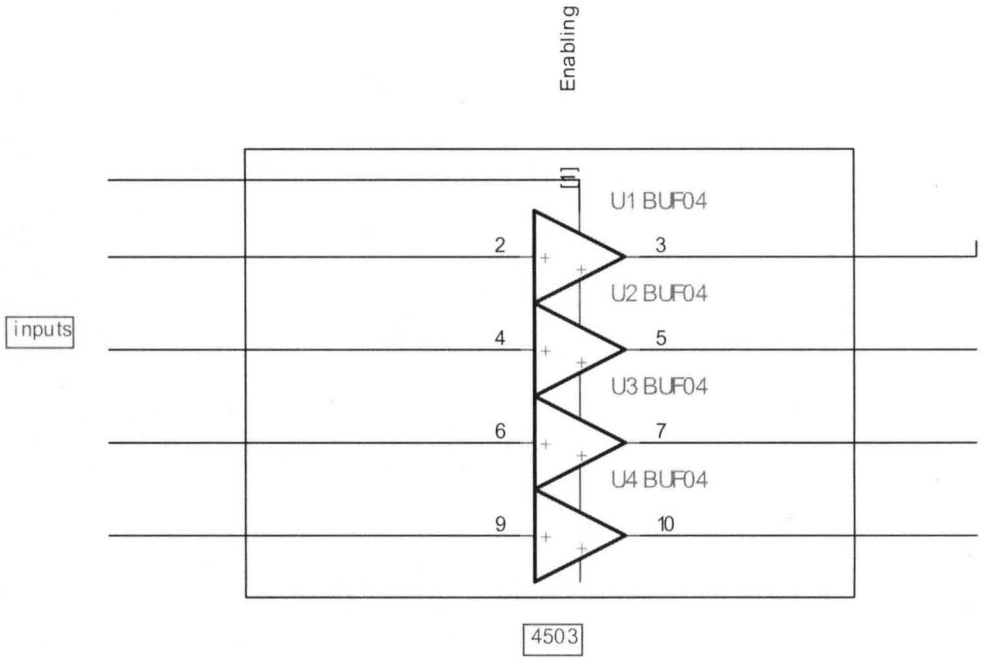
The buffers (4503) is a non investing buffer, it's enabling input is used to enable or cut off the incoming input toward the output.

When the enabling input is 0 (low), the code or logic flows, but when the enabling input is 1 high (high) the input codes do not flow (the code is cut off).

However, this mechanism of the butter is used to multiplex the outputs of the counter towards the only decoder (4511) which displays the digital on the display panel.

NOTE: Multiplexing is a technique used in communications and input/output operations for transmitting a number of separate signals simultaneously over a single channel or line. To maintain the integrity of each signal on the channel, multiplexing can separate the signals is a multiplexer.

The internal structure of the buffer is shown below in figure 2.5.0 for better understanding.



However, to check the functionality of the buffers a scanner will be required to be able to enable a buffer at a time to avoid conflictions, then a stepper is used (401703) to scan the buffers.

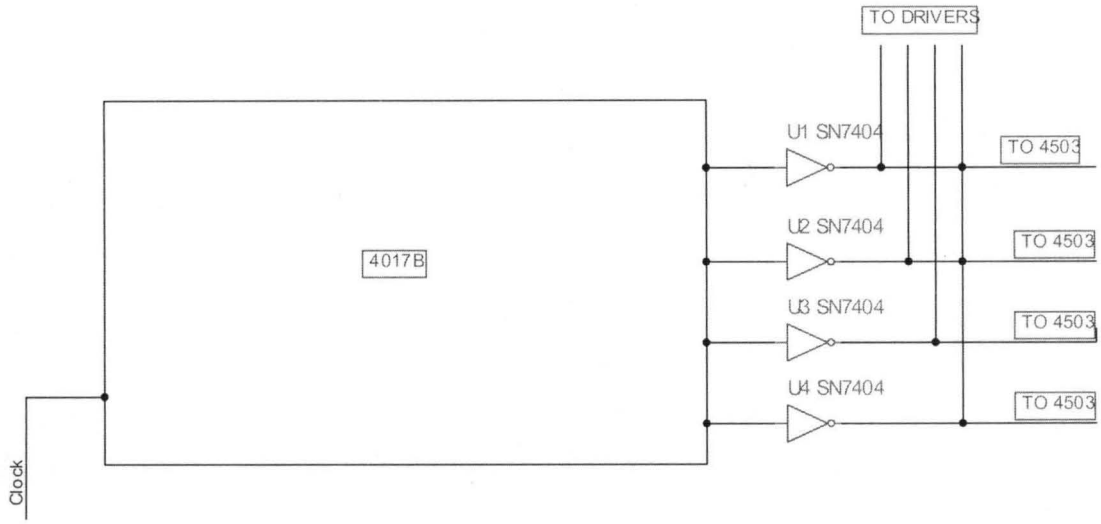
The truth table for the scanner is shown in below 2.5.0

		OUTPUT		
Clock	1	2	3	4
0	1	0	0	0
1	0	1	0	0
2	0	1	0	0
3	0	0	0	1
Back Again				
4	1	0	0	0
5				
6				

A truth table 2.50 for the stepper (401713)

The 4017B operates in a mode that only one of the buffer will be enabled that is it is only one of the buffers that will be connected to the 7 - segment decodes (45113) the rate of the scanning connects each of the buffer with their output from the respective counter to the decoder.
But for enabling the buffer logic "O" is required, so the not gate, (4069) in the multiplexing circuit are used to invert the logic 1 from the 4017 so as to make the 4017 and 4503 compatible. The diagram of the stepper

connected to the inverter and the drivers are shown below in figure 2.510



stepper

2.6 DECODER/DRIVERS

Many numerical displays use a 7 - segment configuration to produce the decimental characters 0 - 9, 7 segments displays are used to convert a 4 - bit BCD number into a visible read out, each segment is made up of

a material that emits light when current is passed throughout. Modern hand calculators, digital clocks, uses 7 - segment displays for their read out - 7 - segments may be of L.E.D. types, LED which is commonly used is chosen because of its brightness, low cost, reliability and compatibility with low voltage integrated circuit the figure below shows the 7 - segment arrangement.

(a) 7-segment arrangement

(b) Active Segments for each Digits.

(a) The segments of the 7 - segment display turn on that which most closely approximate the shape of the decimal digital equivalent to the binary values of the input, figure (b) shows the patterns of segments which re used to display the various digits. Since the numbers to be presented must be between on and 9. Numbers greater than 9 should not appear on the inputs and the outputs corresponding to these prohibited inputs are written as don't cares. In the typical 7 - segment display shown in figure each segment appears at a terminal and all segments are connected in common to a supply terminal and all segments are connected as a command anode display. In which the positive side of the power supply is connected to the anode of each segment and a voltage (0) at the segment cathode lights the segment, or they may be connected as a common cathode display in which the negative side of the power supply is connected to the cathode of each

segment, but for this project a common anode 7 - segment LED display is used the truth table for a common anode 7 - segment display is shown below in table 2.61

Truth table 2.61 for common anode connection display

Decimal Display	Input									
	D	C	B	A	a	b	c	d	e	f
	g									
0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
	5	0	1	0	1	0	1	0	0	1	0
	0									
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

Using 19 - map to determine the minimal equation for each output gives group of tables designated by table (a)

Driver 1 using 25A733 are used to switch 1 particular display related to the counter connected through the butter to the decoder to that display.

The speed of the 401713 s very high around 512H3 which is gotten from 4060B oscillator frequency divided. so that one won't motive the multiplexing effect of the display.

Driver 2 using 2SC945 are used, the divider output of 4511 B to the display LEDS.

All the corresponding segments are connected in parable to a common anode.

Each segment consist of one LED the anote of the LEDS are all tied to 9V the cathodes of the LEDS re connected through current limiting resistors to the appropriate outputs of the decoder/driver the decoders/drivers has active low outputs which re open collector driver transistor that can sink a fairly large current this is because LED red outs may require 10MA to 40MA per segment depending on their type and size.

To illustrate the operation of this circuit, let us suppose that the BCD inputs is D = 0, C = 1, B = 0, A = 1, which is BCD 5, with these inputs the decoder 1 drivers outputs a, f, g, c and d will be driver low (connected to ground), allowing current to flower through the a, f, g, c, and d LED

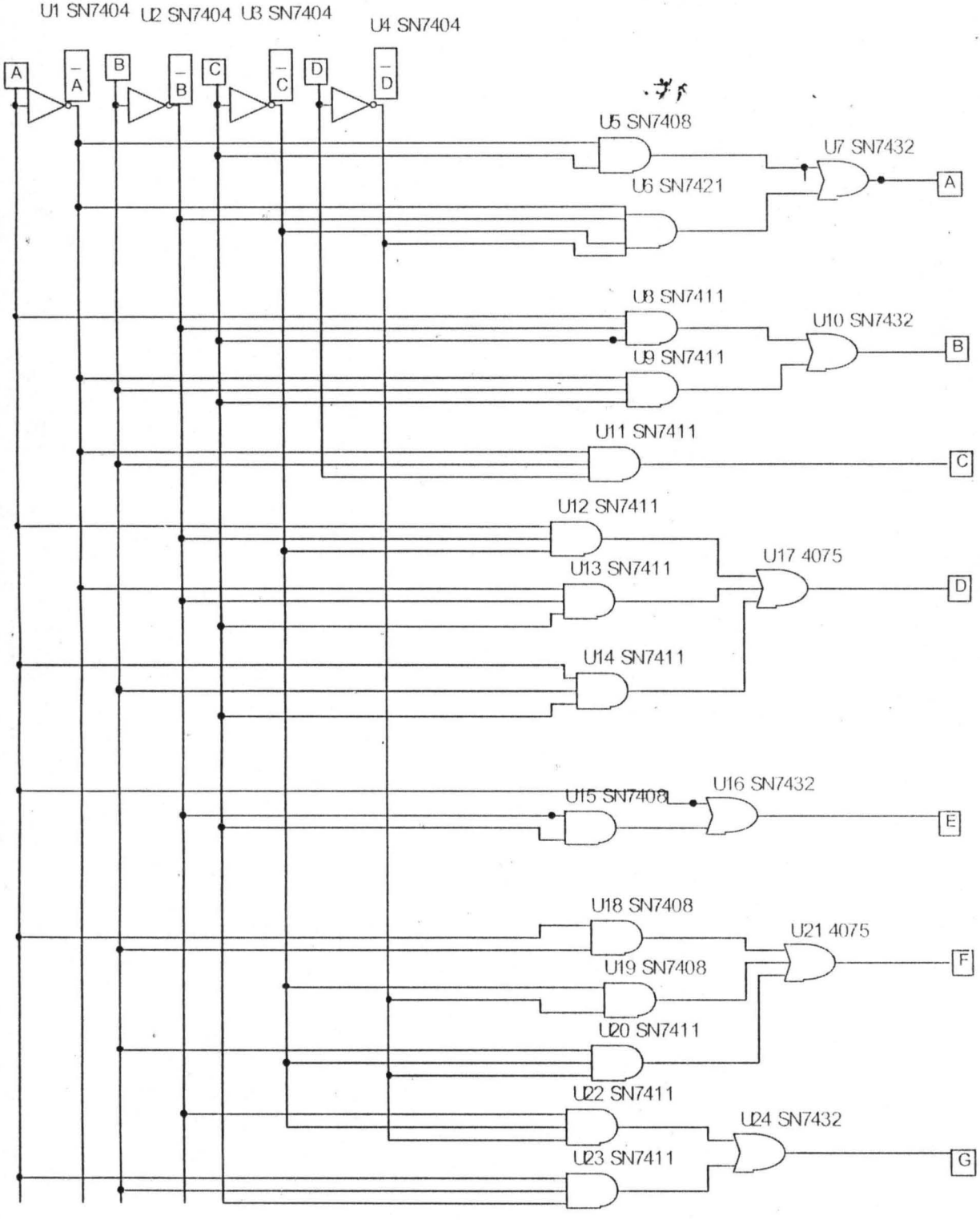


Figure shows a BCD for a 7-segment decoder driver

figure shows a BCD to 7-segment decoder/driverbeing used to drive a 7-segment LED READ-OUT.

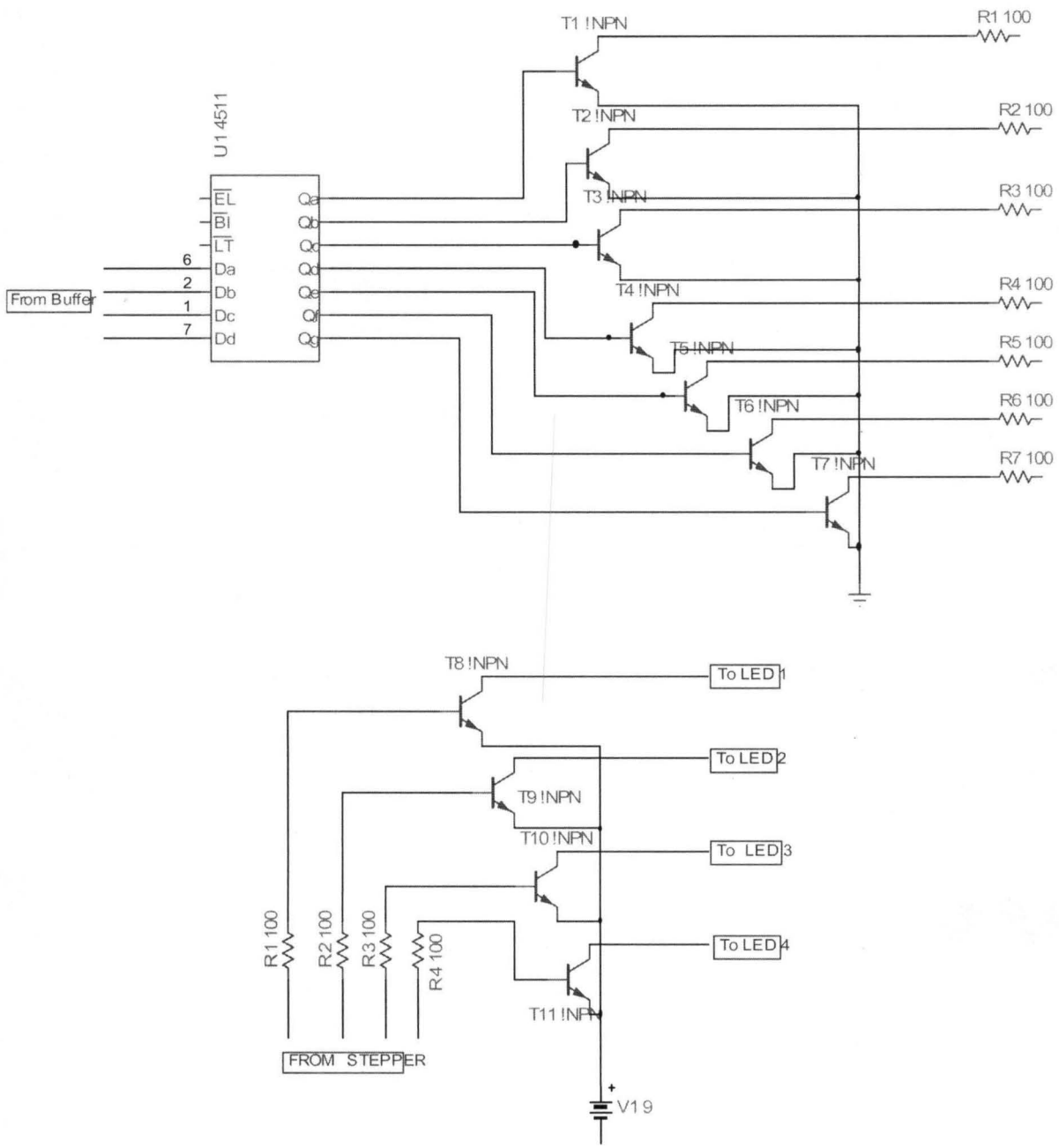


FIGURE bcd to 7-segment decoder/driver driving a common anode 7-segment LED display

segments and thereby displaying the numeral b and c cannot conduct. The LED display used in figure (c) has a common anode type because anodes of each segments are tied together to 9v. Each segment of a typical 7 - segment LED display is rated to operate at 10MA at 2.7v for a normal brightness we can see that the series resistor will have to have a voltages drop equal to the difference between 9v sand the segment voltages of 2.7v. This 6.3v cross, the resister must produce a current of about 10MA. Thus we have, RS = 6.3v/10MA = 630 a standard resistor value close to this can be used. a 220 resister would be a good choice.

CHAPTER THREE

THE CONSTRUCTION

3.0 INTRODUCTION

In the construction of each of the sections that makes up the Digital clock the design specification are sterilely adhere to.

The power supply was constructed as designed the timer (pulse generator) section was also constructed with a little change in the design the count accumulators were constructed as designed.

As much as possible the logic Family used in the project is resistricted to a particular one CMOS after considering the problems associated with the interfacing of different logic things considered during the choice of logic family are briefly discussed below.

3.1 CHOICE OF LOGIC FAMILY

It has been a common practice to classify logic families by the circuit configuration of the basic gate technology the earlier types being Register logic (Del) Resistor transistor logic (RTL) and Transistor logic (DTL) these early types have been largely superseded by the following I.C. Logic families. Transistor -transistor logic (TIL emitter coupled logic (ECL) and complementary order silicon logic COS) and come are the most popular but use different technologies in their manufacture (TT) bipoler unipolar

which have different handling

When handling CMOS devices great care must be taken since they are very susceptible to damage from excessive voltage caused by static electricity and equipment which is not correctly earthed.

POINTS TO REMEMBER WORK WITH CMOS GATES

(a) Ti e unsed inputs to licc with a 1kz resistor or directly to ground.

(b) The outputs of CMOS gates should not be connected together

(c) The Maximum signal is 7V

(d) The Maximum Signal is 1-5 to 5-5v

(e) There is maximum fan out of 10 gates within each CMOS family.

(f) Install a 0.2-or0.02 Nu by pass capacitor is feasible

(g) Connecting head should not be more there 12to 124 inches (30-5 to 35 6cm) for standard CMOS.

3.2 THE COUNTER AND COMBINATIONAL CIRCUITS.

In the counter construction the divide by 15 counter was constructed with a divide by +4 counter feeding a ship flop 2Jia counter the count accumulator was also constructed using an 8-bit counter with only 6-bits functional.

The light emitting diodes (LEDS) were used as the 5 second indicator

they emit light when they are forward biased and should be counted with a service registor to limit the counrent flowing through it.the diagram of the LED is shoun in figure 3.1 and the coloure type used for this project is blue and green.

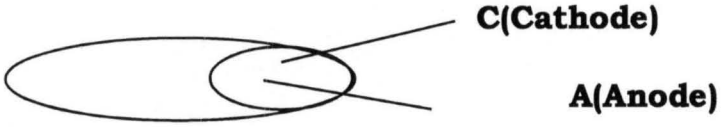


FIGURE 3.2

3.3 CONSTRUCTION

The power supply is a D.C. Energy VIa the use at a butterly cell.

The pulse generator was constructed using a quartz crustal oscillator as an Astable multivibrator with R-A I mr and a capacitor of 22 PF guing 32.7 st kt3.

The count accumulator section was constructed by using an 8 bit counter feeding decade counters.

The decoder/Driver display was constructed using the output of the count accumulator as its own inputs and a resistor of (1002) 200 of each was used to limit the current from the output at the deode the segment dispel.

The stages are arranged is such a way that the out put at one stage serves as the input to the other stages.

Which count and display hours from o through 23. This hours section

is different from the second and minutes section the circulatory in this section is sufficiently unusual to warant a closer investigation. Fig 1.01 shows the detailed circutory in the hours section it includes a BCD counter to count unit of the hours section and a MOD counter to count tens of hours the BCD counter counts only between OOO and 1001 and count up in response to the I pulse per hour signal coming from the minutes section.

The Inveter on the CPu input is needed because the BCD counter responds to pGTs and we want it to respond to NGTs that occurs when the Minutes section recycles back to ZERo hour for example at 7 cloua this counter will be at 0111 and its decoder/ display ciruitory will display the numeral 7 at the same time Q2 od mode counter will be low and its display will show a Zero this two displays will show 07 when the BCD counter is in 1001 (9) state and next toggle MOD 3 counter Q2Q from))to)1 this produces a mumeral 1 on the MOD 3 counter display and a numeral "O" on the BCD display so that the combined display show 10 for10 O' clock

CHAPTER FOUR

4.0 TESTING AND ERROR DETECTION

What the construction was completed the distal clock was teated at each stage.

The power supple has already been known since its from a try cell (Batter of 9v

The timer output was tested by feeding its output into an oscilloscope and the measure ment geuite 1.2 my and Tz =1.8 ms but T=t.ttz there-fore f=Yt 32.

The divider 15 counter output was also tested using an oscilloscope to deter mine its presumey found to be 1 it 3 (IPPS)

The count accumulator was tested when it was few in to the deode driver display which the display shows the counting seguaies.

For error detection the LED indicator at the power supply output will be on when there is power at the output of the timer also the LED will also be on if the time is in good condition at the output of the divider by is counter is another stop if there is an cmor in the circutory and for the count accumulator the 7 segment display indicates the counting sequence therefore if there is can error the display will be off.

The mext four pulses advance the BCD counter to 0101 (4) in this state the counter's Qz output HIGH and Qz and Q t Mods counter are

both btigh to the MAMD gate. This the NAND gate output goes low and activates the MOD 3 counter and PT Input of the BCD counter. This cleas MOD counter to a and presets The BOD Counter to 000 the resuts is a display of"O" for 120 clock in the eary morning and night.

This report assumes that the reder has a basic lanowledge of both digital and power. A basic lanowledge of combinationaland sequential circuts helps us understand the time conuter and conbinational circult sections of the project. Also Litle hnowledge of power will help him understand the power section.

In order to understand the report more the first chapter thows some light on some necessary basic topics. The second chapter deals with thge desig component. the third chapter state how the design obective of the second chapter is achieved in the constructive faces. Chapter four goes to present. the falrication and the tests carried out.

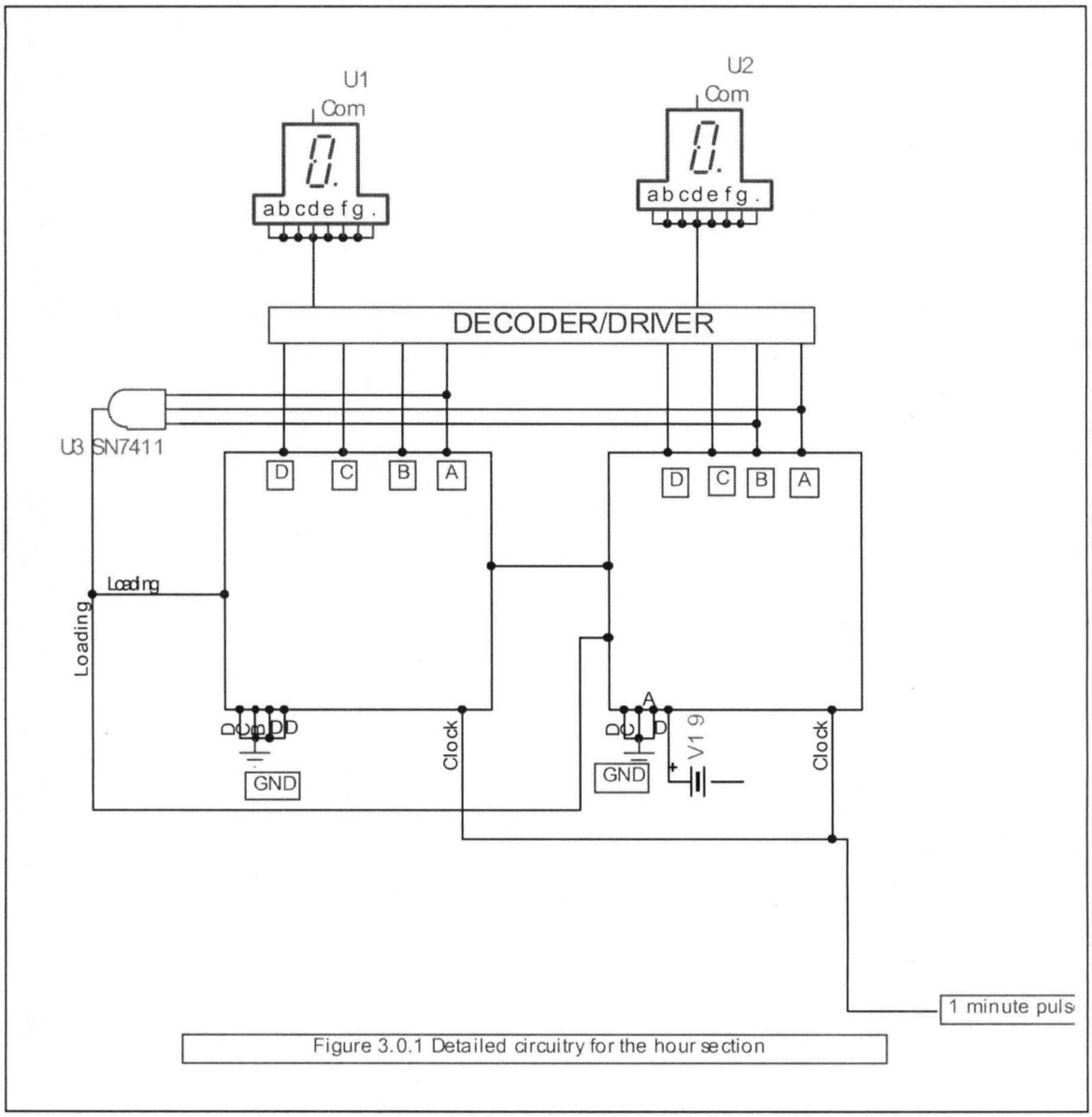


Figure 3.0.1 Detailed circuitry for the hour section

CHAPTER FIVE

5.0 CONCLUSION AND RECOMMENDATION

Having tested all the stages it can be seen that the disital clock can be desigined and constructed from the basic prineiple of eletronics countiing and seguening using counters.

To some great sctend the objective of the desigin was achieved in the congtruction that is the desigin and contruction of addigital clock to display time sequentially which display the time of the day in hours and minutes which seconds is the LED indicator.

It show be seen from the test carried out in the department laboratry that theontieal caluclation agree withgin the practical calculation.

Although H there is a failure the disgital clock will be out of use therefore it coud be suggested that the power supply section showd be replaed with an uniterupt able power supply the second sections which is been indicated by LED coud also be replace by two 7 segment displays insted..

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