DESIGN AND CONSTRUCTION OF RECORDING/PLAYBACK DEVICE

BY

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MATRIC. NO 2003/15393EE

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

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A THESIS SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

NOVEMBER 2008

DEDICATION

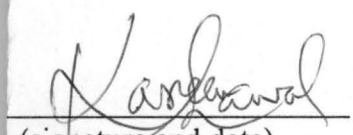
s project is dedicated to Almighty Allah, the creator of the heaven and earth with all

ein. It is also dedicated to my parents and to all my teachers especially my Mallam.

DECLARATION

AREEM, LAWAL OLALEKAN , declare that this work was done by me and has never
n presented elsewhere for the award of a degree. I also hereby relinquish the copyright to
Federal University of Technology, Minna.

REEM, LAWAL O.
(Name of student)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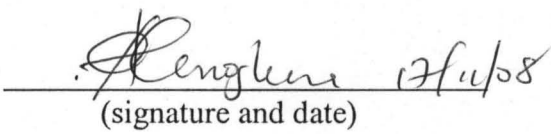
ENGR. (MRS) C.O ALENOGHENA
(Name of supervisor)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GR. DR. Y.A ADEDIRAN
(Name of H.O.D)

(Signature and date)

(Name of External Examiner)

(Signature and date)

ACKNOWLEDGEMENTS

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I thankfully recognize the effort of my friends, because "Friendship without self interest is one of the rare and beautiful things in life". In that case I am magnanimously indebted to my following friends: Azeez Taofiq, Ismail Taofiq, Mrs Fatimo Adejumo{spain},Modinat.A., Babatunde Qasim, Abu Aminah, M.Sarafadeen and Miss Fatimoh Sulaiman{Habibatiy}.I cannot but also commend the effort of those whose names could not be reflected here but in one way or the other contributed to the

success of my degree. May Allah be with you all. May the peace and blessing of Allah be upon our noble prophet Muhammad {S.A.W}, his companions, his households and the Muslims who adhere to his teachings. {Amen}.

ABSTRACT

ording and playback Device is a device that is capable of storing analogue speech sounds igital form and reproduces it when desire in exact way it has been stored.

device has input signals from microphone, this input data is stored and processed by a seconds, 480k cell non-volatile EEPROM. Recording and Playback are initiated and cated by a toggle switch and two different colours LEDs respectively. Both processes can paused or altogether terminated simply by push (start'/pause and stop/reset) buttons. The io output is achieved through a 16Ω speaker via an inbuilt amplifier in the IC (ISD2590).

s device breaks the monopoly of the mechanical means of recording and as such minates the problem of loss of data on exposure to stray magnetic field.

e constructed project has been tested and worked with specification (90s).

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CHAPTER ONE

INTRODUCTION

A Digital Playback/Recording Device is purely an electronic device which converts and analogue signal representing a voice to a digital signal and records the digital signal in a recording medium. When the voice is recorded, it converts the digital signal to an analogue message when the voice is reproduced.

It consists of several transducers, driver stages, regulated power supply unit and has at its heart, a newly developed chip, on which all data are stored. The input transducer is an Electret microphone. It is a device that is capable of converting analogue speech sounds, in form of varying wave patterns, into slightly appreciable electrical signal (current). [3,4]. This signal is amplified by an in built amplifiers and decoded by decoder which converts the analogue signal generated into binary digits (bits) for further processing.

This device provides high-quality, single record/playback solutions for 90 second messaging application. The device also has an on-chip oscillator, microphone preamplifier, automatic gain control (AGC), anti-aliasing filter, smoothing filter, speaker amplifier and high density multilevel storage array. Digital compression/de-compression circuits may be employed to increase storage capacity for a fixed memory size. These integrated circuit recorders may record analogue value representing the instantaneous amplitude of the sound reaching the unit's microphone or microphone output may be digitalized and stored as binary values. The analogue signal representing the collected voice is converted to a digital signal which is the then stored in a storage medium of the digital recorder. Then the recorded voice is produced, the stored digital recorder. Then

the recorded voice is produced, the stored digital voice is read out from the storage medium and converted to an analogue signal. The analogue signal is then reproduced by a speaker [1].

Most voice recorder provides basic function such as record, stop, play rewind and fast forward. To permit a user to selectively activate these functions, a number of manually operable switches are typically provided on the cosine of the recorder, of which the Recording/Playback Device also incorporates some. In addition, the device is microcontroller compatible allowing complex messaging and addressing to be achieved. Recordings are stored in on-chip non-volatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through multilevel storage technology [2, 5].

Voice and audio signals are stored directly into memory in their natural form, providing high-quality voice reproduction.

.1 Objective of this Project.

The design work aims to demonstrate how a single, very flexible and versatile hip can be used to record and playback analogue speech sound eliminating the former nechanical means and the problem associated with it.

.2 Methodology

The main building blocks on which the design project is built around is as shown elow.

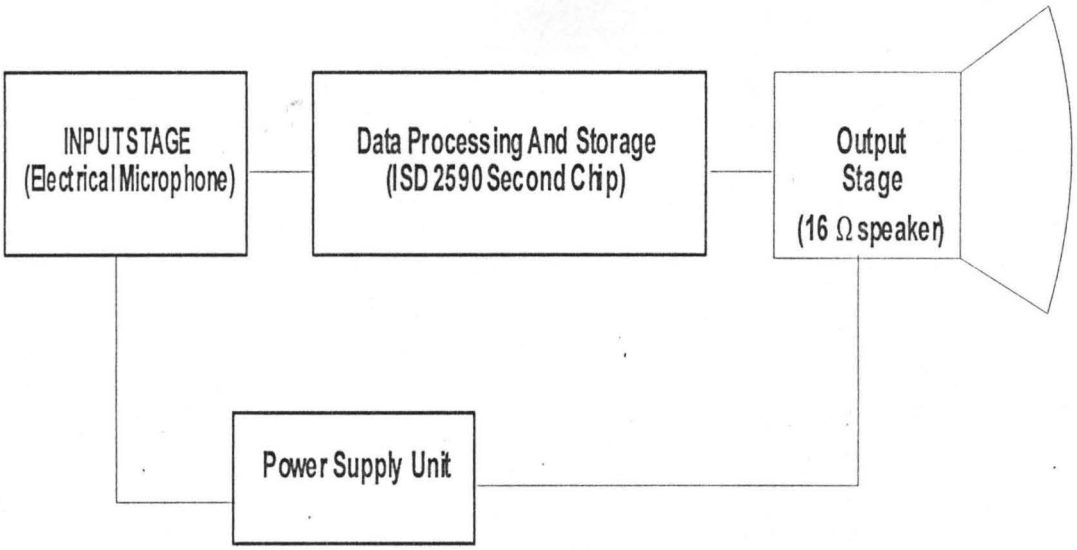

Fig.1.1: Building Block.

The input stage consists of the input transducer (microphone) that converts the analogue speech sounds into electrical signal of small magnitude.

Storing and processing of the input data is accomplished by a 90 second 480K cell non-volatile electrically erasable programmed read only memory (EEPROM). Record and playback are initiated by a simple toggle switch while playback can be paused or altogether terminated by a simple push stop/reset button.

The output (audio) is achieved through a 16-Ω speaker from an inbuilt audio amplifier. The power is supplied to both input and output stage from a 6V dual source power supply unit (from both AC and DC).

1.3 Project Layout

This project is divided into five chapters for easy references. The feature of each chapter is summarized as follow:

CHAPTER 1

CHAPTER 2

This comprises literature review on the old forms of recording voice message, their limitation, and the present means of recording, the project and future improvement.

CHAPTER 3

Here the general description of the device is done, the analysis of each circuit block and design are also carried out.

CHAPTER 4

This chapter discusses the result obtained and compares it to the values recommended by the manufacturer. Also in this chapter, the operation modes and operating principle of the project are discussed.

CHAPTER 5

Here the conclusion drawn on this project and recommendation for future improvement are explained.

CHAPTER TWO

LITERATURE REVIEW

Recording is a technique for storing information on a storage device. It serves as a means of permanently documenting, individual speech, telephone message, musical sounds and instructions [2, 6].

The technique usually involves converting the speech sounds to be recorded into small electrical currents by microphones. The alternating current generated are embedded on storage elements, which varies from days of gramophone recording to more robust magnetic tape storage principle.

Playback can be only achieved by the use of special equipment that will extract the information from the storage and then reproduce it using several amplification stage and loud speaker.

2.1 Historical Background.

Before the advent of radio and telephone, messages are recorded using designated graphic symbols drawn on notepads. Such records are sent by human carries to various destinations from the sender to the receiver.

The first practical sound recording and reproduction device was mechanical CYLINDER PHONOGRAPH, which was invented by Thomas Edison in 1877 followed by the next major technical development which was GRAMOPHONE DISC, credited to Emile Berliner 1882 [6]. Disc which are double sided are easier to manufacture, transport and store and characteristics with loudness (marginally) then cylinders, which are single sided.

Sound recording began as a mechanical process and remained so until the 1920's with the exception of TELEGRAPHONE) when the string of ground breaking nventions in the field of electronics revolutionized sound recording and young recording ndustries. These included sound transducers such as microphones and loudspeakers and arious electronics devices such as mixing desk, designed for the amplification and nodification of electrical signals. In 1960s Lec De Forest invented the AUDIO TRIODE /ACUUM TUBE, electronic value, which could greatly amplifier weak electrical signals /hich became the basis of all subsequent electrical sound systems until the invention of ıe TRANSISTOR [6].

Emerging technologies in Radio and Telecommunications made it possible for ıessage to be relayed instantaneously from point to point. Such messages are stored on ıagnetic tape, which on exposure to stray magnetic field can result in the permanents ›ss of data.

In 1930s, radio pioneer Galileo Marconi developed a system of magnetic sound cording using real tape. This was the same material used to make razor blades. The erman Engineers invention brought about sweeping changes in both audio and cording industries. Sound could be recorded, erased and re-recorded on the same agnetic tape many times. Also duplication were possible with only minor loss of quality d recording, could now be very precisely edited by physical cutting the tape and ining it back[6].

The next important invention was the compact cassette introduced by Philips ctronic eventually led to the development of the Sony walkman, introduced in 1970s. is gave a major boost to the mass distribution of music recording. The "compact age"

brought so many advancements in area of data processing and data storage. Based on the volume of data involved in computing, so many resources had been committed to the field of data storage and data security. This is to ensure that data stored are retrieved in exactly the same format in which it was originally stored.

Analog to Digital converters (ADCs), Digital to analog converters (DACs} digital processors, data filters and operational; amplifiers made it possible to convert analogue speech into its equivalents. Such conversion will bring about good sound processing and storage associated with digital circuits, making it possible to get very good reproduction with little or no harmonic distortion.

In recent years, digital audio recorders have been developed in which audio information is stored as digital data in solid-state memory. Digital audio recorders generally employ non-volatile semiconductor memory e.g. flash memory, as a recording medium. A simple memory device may store several recorded messages, so address information indicating where each message begins and ends is also stored. Semi conductor device typically stored information in a large array of cells. These memories are broadly divided into two categories depends on whether the memory retains its data when the power is off as in Random Access Memory (RAM) or not in Read only memory (ROM) , Electrically Erasable Programmable Read only Memory (EEPROM) and flash memory. Computer applications used flash memory to store BIOS firmware where regular access to data is seldom changed. Peripheral devices such as printers store fonts on ROM and flash memory while portable applications such as digital cameras, audio recorders, test equipment and digital personal assistants use flash memory to store data [8].

2.2 The Project Design

This project design provides single-chip record/playback solutions for 90 seconds messaging applications. The input data from the microphone is stored in a 480K cell, non-volatile multilevel storage arrays, after being amplified by microphone pre-amplifier, then to an automatic gain control (AGC) which provides constant signal level to the data processor no matter the incoming signal strength and subsequently filtered by 5-poles active anti aliasing filter. The output (when selected from the address buffers, goes to decoder where the message is selected from the cell) also to 5 poles active smoothing filter to reduce the noise, then to a MUX (Multiplexer)which selects the desire message before amplification is done on the message again and finally pass the outgoing audio signal to the 16Ω loudspeaker [2].

Three LEDs are included to power supply level, recording and playback indication respectively.

CHAPTER THREE

CIRCUIT DESCRIPTION AND DESIGN

3.1 GENERAL DESCRIPTION

This project is made up of discreet components (like resistance capacitors, and diode) and linear integrated circuits. Other components include: microphone, loudspeaker and switches. The particular functions carrying out by the device are indicated by the LEDs indicators which are driven by bi-polar junction transistor.

The circuit can be broadly divided into various stages, the input stage data processing and storage stage, and the output stage as shown in the block diagram below.

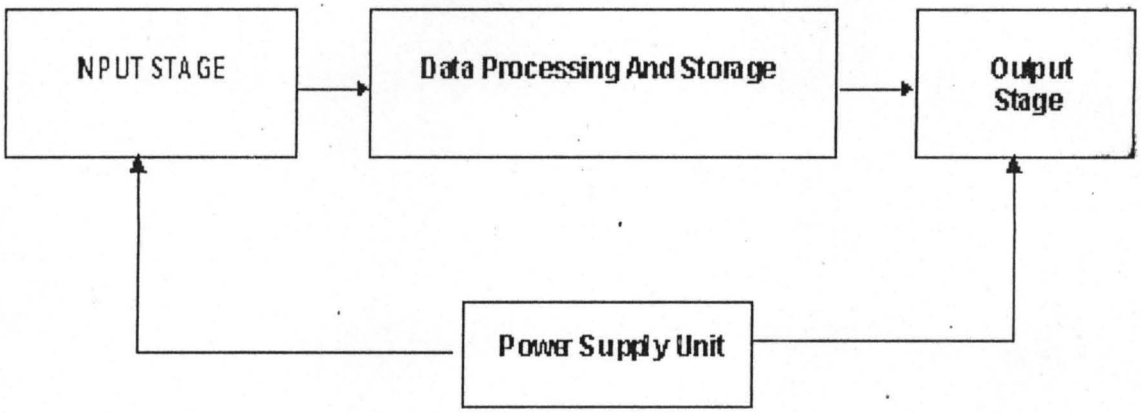

Fig. 3.1: BLOCK DIAGRAM OF THE DEVICE.

3.2 The Input Stage.

This stage consists of the input transducer (the electrets microphone) which stands alone as a single component; it converts the analogue speech sounds into electrical signal of small magnitude. It also has a pre-amplifier and the main amplifier that raise the signal level to the desired level. There is also a provision for an Automation Gain control (AGC) that ensures constant signal level into the data processor all of which are embedded in the IC.

2.1 Electret Microphone

An electret microphone, is a transducer that converts analogue speech sound into ectrical signals. Unlike the usual available microphone, it works in the principle that ırrent varies as the capacitance of a circuit varies [4, 14].

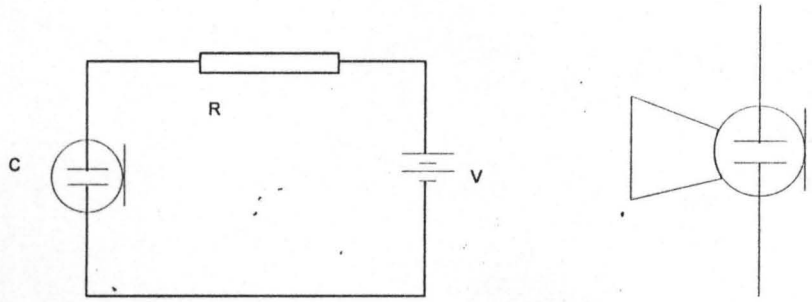

Fig. 3.2: Electrets microphone circuit & symbol.

e advantages derived from using this type of transducer are as follows;

1. They are very sensitive if compared with others.
2. Surround sounds can be eliminated before the converted signal get to the in-built amplifiers and filter system of the IC

2 Input Pre-Amplifier

nal amplification is achieved by using operational amplifier, as it's the most important ctions in electronics instrumentation. The need to amplify low-level electrical signals es frequently in converting low-voltage signal from microphone, tape player, radio iver, CD player to a level suitable for driving a pair of speakers. The op-amps are acterized with high gain.[3,12]

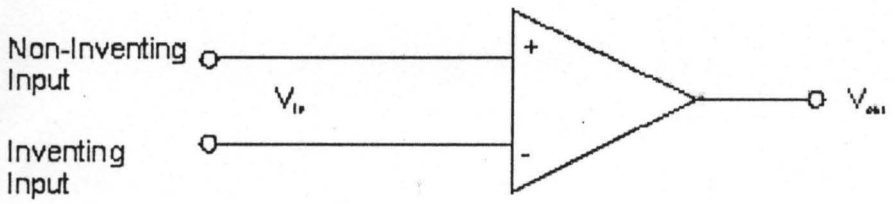

Fig. 3.3 Op-Amps Circuit Symbol.

$$V_{out} = \frac{-R_f}{R_i} V_{in} = AV_{in} \text{ : closed - loop gain for inverting op - amps}$$

$$V_{out} = (\frac{R_f}{R_i} + 1) V_{in} = AV_{in} \text{ : closed - loop gain for non - inverting op - amps}$$

3.3 Data Processing / Data Storage Stage.

The major features of this stage consist of:

i. Filter Network.

ii . Memory address buffers.

iii. Signal decoder.

iv. Analog transceivers and

v. 480K cell non-volatile multilevel storage array.

All the above serve the purpose of positioning the received signal (analog) in its appropriate bandwidth while eliminating unwanted signals, before the actual data storage[8,3].

3.3.1 Anti-Aliasing Filter / Signal Sampling

Filters in electronics devices make it possible to alternate or altogether eliminate signals of unwanted frequencies, such as those that may be caused by electrical noise or other forms of interference.

The speech sound signal generated is a continuous waveform (analogue signal), which must be processed for storage and retrieval.

Digitizing a signal consist of sampling and quantizing the signal. The frequency of such sampling must be that the sampled output gives a signal that is much closer to the original analogue signal. Thus, NYQUIST's CRITERION for sampling frequency f(s) must be considered, which stated that;

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In other not to lose any signal information, then the criterion for sampling frequency f(s) is;

$$Fs \geq 2fmax$$

Where:

Fmax is the maximum frequency component of the signal being sampled.[17]

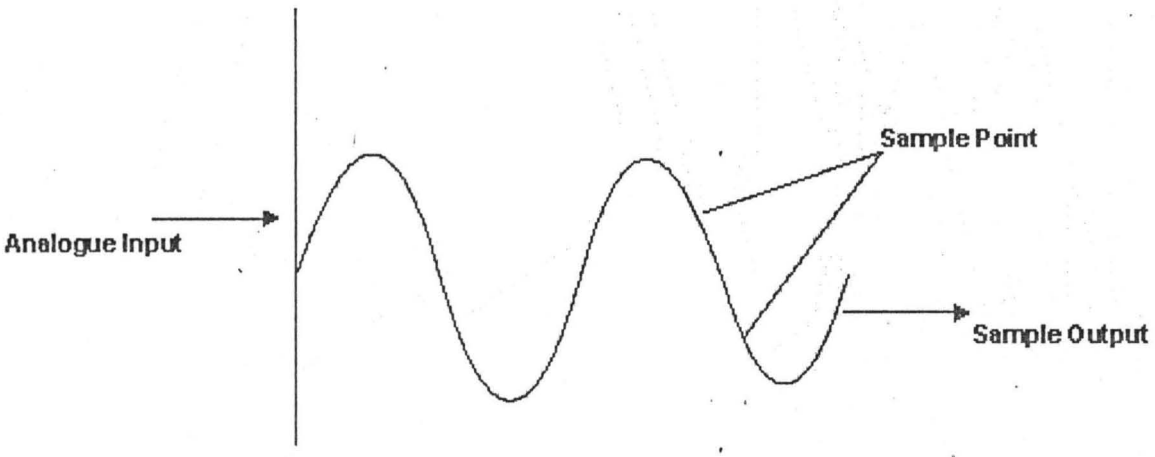


Fig. 3.4 Sampling Process Waveform

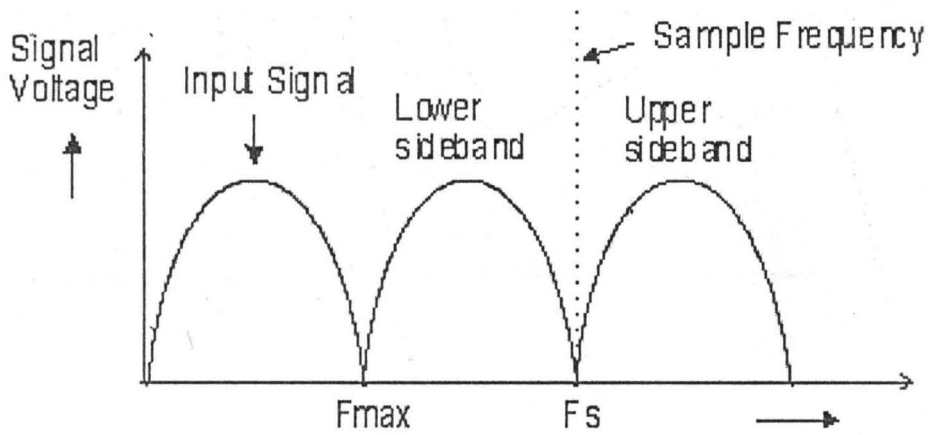


Fig. 3.5 Sampled Signal Spectrum.

Also, in order to avoid overlapping of the sampled signal, the use of anti-aliasing filter is necessary and must obey Nyquist sampling theorem as thus;

$F_s \geq 2f_{max}$

Where: f_{max} is the maximum frequency in the input signal.

If $f_{(s)} \geq 2\ f_{max}$ then,

$F_{(s)}/2 \geq f_{max}$

$f_{max} \geq F_{(s)}/2$

It is therefore vital analogue signals are subjected to anti-aliasing filtering prior to sampling in order to insure that no frequency components higher than $F_{(s)}/2$ are present.

3.3.2 Multilevel Storage Array (MSA)

MSA is a device on which the sampled data signal (digital format) is stored. It is classified as non-volatile, which means that it retains its stored data permanently, and removal of its power supply does not result in loss of data.

Any storage device must posses the following facilities [11];

1. A number of individual storage elements known as memory cells, each capable of temporary or permanent storage of a single binary digit.
2. A system of addressing which provides a means of selecting a specific memory cell (or group of cells) within the memory device.
3. A means of writing data into a specific memory location.
4. A means of reading data from a specific memory location.

3.3.3 Electrically Erasable Read-Only Memory (EEPROM).

Read –only Memory (ROM) is a type of memory that is used for non-volatile storage of data. Such storage is done by the hardware manufacturer according to bit patterns supplied by the user (the customer).

In this project, the memory device used can be programmed by the user (i.e. it is field programmable), erased and re-programmed. These processes of erasure and re-programming does not require that the device be removed from the circuit.[3, 8]

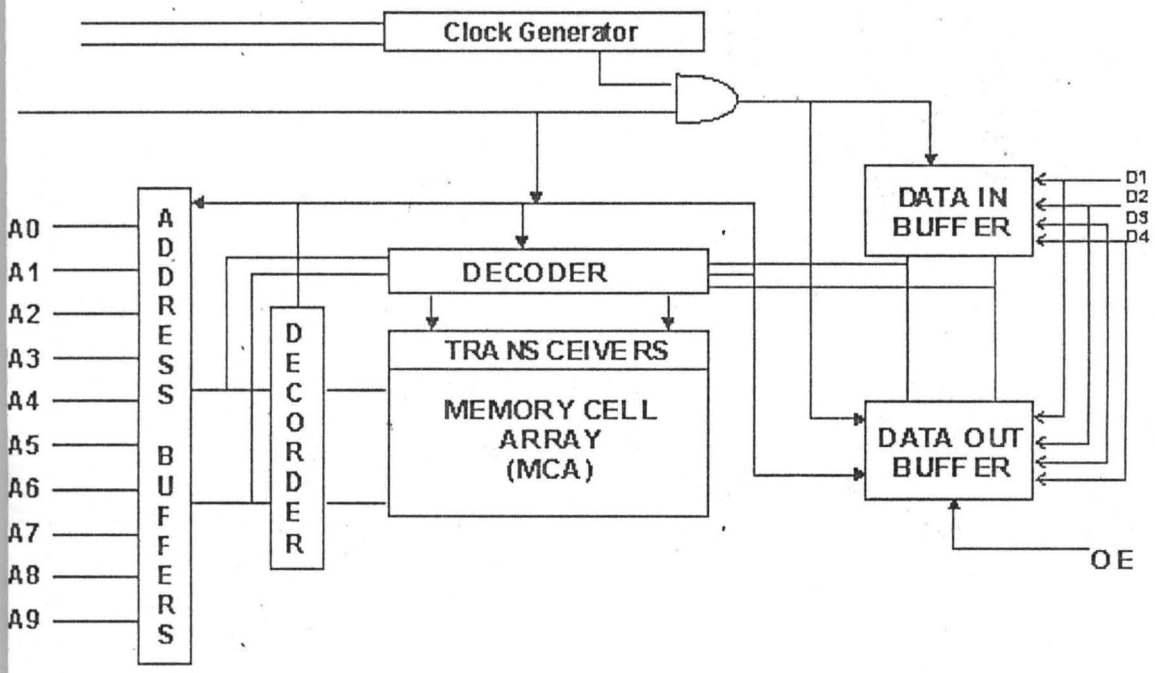


Fig. 3.7: Internal Structure of an EEPROM Device.

3.3.4 Memory Addressing.

Memory addressing is a system of addressing which provides a means of selecting a specific memory cell or group of cells within the memory cells array (MCA).

Data can be accessed or written into the memory cells array using a number of different ways to identify the location or destination of that data. Each method is known as Addressing Mode. The mode employed depends on the system architecture and design.

The following addressing modes are commonly used;

1. Implied Addressing Mode
2. Immediate Addressing Mode.
3. Direct Addressing Mode.
4. Indirect Addressing Mode.
5. Relative Addressing Mode.

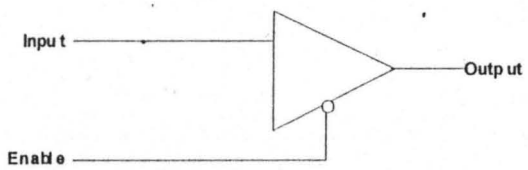
Several modes can be combined in order to accurately access data from a destination.

3.3.5 Memory Address Buffers.

A buffer is a device that is connected between two (2) parts of a system to prevent unwanted interaction. It serves as an Isolator. It frequently consists of a current amplifier or a small memory. A conventional buffer used in a logic current would have its output at one of two different logic states; logic O (low) or logic 1 (high), but there is a third output state of high impedance (tri-state buffers)[8].

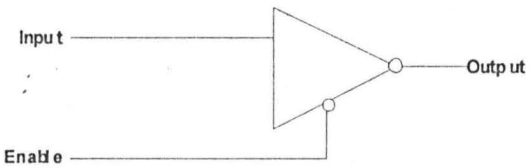
The types of buffer available are as follows:

a. Non- inverting, active low



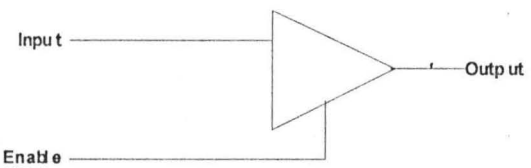
Enable	Input	Output
0	0	0
0	1	1
1	0	High impedance
1	1	High Impedance.

b. Inverting, active low.



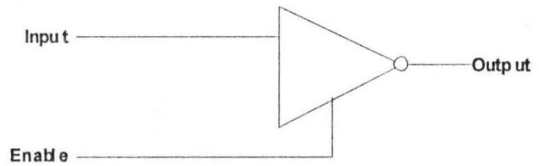
Enable	Input	Output
0	0	1
0	1	0
1	0	High Impedance.
1	1	High Impedance.

c. Non inverting, active high.



Enable	Input	Output
0	0	High Impedance
0	1	High Impedance.
1	0	0
1	1	1

d. Inverting, active high.



Enable	Input	Output
0	0	High Impedance.
0	1	High Impedance.
1	0	1
1	1	0

Fig. 3.71 Memory Buffer with their Truth Table.

3.3.6 Control Signals for Data Transfer

Data transfer are actually carried out when the address buffers have received appropriate control signals, applied to their chip enable (E) or chip select (Cs) input.

Controls signals require for the memory device used in this project design are as follows.

1. A chip select (Cs) signal to select one particular memory location or group of cells.

2. An (RD) Read signal to enable the output buffer to allow memory place data onto its output.
3. A write (WR) signal to enable the input buffer to allow data to be stored into the memory[9].

3.3.7 Addressing Decoding

Decoding is the use of a logic network to detect unique combinations of binary input having its own particular output.

Memory chips make use of binary addresses, (which must be decoded) since this result in a reduction in the number of address select lines. Required for a given memory size. If "n" address lines are available (A_0, A_1, A_2...A_n) on a memory chip, the 2^n different binary outputs are possible.

For 1SD2590 chip, the address lines available are ten (A_0, A_1, A_2...A_9). This means that it will permit 2^{10} different locations to be addressed (i.e. 1024 unique memory locations) [3,8].

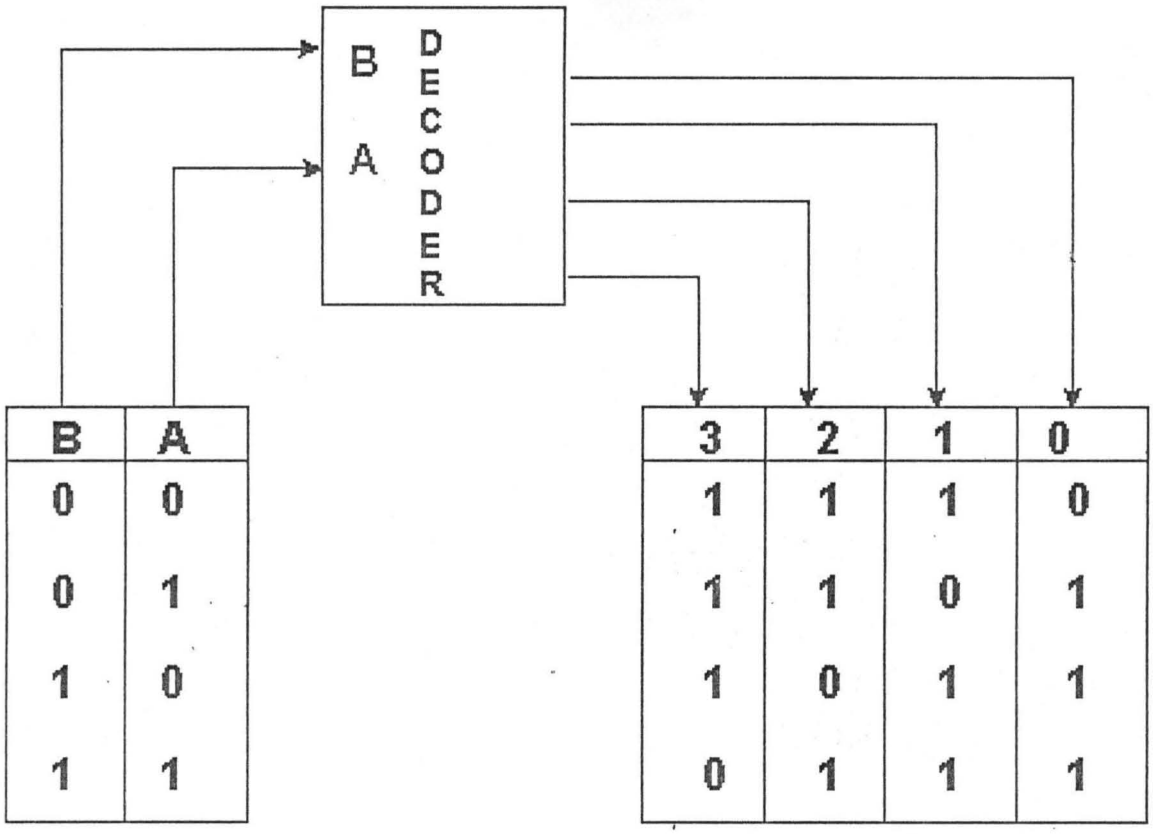


Fig. 3.8: A Typical Address Decoder.

The above logic diagram makes use of logic state "0" detection rather than logic state "1" (it uses NAND Gates)

3.3.8 Smoothing Filter

It is mandatory that the frequency bandwidth of the project circuit be restricted. This is necessary for the purpose of optimizing the signal-to-noise ratio.

Hence, it makes sure to limit the bandwidth of the system to the minimum, since noise power is usually directly proportional to bandwidth, which will allow the wanted audio signal to pass un-impaled.

On playback, analog transducers will convert the stored digital signal into a true replica of the original analog speech are removed by the smoothing filter, which is a low-power active filter matched to the frequency spectrum of the analog speech sound.[8]

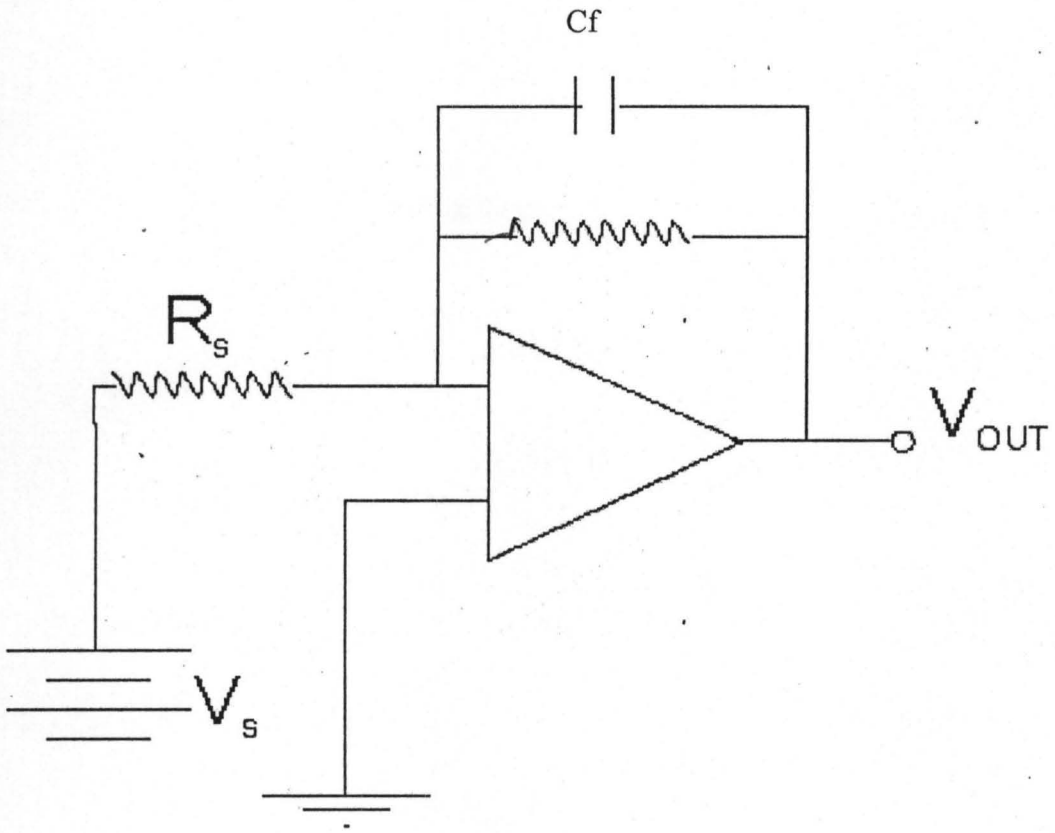


Fig.3.9: Typical active low past filter

3.4 Output Stage

3.4.1 Power Amplifier

The output of the smoothing filter is further fed into an audio frequency (AF) power amplifier in order to raise the signal level to point suitable in driving the output transducer (Loud speaker).

Operational amplifier found diverse application in their regard. This is due to the unique characteristics of the ideal op-amp such as:

1 Infinite gain ($A = \infty$)

2 Infinite bandwidth

3 Infinite input Resistance ($Ri = \infty$)

4 Zero output resistance ($Ro = 0$)

And they can be used in either inverting or non-inverting mode.

3.4.2 Loudspeaker

A loudspeaker function is to convert analog electrical signal to analogue speech / audio sounds.

It uses a permanent magnet and a moving coil to produce the vibration motion that generates the pressure waves we perceive as sound. This vibration is caused by changes in the input current to the coil; the coil is, in turn coupled to a magnetic structure that can produce time varying force on the speaker's diaphragm. They are generally low impedance transducers that are very sensitive to the electrical signals coming from the power amplifier.

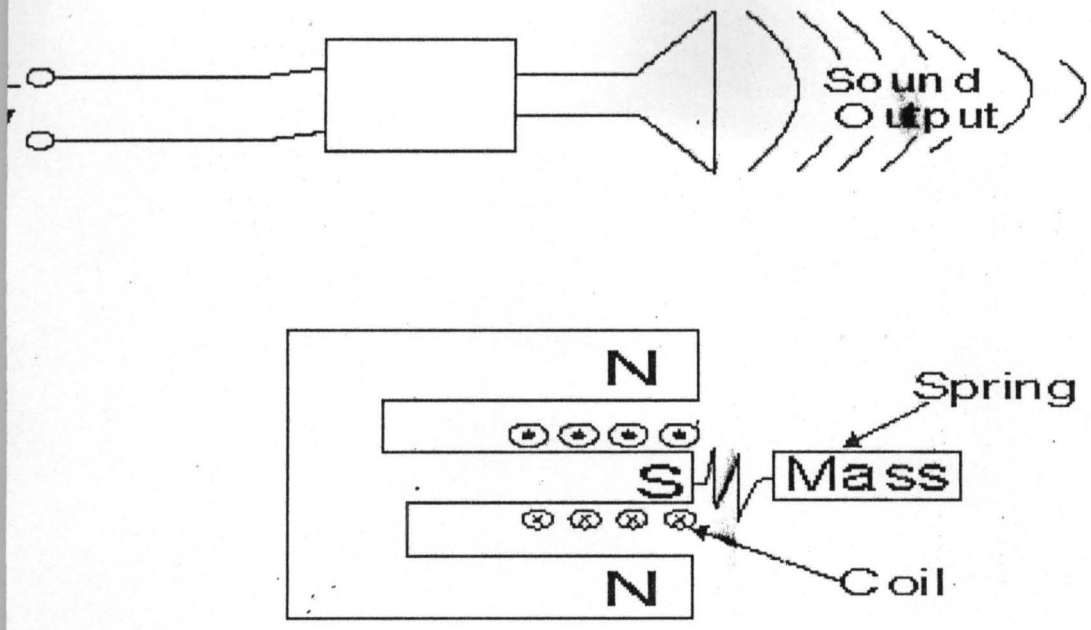


Fig. 3.91: Loudspeaker and its longitudinal section.

5 Power Supply Unit.

All the stages described, will not operate unless suitable means of D.C power supply available and applied appropriately to various required stages.

The most portable and available source of D.C power supply is dry cell battery. On other hand, batteries are proving to leakages over the time, that is, their emf is not ually constant overtime. Therefore, the cheap alternating power supply (A.C 240V, Hz) used is described as follow.

5.1 Transformer Calculation

The transformer used steps down from 240v to 12v basically for bridge tifications.

Turn ratio; $\frac{N_1}{N_2} = \frac{E_1}{E_2} = \frac{240}{12} = 20:1$

3.5.2 Bridge Rectification Design

D_1 to D_4 should be able to carry current = 3/2 = 1.5.

Since two diodes conduct at a time (for either positive or negative cycle of the supply). The peak inverse voltage (PIV) of the diode must be greater than the peak value of the output voltage at the secondary, that is PIV > (12X 2), PIV > 17.0

IN4001 is preferred for D_1, D_2, D_3 and D_4 of the bridge or their package. Since it PIV is even greater than 17V.

3.5.3 Filter Design

The filter capacitor is chosen to provide acceptably low ripple voltage, with voltage rating sufficient to handle the worse-case of no load and high line voltage.

Vp (Peak voltage at the secondary terminal) is

$$= V_{rms} \times \sqrt{2}$$

$$= 12 \times \sqrt{2}$$

$$= 17V$$

The diode forward drop V_D = 0.64 (for silicon) and f = 50Hz. However, the require input DC voltage should be such that V_{dc}. 12V and Vdc < that is $12 < V_{dc} < 17V$.

Selecting in the range, V_{dc} = 13v.

C_1 and C_2 are calculated using equation 1.0

$$C = \frac{V_{dc}}{4f_r R_L (V_{ip} - V_{dc.})}$$

$$V_{ip} = Vp - V_D$$

$$= \frac{13}{4 \times 50 \times 16 \,(\, 17 + 0.6 - 16).}$$

$$= 0.00290$$

$$= 29.0 \times 10^{-4} = \cdot 2900\mu F$$

So C_1 and C_2 were chosen to be 222μF and 220V respectively.

included in the power is the 9V DC source which serves as back up for PHCN er failure

This battery source has many advantages and disadvantages which have been ıssed above in this subsection of power pack.

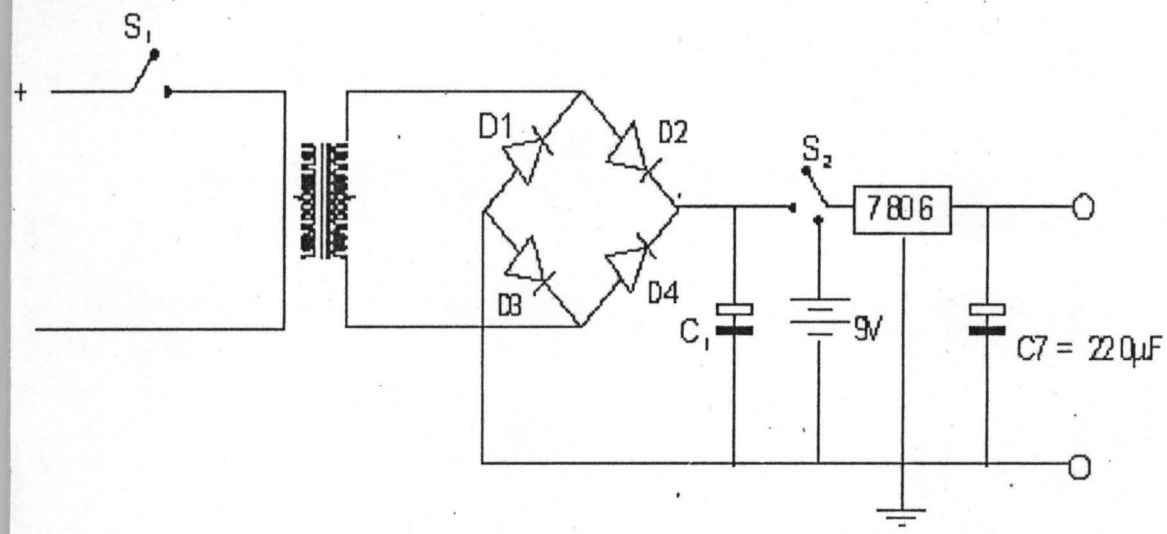


Fig. 3.92: Power Supply Unit

LEDs Driver Circuit

Light emitting diodes (LEDs) are good devices to visually a high (1) or low (0) al state. A typical red LED will drop 1.7V cathode to anode when forward biased itive anode-to-cathode voltage) and will illuminate with 10 to 20mA flowing through the reverse- biased direction (Zero or negative anode-to-cathode voltage), the LEDs block current flow and not illuminate, because it takes 10 to 20m,A to illuminate a

LED, there is need to construct its own circuit, which is known as LEDs Driver circuit [8, 4, 3].

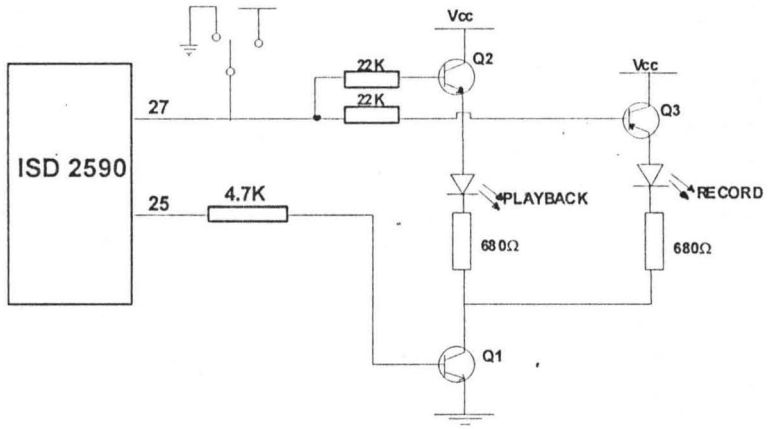


Fig. 3.93 LED drivers/Switching circuit.

LED Driver Calculation

Given values

$V_{cc} = 5V$

$V_{LED} = 1.4V$

$V_{CE\ sat} = 0.2V$

$Ic = 5mA$

$\beta = 55$

$$V_{cc} = Ic\,R_c + V_{LED} + V_{CE\ sat}$$

$$R_c = V_{cc} - V_{LED} - V_{CE\ sat}$$

$$I_c$$

$$= \frac{5 - 1.4 - 0.2}{5x10^{-3}} = \frac{3.4 \times 10^3}{5}$$

$$= 680\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{5mA}{55} = 0.09mA$$

$$R_B = \frac{V_{in} - V_{BE}}{I_B} = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{(5 - 0.7) \times 10^3}{0.09} = \frac{4.3 \times 10^3}{0.09}$$

$$= 47.8 \times 10^3$$

$$= 4.7K\,\Omega$$

For switching transistor Q_2 (NPN) and Q_3 (PNP), by applying a positive voltage from base to emitter (through the toggle switch being turned to play position) causes the collector to emitter junction to short (i.e. turning the transistor Q_2 ON and Q_3 OFF). While applying a negative voltage or 0V from the base to emitter cause the collector to emitter junction to open (turning the transistor Q_2 OFF and Q_3 ON). This is achieved by switching to Record position of the toggle switch [7].

For Q_2 and Q_3; $I_E = I_C Q_1 = I_C Q_3 = 5mA.$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 5 - (5 \times 10^{-3} \times 680)$$

$$= 1.6v.$$

For good switching; at low V_{CE}, β is as also low as 25

Therefore, $I_B = I_{E/\{\beta+1\}} = 5mA/26 = 0.2mA = 20\mu A$

$$R_B \text{ For } Q_2 \text{ and } Q_3 = \frac{V_{BB} - V_{BE}}{I_B} = \frac{5 - 0.7}{20 \times 10^{-5}} = 21.5k = 22k\Omega$$

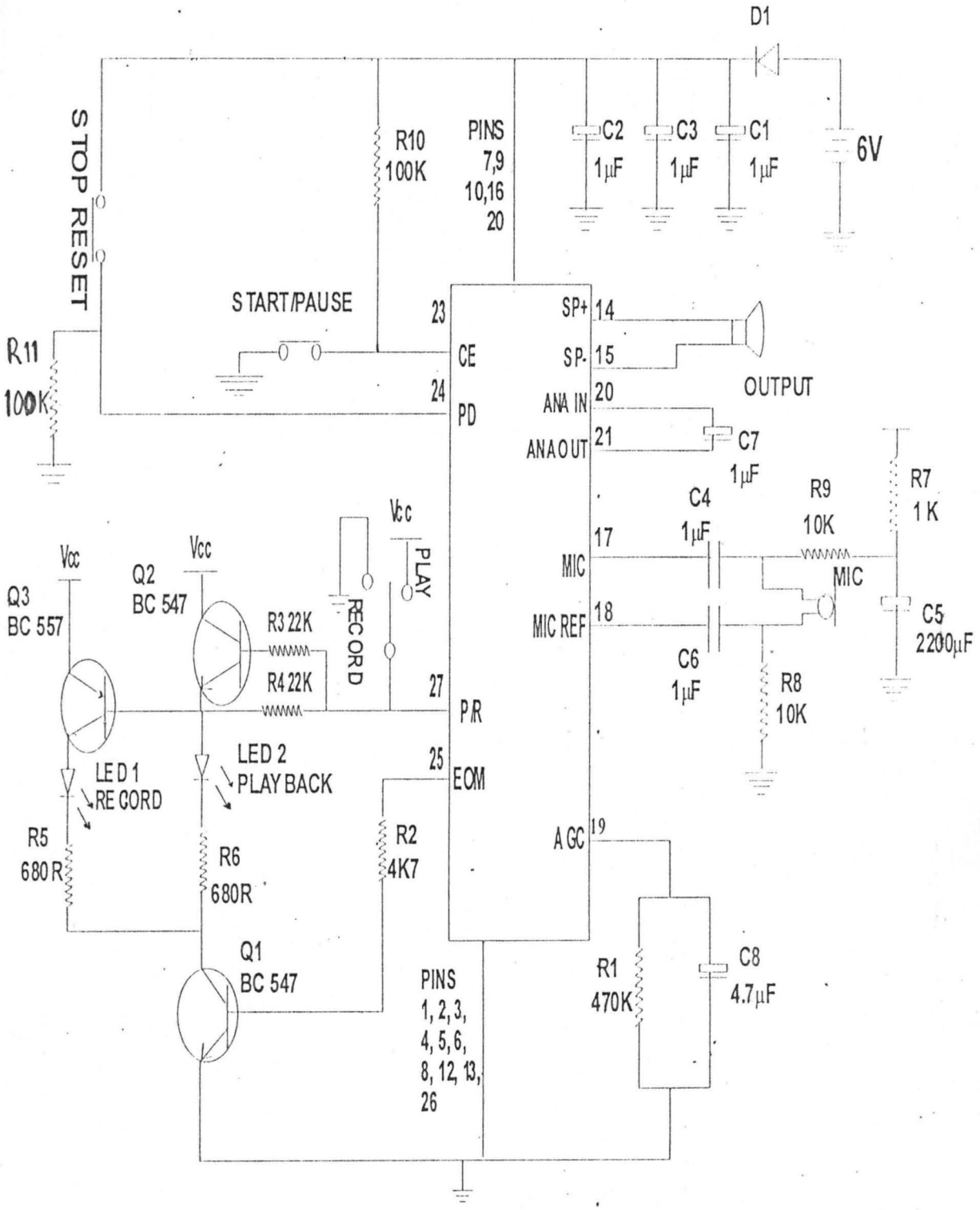


Fig. 3.93: Circuit Diagram of the Recording / Playback Device

CHARPTER FOUR

) PRINCIPLE OF OPERATION, RESULT AND DISCUSSION OF RESULT

1 Operational Mode Description

The available operational modes are described below. The mode can be used in njunction with microcontroller, or they can be hardwired to provide the desired system eration.

1.1 M0-Message Cueing

It allows the user to skip through messages, without knowing the actual physical dress of each message. Each CE LOW pulse causes the internal address pointer to skip the next message. This mode should be used for play back only, and is typically used ith M4 operational mode.

1.2 M1-Delete EOM Markers

This mode allows sequentially recorded messages to be combined single message ith only one EOM marker set at the end of the final message. When this operational is nfigured, messages recorded sequentially are played back as one continues message.

1.3 M2 Unused

is is an unused mode, when operational modes are selected, the M2 pin should be low.

1.4 M3- Message Looping

This mode allows for automatic continuously repeated play back of the message cated at the beginning of the address space. A message can completely fill this device d will loop from beginning to end without OVF going low.

.5 M4- Consecutive Addressing

During normal operations, the address pointer will reset when a message is played rough to an EOM markers. The M4 operational mode inhibits the address pointer reset EOM, allowing messages to be played back consecutively.

1.6 M5- CE Level Activated

The default mode for this device is for CE to be edge –activated on play back and vel record. This mode causes the CE pin be interpreted as level activated as opposed to ge activated during playback. This is specially useful for terminating playback eration using the CE signal

In this mode CE LOW begins a playback cycle, at the beginning of the device emory. The play back cycle continues as long as CE is held LOW. When CE goes IGH, playback will immediately end. A new CE LOW will reset the message from the ginning unless M4 is also HIGH.

1.7 M6- Push Botton Mode.

This mode is used primarily in very low cost applications and is designed to inimize circuitry and components, thereby reducing effective system cost. In order to nfigure this device in Push –button operation mode, the two most significant address ts must be HIGH, and the M6 mode pin must also be HIGH.

A device in this mode always powers down at the end of each playback or record ter CE goes HIGH.

When this operational mode is implemented, several of the pins on this device ternate functionality.

2 Operation Control Signal

2.1 CE Pin (Start / Pause)

In push button operational mode, CE acts as a LOW–going pulse activated TART/PAUSE signal. If no operation currently in progress, a LOW–going pause on this ignal will initiate a playback or a record cycle according to the level on the P/R pin (play IGH, record low signal)

A subsequent pulse on the CE pin, before an End – Of – Message is reached in ayback or an overflow condition occurs, will cause the device to pause. The address ounter is not reset, and another CE pulse will cause the device to continue the operation om the place where it was paused

2.2 PD Pin (Stop Reset)

In this mode employed, PD acts as a HIGH–going pulse activated STOP/RESET gnal. When a playback or record cycle is in progress and a HIGH going pulse is bserved on PD, the current cycle is terminated and the address pointer is reset to address the beginning of the message space.

2.3 P/R Pin (Playback / Record)

In order to initialize the playback cycle, a HIGH–going Pulse must be applied to . On the other hand, a low going LOW–going applied to the input pin will start a Record ycle.

2.4 EOM Pin (Run)

In Push–Button Operation Mode, EOM because the active HIGH RUN signal hich can be used to drive LED or other external device. It is HIGH whenever a record r playback operation is in progress.

.3 Recording Operation

The recording operation can be described by the machine code operation.

.3.1 Machine Code Operation (Recording)

i) The PD should be low, usually using a pull down resistor.

ii) The P/R is taken LOW

iii) The ĆE pin is pulsed LOW, Recording, starts; EŌM goes HIGH to indicate an operation in progress.

iv) The ĆE pin is pulsed LOW Recording pulses, EŌM goes back LOW. The internal address pointers are not cleaned, but an EOM marker is stored in memory to point to the message end. The P/R pin may be taken HIGH at this time. Any subsequent CĒ would start a playback at address O.

v) The CĒ is pulsed LOW, Recording start at the next address after the previous EOM marker. EŌM goes back HIGH. (If the M1 Operation mode pin is also HIGH, the just previously written EOM bit is erased, and recording starts at that address).

Vi) When the recording sequences are finished, the final CĒ pulse LOW will end the last record cycle, leaving set EŌM markers at the message end .Recording may also be terminated by a HIGH level on DP, which will leave a set EOM marker.

.4 Playback Operation

.4.1 Machine Code Operation (Playback)

i) The PD pin should be LOW

ii) The P/R pin is taken HIGH

i) The $C\bar{E}$ pin is pulsed LOW. Playback starts; $E\bar{O}M$ goes HIGH to indicate an operation in progress.

v) If the $C\bar{E}$ pin is pulsed LOW or an $E\bar{O}M$ is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $E\bar{O}M$ goes back LOW. The P/R pin may be changed at this time. A subsequent record operation would not reset the address pointer and the recording would begin where playback ended.

) Playback continues as n step 4 and 5 until PD is pulsed HIGH or overflow occurs.

i) $C\bar{E}$ is again pulsed LOW. Playback start where it left off, with $E\bar{O}M$ going HIGH to indicate in progress.

ii) If in overflow, pulling $C\bar{E}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address O.

5 Construction, Test and Result

During the first stage of design, the project was mounted on the breadboard and some ts were carried out, the whole design was later transferred onto the Vero board so far aim and objective of the project has been achieved, and then the final test was carried t.

All the results recommended by the manufacture and the experimentally obtained es discussed in a tabular and graphical form below.

4.5.1 Operation Conditions Result

Conditions	Manufacturer Recommendation	Values experimentally Obtained
Supply voltage V_{ss}	+ 4.5v to +5.5v	5.4v
Ground voltage V_{ss}	0v	0v
Operating temperature	0°C to 70°C	28°C
Storage temperature	- 65°C to 150°C	29°C
V_{cc} - V_{ss}	- 0.3v to +7.0v	6v
Voltage applied to any pin (Input current<+22mA)	(V_{ss} – 1.0v) to (V_{cc} +1.0v)	

Table 4.1: Operating conditions result.

4.5.2 DC Parameters Result

Symbols	Parameters	Manufacturer Recommendation	Values experimentally Obtained
V_{IL}	Input low voltage	0.8v	
V_{IH}	Input High voltage	2.0v	
V_{OL}	Output low voltage	0.4v	
V_{OH}	Output High Voltage	V_{CC} - 0.4V	5.6V
I_{CC}	Operating Current	25mA -30mA	23mA
I_{SB}	Standard	(1 – 10) μA	1 μA
T_{IL}	Input leakage current	+ μA	
R_{EXT}	Output head Impedance	16Ω	16Ω
R_{MIC}	Preamp Input resistance	(4 – 15) KΩ	9kΩ
R_{AUX}	Aux Input Resistance	(5 – 20) KΩ	11 KΩ

AC Parameters Result.

bol	Characteristic	Manufacturer Recommendation	Value experimentally Obtained
	Sampling Frequency	5.3kz	
	Filter pass band	2.3kz	
	Recording Duration	8901 – 93.0s	90.0s
Y	Playback duration	8701 – 93.0s	90.0s
	CE Pulse width	100n sec	
	Control/Address set up time	300n sec	
LD	Control/Address Hold time	O n sec	

Table 4.3: A.C Parameter Results

5.4 ISD Current Pin Destinations and Name

N	PIN NAME
)	Address 0
1	Address 1
2	Address 2
3	Address 3
4	Address 4
5	Address 5
6	Address 6
7	Address 7
8	Address 8
9	Address 9
ux IN	Auxiliary Input
$_{ss}$D	V_{ss} digital Power Supply
$_{ss}$A	V_{ss} Analog Power Supply
P+	Speaker Output +
P-	Speaker Output -
$_{cc}$A	V_{cc} Analog Power Supply
IC	Microphone Input
IC REF	Microphone Reference
GC	Automatic Gain Control
NA IN	Analog Input

NA OUT	Analog Output
VF	Overflow Output
E	Chip Enable Input
D	Power Down Input
OM	End Of Message
CLK	No Connection(optional)
/R	Playback/Record
$_{cc}$D	V_{cc} Digital Power Supply

.5.4 Timing Diagram Result

The timing diagrams obtained from oscilloscope for both record and playback ith manufacturer accompanying timing diagram for both operations are shown in gures below.

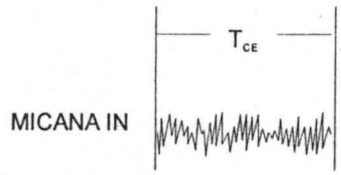


Fig. 4.1a: recording timing diagram as drawn from oscilloscope.

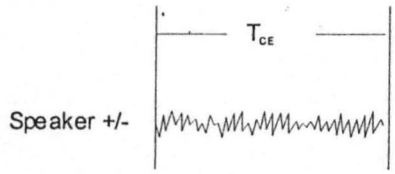


Fig. 4.2a: playback timing diagram as drawn from oscilloscope.

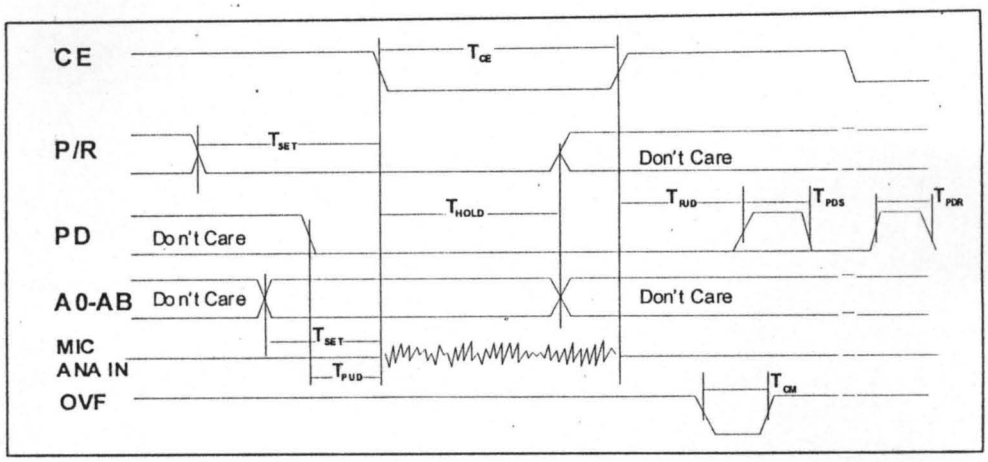


Fig. 4.1b: manufacturers accompanied record timing diagram

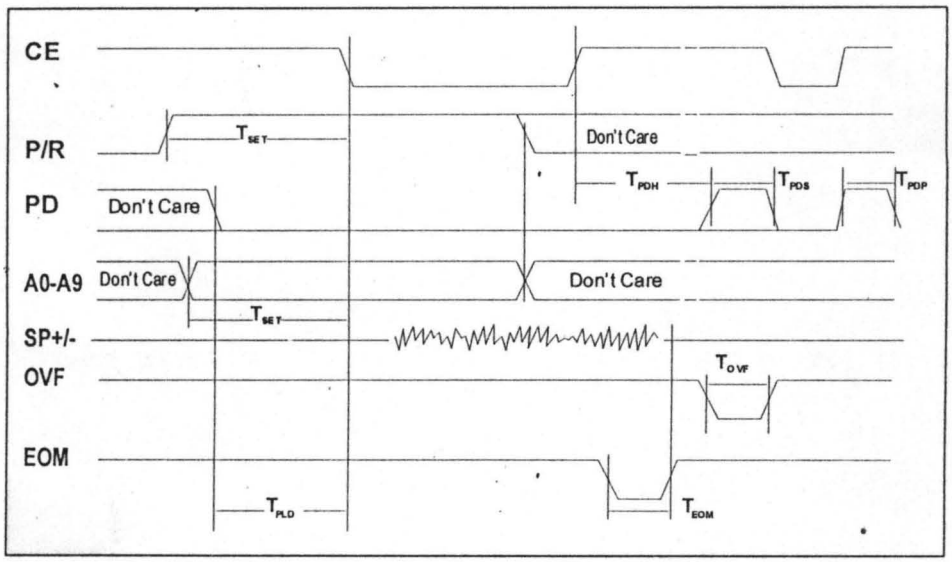


Fig. 4.2b: manufacturers accompanied playback timing diagram

Limitation

The mechanical mode of recording (magnetic cassette or disc type) has a greater ntage over this integrated circuit types in this area of limitation, where both rding and playback can be do done simultaneously. This is due for the fact that the rated circuit design lacks two output buffers that playback the audio-recording m simultaneously as it is recording.

.6 Casing and Measurement

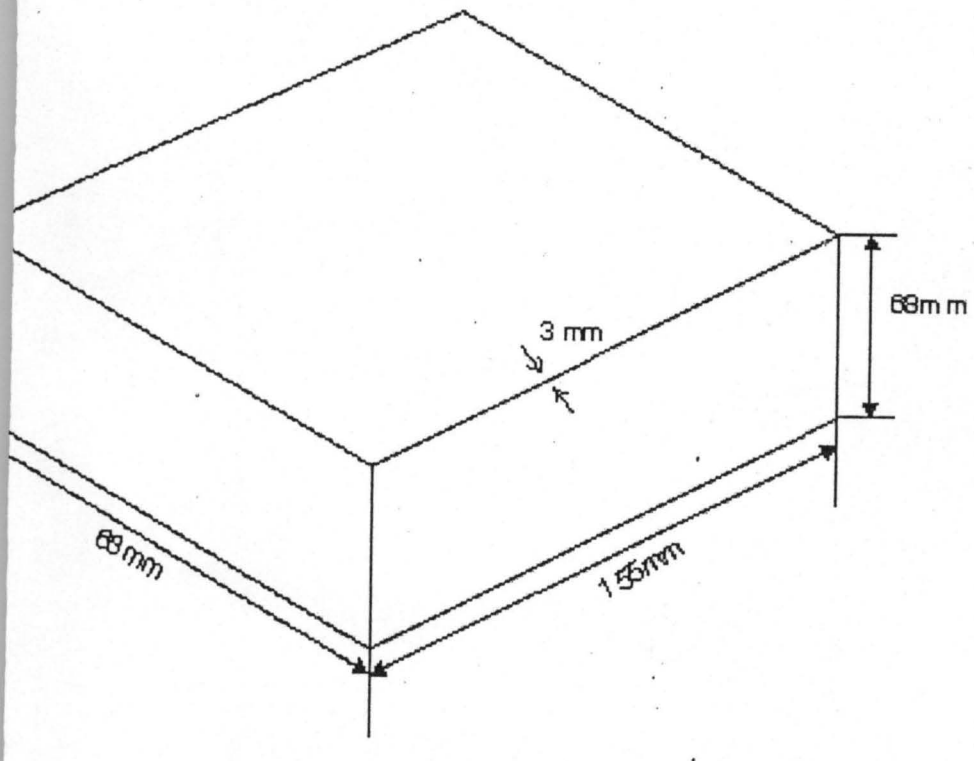
In this construction, the ISD2590 IC, the power pack and all other passive nponents are all enclosed in a very portable wooden-material for the ease of carrying ut, and the dimensions are given below;

ckness = 3mm

ngth = 155mm

adth = 68mm

ight = 36mm



4.5.7 Passive Component Function

The various functions of the passive circuit components are as summarized below:

PART	FUNCTION	COMMENTS
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant.	Sets release time for AGC
R3, R4	Microphone biasing resistors	Providing biasing for microphone operation
R5	Series limiting resistor	Reduces level to prevent distortion at higher voltage supply
R6	Series limiting resistor	Reduces level to high supply voltages.
C1, C5	Microphone DC-blocking capacitor low frequency cut-off	Decouple microphone bias from chip, provides single pole low-frequency cut-off and common mode noise rejection.
C2	Attack/release time constant	Sets attack/release time for AGC
C3	Low-frequency cut-off capacitor	Provides additional pole for low frequency cut-off.
C4	Microphone power supply decoupling	Reduces power supply noise.
C6,C7,C8,C9,C10	Power supply capacitors	Filter and by-pass of power supply

TABLE 4.5: Passive Function Components

CHAPTER FIVE

CONCLUSION AND RECOMMENDATIONS

Conclusion

A recording/playback device makes use of the latest technology in digital storage ces. It stores digitally, a sound signals inputted from a microphone (already erted to electrical signals) and after recording duration, playback the recorded sage in an audible form.

The users must shield the device from unnecessary environmental noise especially ng operation. Also, all other precautions associated with electronic devices must be ngly observed.

Furthermore, there is no need for power supply in order to keep the message d in the IC memory stored or not losing it, because the device provides zero-power sage storage.

Recommendations

There is need for improvement in all areas of work. The full application potentials is project can be realized if this design is improved to be microcontroller compatible. will allow complex messaging and improve efficiency.

Also, more recording time can be achieved by cascading several ISD chips nlessly, adhering to the manufacturers' technical specifications.

Furthermore, two output buffers could be incorporated for effective functioning of device. In the sense that one of the buffers playback the recording sound ltaneously as it is being recording while the other one holds the data on the semi luctor's memory

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QUICK OPERATIONAL MANUAL REFERENCE

1. Plug the power cord to source of electricity (socket) or switch to battery source
2. To record switch record/playback button to record position, press the start button and put the microphone very close to the mouth but not touching it. The user has 90 seconds to record.
3. To playback switch record/playback button to playback position and then press start button. In case of many messages, to select, just press the start pause button. The number of press is equivalent to the message number selection.