DESIGN AND CONSTRUCTION OF AUTOMATIC LAN CABLE TESTER

BY

OTULUGBU BENOR

2003/15344EE

A THESIS SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

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ATTESTATION /DECLARATION

I, Otulugbu Benor declare that this project was done by me and has never been presented elsewhere for the award of Bachelor degree. In this regard I am tendering this thesis copy to the Department of Electrical and Computer Engineering of Federal University of Technology, Minna.

Otulugbu Benor	Engr. J.G. Kolo
....	....
(Name of student)	(Name of supervisor)
14/11/08	....
(Signature and date)	(Signature and date)
Engr. Dr. Y.A. Adediran	
....	....
(Name of H.O.D)	(Name of External Examiner)
....	....
(Signature and date)	(Signature and date)

DEDICATION

This project is greatly dedicated to God Almighty who has made it possible for me to the completion of this project without much agony. I also wish to dedicate this project to my parents Mr. & Mrs. Otulugbu and family for making themselves available for God's use upon my education.

ACKNOWLEDGEMENT

In the name of God most gracious, most merciful, thanks to God for everything. I want to thank my supervisor Engr. J.G. Kolo for the help, assistance, and motivation he provided me during the time of this project. Also, my appreciation goes to my parents, Mr. M.C. Otulugbu and Mrs. Queen Otulugbu for their prayers, love, care and provision to me from my day one on earth to this present time. I wish to express my sincere gratitude to all members of my family for all their financial support despite the very economic indices of the country.

I would not forget my friends, Ebikefe George, Ben Haruna Omijie, Abdul Kadir, and my baby girl Promise Akuwudike, just to mention a few, I love you all. My special thanks also go to my H.O.D, Dr. Y.A Adediran who would not stop to put me to work with his advice every Friday to see that this project is finished on time, God bless you sir. My special thanks to Chris for his contribution and assistance during the construction, God will finish that which he has started on you.

ABSTRACT

This project is a continuity tester which tests a computer networking cable for the correctness and continuity of the cable type. The networking cable aids the connection of similar, dissimilar and Cisco devices for the sharing and transfer of data between one and the other. The project is designed with the use of micro processor as the main processor unit of the work. It processes the input signal of the cable and gives an output on a 7 Segment based on the processed signal. Other components that are put together to make this project achievable are resistors, reset button, RJ-45 jack, crimping tool, capacitors, crystal oscillator, normally open switc

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CHAPTER ONE

1.1 INTRODUCTION

In the distance past, almost all paper works such as file sharing/transfer are done manually, but these days most paper works has being taken over by an electromagnetic device called computer. Computer has done an extensive work in document sharing via network. A network is a connection of two or more computers for the purpose of sharing information, resources, etc intelligently together, such as a scanner or printer, exchanges files and enable electronic connectivity.

Basically the connection of computers to share information and resources is done through a cable known as network cable. Networking cables are data transmission cables and are used to connect one network to another. These cables enable high speed data transfer between different components within the network. The network cables are of different types that needed to be crimped differently based on their plug type. Some of these cable are the 10 base 2, 10 base T, RJ-45(straight, crossed, rolled), RJ-11, DB connector, etc. among all these, the one that is mostly used is RJ-45.

The necessity of network has come to stay especially in information technology and communication service. Telecommunication applications are widely spread, ranging from global network to local telephone exchange to subscribers homes to desktop computers. These involves the transmission of voice data or video over specified distances of less than a meter to hundreds of kilometer, using one of a few standard fiber designs in one of several cable designs, which can be of a local area network (LAN).

A LAN is a group of interconnected computers that span a relative small area within which each individual node can execute its program locally i.e. within the same network while also being able to access data and device anywhere on the LAN (subject to security access parameters). For instant, use of workgroup LANs has been a major factor in improving the productivity and efficiency of individual users by enabling them to interact, exchange information and to share expensive resources, such as laser printers disk arrays etc.

LANs are capable of transmitting data at very fast rates; much faster than data can be transmitted over a telephone line but the distances are limited and there is also a limit on the number of computers that can be attached to single LAN. Most LANs are confined to a single building or groups of buildings. However, an individual LAN can also be connected to many other LANs over any distance via routes using telephone lines and radio waves. A system of LANs connected in this way is typically called wide area network (WAN). The geometry arrangement of devices on the network for example, device can be arranged in a bus or a ring or a star topology.

Protocols: the rules and the encoding specification for transferring data. It is the protocol that determines if the network uses point to point or client/ server architecture.

1.2 Motivations

Design and construction of an Automatic LAN cable tester is very essential in networking organization either newly built or existing network. A network administrator will find it very easy to implement when he has to connect and trouble shoot as many computers as possible.

1.3 Aims and Objectives

This project is designed to serve as a troubleshooting device in any networking environment. The tester is designed to safe a great deal of time in testing the continuity of a networking cable without going through the manual process.

1.4 Methodology

The design and construction of this device was done base on the concept of a network tester that uses light emitting diodes to indicate the type of cabling, while this project make use of microcontroller as the main component and indicate the result on a seven segment display. The tester device that will be described in this project is a basic continuity tester rather than a performance issue resolution. However, it work as a basic continuity tester for any standard UTP/RJ-45 cable as used in an Ethernet installation.

CHAPTER TWO

LITERATURE REVIEW

2.1 HISTORIC BACKGROUND

Network and networking have grown exponentially over the last 15years. Understandably so, they have had to evolve at high speed just to keep up with huge increases in basic missions critical uses needs, such as sharing data and printers as well as video conferencing. Most times, clients need to share networking resources in a location within the same office area which is a common situation today and as a result poses challenges in the field of computer networking.

The need to test LAN cables efficiently, effectively and most imperatively trouble shooting its functionality for the very dynamic connections of desperate systems together has been on the increase, not until in the late year 2000 that engineers were able to make a break through in the field of computer networking technology. However, the earlier cable tester and its networking solution were having some limitations such as the portability, power consumption etc.

The technology on LAN cable kept improving years after year, not until some few years back that a LAN cable tester that uses LED as indicator to detect the continuity of a network cable. This tester was not too portable but does the functionality of which it was designed for. Today we have various kind of networking cable tester with different kind of functionality. For instance, some of them can test for RJ/11 alone, some can test for RJ/45 alone while other can test for both RJ/11 and RJ/45.All of these uses LEDs as their continuity test indicator.

2.2 LAN CABLE STANDARDIZATION

2.2.1 ETHERNET

The institute of electrical and electronics engineering (IEEE) has defined and document a set of standard for the physical characteristic of both collision-detection and Token-passing networks. These standard are known as 802.3 (Ethernet and IEEE 802.5 (Token-Ring)). IEEE 802.11b defines a wireless version of Ethernet. The Ethernet is a standard that makes LANs in a group to communicate intelligently together and with millions of computers connected by Ethernet cards and cables through a network called WANs.

Ethernet has since becomes the most widely used date link protocol in the world today and as result, Ethernet based LANs enable you to interconnect a wide variety of equipment including UNIX and LINUX workstations, Apple computers, printers, and PCs. You can buy Ethernet adapters from dozens of completing manufacturers, supporting all three of the cable types defined in the standard, thinnet, thicknet, and unshielded twisted pair(UTP).

Basicaly, Ethernet operates at a speed of 10Mbps. But the most recent (and most popular of the Ethernet flavors is Fast Ethernet standards which pushes this speed to 100Mbps. The latest version Gigabit Ethernet, reaches speeds of 1000Mbps, or 100times the speeds of original Ethernet,

2.2.2 FAST ETHERNET

Fast Ethernet requires adapters, hubs and UTP or fiber optic cables design to support the higher speed, but you can get combination devices that run at both 10Mbps and 100Mbps enabling the gradual upgrading of network by installing new NICs and hubs over an extended period of time. Both the most popular form of fast Ethernet (100base-TX) and 10base-T standard

Ethernet use two of the four wire pairs found in UTP category 5 cables. An alternative Fast Ethernet standard called 100base-T4 uses all four wire pairs in UTP category 5 cables, but this fast Ethernet standard was never popular and is seldom seen today.

2.2.3 GIGABIT ETHERNET

Gigabit Ethernet also requires special adapters, hubs and cables. Most users of Gigabit Ethernet use fiber-optic cables, but can run gigabit Ethernet over the same category 5 UTP cabling that Fast Ethernet is used band Gigabit Ethernet is also referred to as 100base-T.

Unlike Fast Ethernet, Gigabit Ethernet uses all four wire pairs. Thus, Gigabit Ethernet requires dedicated Ethernet cabling. You can't borrow two wires pairs for telephone or other data signaling with Gigabit Ethernet as you can with the slower forms because Most Gigabit Ethernet adapters can also be UTP-based form of Ethernet on a single network. Neither fast Ethernet nor Gigabit Ethernet supports the use of thin or thick coaxial cable and traditional Ethernet can also be interconnect with UTP-based Ethernet network by using media converters or specially designed hubs and switches.

2.3 NETWORK ADAPTERS CONNECTOR

Ethernet adaptor typically have a connector that cooks like a large telephone jack called an RJ-45 (For 10base-T and Fast Ethernet twisted–pair cables), a single BNC connector(For thinnet coaxial cables). A few older 10Mbps adaptors have a combination of two or all three connector type; adaptors with two or more connectors are referred to as combo adaptors. Token-Ring adaptors can have a 9-pin connector called a DB 9(for type 1 STP cable) or sometimes an RJ- 45 jack(for type 3 UTP cable)

2.4 NETWORK CABLES

Originally all networks use some type of cables to connect the computers on the network to each other. Although various type of wires are now in the market and most office and home network are still based on one of the following topologies;

- Coaxial cable
- Twisted- pair cable

2.4.1 THICK AND THIN ETHERNET COAXIAL CABLE

The first version of Ethernet was based on coaxial cable. The original form of Ethernet 10 base-5, used a thick coaxial (called thicket) that was not directly attached to the NIC. A device called an attachment unit interface (AUI) ran from a D815 connector on the rear of the NIC to the cable. The cable had a hole drilled into it to allow the "Vampire tap" to be connected to the cables. NIC designed to use with thick Ethernet cable are almost impossible to find as new hardware today.

Twisted- pair is just what its name implies insulated wires within a protective casing with a specified number of twists per foot. Twisting the wires reduces the effect of electromagnetic interference (that can be generated by near by cables, electric motors and florescent lighting) on the signal being transmitted. They are of two types namely:

- shielded twisted pair and
- Unshielded twisted pair).

The shielded twisted pair (STP) refers to the amount of insulation around the cluster of wires and therefore it's immunity to noise. It is commonly used in Ethernet network today. Unshielded twisted –pair (UTP) Cable is often used for telephone wiring

2.4.2 NETWORK CABLE TYPES AND TOPOLOGIES

A LAN is a group of interconnected computers, that span a relatively small area within which each individual computer node can execute its own program locally i.e within the same network while also being able to access data and device any where on the LAN(Subject to security access parameters). For instance, the use of workgroup LANs has been a major factor in improving the productivity and efficiency of individual users by enabling them to interact, exchange information and to share expensive resources, such as laser printers, disk arrays etc.

LANs are capable of transmitting data at very fast rates, much faster than data transmission over a telephone line, but the distances are limited and there are also a limit on the number of computers that can be attached to a single LAN. Most LANs are confined to a single building or group of buildings. However an individual LAN can also be connected to many other LANs over any distance via routers using telephone lines and radio waves. A system of LANs connected in this way is typically called a wide area network (WAN)

There are many different types of LANs, and Ethernet being the most common for PCs. Most Apple Macintosh networks are based on Apple's Apple Talk Network system, which is built into Macintosh computers .Among the key characteristics that differentiate one LAN from another is:

- Topology: This is the geometric arrangement of devices on the network. For example, devices can be arranged in a bus, or a ring or a star.
- Protocols: Is the rules and the encoding specification for transferring data. It is the protocol that determines if the network uses pin-to-pin or client/server architecture.

  However, the tested device that will be described in this project is a basic continuity tester rather than a performance level test device which will proof a particular cable worthy for connectivity of systems together. It is intended to use as a troubleshooting tool for basic connectivity testing rather than for performance issue resolution. However it will work as a basic continuity tester for any standard UTP/RJ-45 cable as used in an Ethernet installation. This applies to cable assemblies made with either category 3 or 6 bulk cable.

2.5 THEORETICAL BACKGROUND

The basic theory behind this project was coined out from some previous project works. In one of the works, light emitting diodes serve as the display unit, by coming up one after the other which indicate a particular cable while in the other one a seven segment display was used to show the result.

A SIMPLE CABLE TESTER

The wire could either be a cat 3 or a cat 5 Shielded twisted pair (STP 8 wire) which are arranged in pair such that (pin1/pin2, pin 3/pin 4, pin 5/pin6, pin7/pin8), resulting to the use of 4 seven segment display. The circuit was designed so that when the end of a STP cable are plugged into each of the "RJ-45 socket", the circuit for each pair is completed and the seven segment will display the result. If there is a break in a wire (or the lead are incorrectly terminated) the corresponding seven segment display will not come on.

The other project that was constructed using the light emitting diodes, for sequential on/off of the LEDs, eight LEDs were used in this case. The basic difference between these two project and the one I am working on is the that this project can test for the three kind of cables and has a unique display in the sense that it will display my name, Auto LAN Cable tester and my matriculation number with a scrolling display for persistence of vision.

CHAPTER THREE

DESIGN ANALYSIS

3.1 INTRODUCTION

This chapter provides the technical details of the working principle and design of the automatic LAN cable tester. It would give an overview of the different circuits which form sub systems that make up the system, their description and how these circuits are interconnected to make up the LAN tester. These details would include system specifications and special features as provided in two major branches: Hardware, Microcontroller circuit: Interfacing circuits, power supply circuit, Seven Segment Display Circuit and Mechanical frame for support and strength.

3.2 DESCRIPTION OF THE LAN CABLE TESTER

The autonomous LAN cable tester is an embedded control system designed for the functionality of testing the continuity of a networking cable, the type of cable to be used and the type of devices to be connected together. It has two ports which when receive the two ends of a networking cable, displays the cable type on the Seven Segment. For the testing process, the device sends an 8-bit through one of the cable terminal and receives an 8-bit signal through the other port on which software for validating the continuity is running. After validation, the result is display on the Seven Segment.

3.3 HARDWARE

This comprises all the physical components of the LAN cable tester that can be felt and touched. Here all the design of the various circuits will be discussed in detail.

3.4 MICROCONTROLLER UNIT

This is the centre of intelligence of the LAN cable tester where all logical operations and control take place. This circuit is analogous to the brain of the system. At the core of this circuit is the Microchip AT89C51 microcontroller which has the following features:

- 40 pins
- 32 programmable Input / Output pins
- Compactable with MCS-51 products
- 8K bytes of In-system Reprogrammable flash memory.
- Endurance: 1000 write/Erase cycles.
- Full static operation; 0 Hz to 24 MHz
- Three level memory lock.
- 256 x 8 bits internal RAM
- Three 16-bit Timer/counters
- Eight interrupt sources-down mode
- Programmable serial Channel
- Low-power Idle and Power
- 4.0V to 5.5V Operating Range
- Interrupt Recovering from Power-down mode
- Watch dog Timer
- Dual data Pointer

• Fast Programming Time

• Flexible ISP Programming (Byte and Page mode

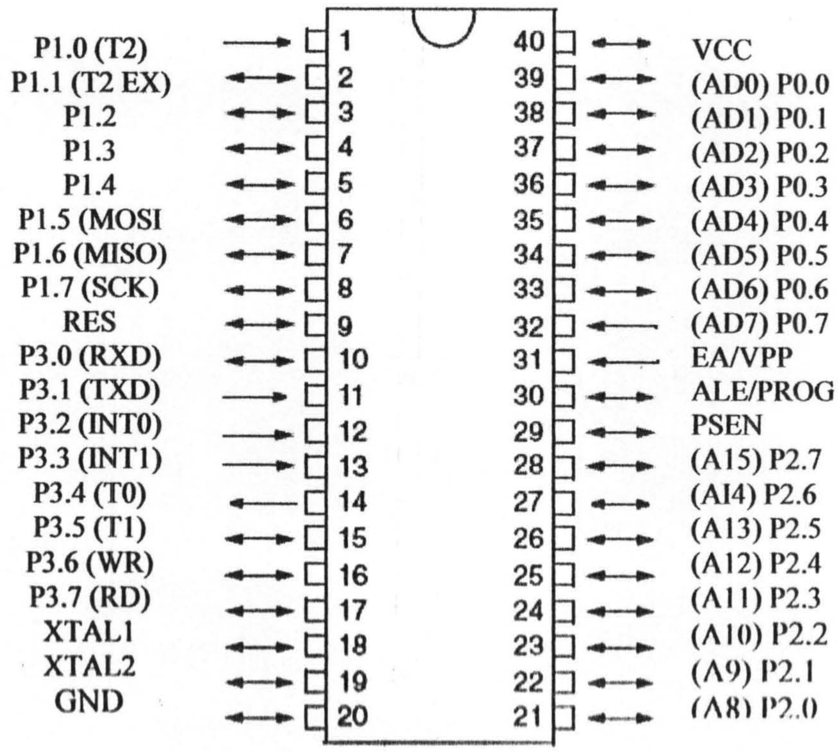


Figure 3.4.1 Pin Outs of the AT89C51 Microcontroller

The above listed features form the foundation for the selection of the AT89C51 over other microcontrollers from this vendor and other vendors.

Further supporting this selection are the following reasons:

- Of all the vendors of microcontrollers the documentations of microchip are most accessible to us and are also readily available
- The ease and speed of developing embedded systems on the Microchip
- The LAN TESTER is an embedded system which requires many input / Output pins and AT89C51 provides this numerous number of pins.
- Above all, the chip is readily available and affordable.

The microcontroller circuit is shown in figure 3.2 below.

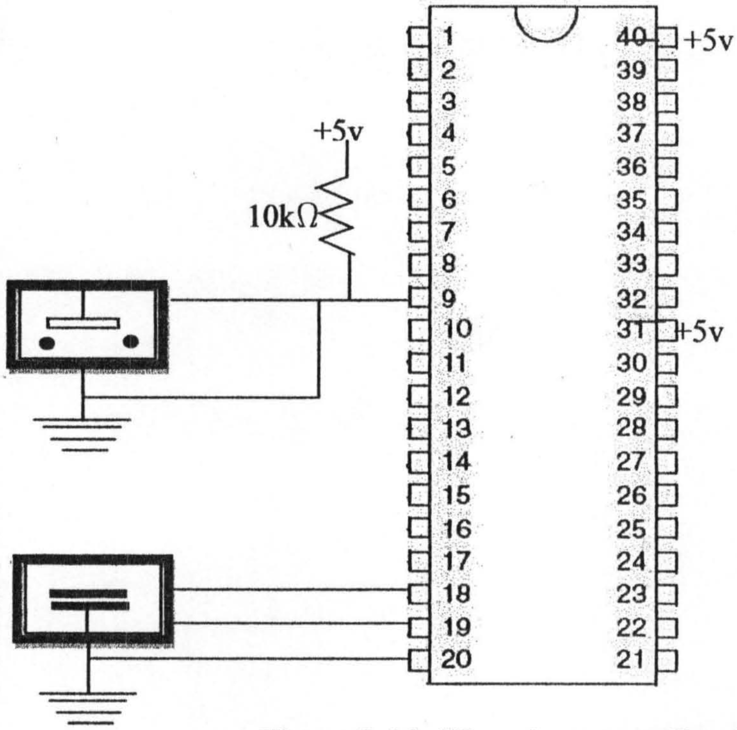


Figure 3.4.2: The microcontroller Circuit

The microcontroller is powered by a standard regulated 5V dc supply connected to pins 40 and 32. The pin 20 is the ground pins. The circuit uses 16MHz external crystal oscillator which provides the clock signal required for the execution of instructions by the microcontroller. This oscillator determines the speed of the microcontroller. The reset pin (pin 9) of the microcontroller is an active low and must be pulled up to VDD for the microcontroller to function properly. The reset button is a normally open push button which can be pulled to VSS to hard reset the chip.

The microcontroller begins to execute the embedded program as soon as power is supplied to the chip. The I/O pins serve as means of interfacing the microcontroller with the various type of networking cable.

3.5 INTERFACING CIRCUITS

Control and data signals from the various sub circuits can be inputted to or sent out from the microcontroller. The variations in the type of signals required for activating the various parts of the system and the need for compatibility with the microcontroller necessitates the use of interfacing circuits. Sub systems that require special interfacing circuits and their descriptions are in the following sub sections.

3.6 RJ-45 SOCKETS

The RJ-45 SOCKETS are 8-bit port that receives an input signal when CAT 5 networking cable is inserted into it, the signals are then processed by the microcontroller and the result is display on a seven segment. The RJ-45 is made up of 8-bit metal string, plastic material and an electronic circuit through which the interfacing of the RJ-45 SOCKET and the microcontroller is made possible.

3.7 CLOCK CIRCUITRY

The clock circuitry is made of a single component, a 16MHz crystal. This unit generates the clock pulse for the microcontroller to execute its instruction. The interfacing between the clock source and the microcontroller is shown above

3.8 POWER SUPPLY UNIT

The power supply was obtained from 9 v DC battery source since the device is design to be handy and portable. The power supply diagram is shown below in figure 3.8.1

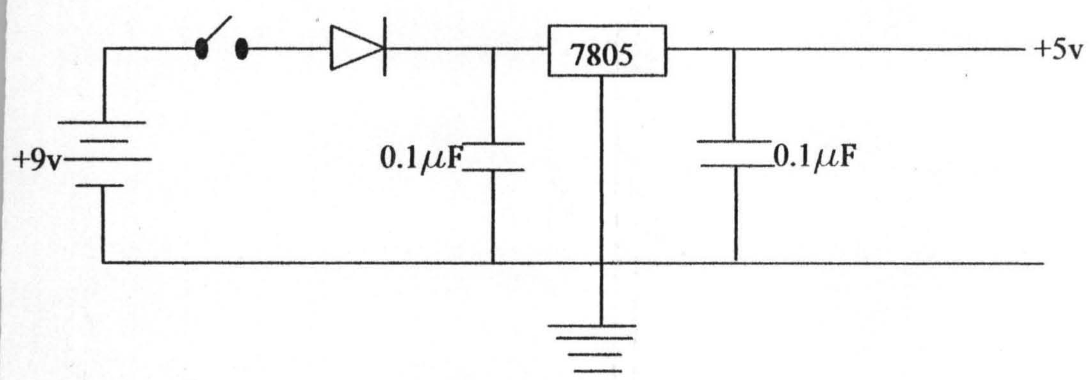


Fig 3.8.1 System power supply

3.8.1 POWER SWITCH

The power switch is a electronic switch which connects the 9v battery source to the power circuit and switches it off after testing or when necessary

3.8.2 THE DIODE

The diode is interposed in between the switch and capacitor to prevent polarity reversal which could damage the system.

3.8.3 FILTER CAPACITOR

Filter capacitor or smoothen capacitor, is placed before the voltage regulator. Smoothing is performed by a large value electrolytic capacitor connected across the DC supply to act as a reservoir, supplying voltage to a voltage regulator which consumes 3v out of the 9v from the power source and then give out 5v though a second smoothing capacitor. The diagram shows the unsmoothed varying DC (dotted line) and the smooth DC (solid line).

The capacitor charges quickly near the peak of varying DC, and then discharges as it supplies current to the output

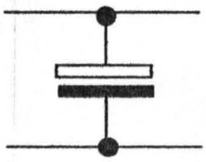


Fig 3.8.2 Filter capacitor

3.9 INPUT UNIT

The auto detection of cable was realized using the following steps;

- ✓ Test cable for 10Base T R/J45 cross connection
- ✓ Test cable for 10 Base T R/J45 straight connection
- ✓ Test cable for 10 Base T R/J45 True/rollover connection
- ✓ Test cable for 100 Base T R/J45cross connection
- ✓ Test cable for 100 Base T R/J45 straight connection
- ✓ Test cable for 10 Base T R/J45 true/rollover connection

If any of the cut fails the six steps above the system does not displays cable detected on the seven segments, otherwise cable detected is scrolled across the display. The 10 and 100 before the base T stand distance travel in mbps, while the Base T stand for base band technology. Basically 10 Base T uses 4 wires for connection and this wire are check for straight cable, swapped for cross while for true or rollover the whole 8 wires are used. End to End continuity by one:

- ✓ Making pin 1and 3 the input port (0FFH is written to both port)
- ✓ Clearing a pin on the master port (P 1)
- ✓ Checking for zero on the slave port. If a zero is detected on the slave port the subroutine move on to check the next pin interface to the cut.

Six routing were used, and the routing were assessed top down as shown below.

- ✓ 100 Base T straight Routine
- ✓ 100 Base T cross Routine
- ✓ 100 Base T true/rollover Routine
- ✓ 10 Base T straight Routine
- ✓ 10 Base T cross Routine
- ✓ 10 Base T true/rollover Routine

Each routine exits with a result if the cut satisfies. There in. Control is then transferred to a different potion of the code that causes a display of the result.

3.9.1 DISPLAY UNIT

This section focuses on the digital display when a continuity test is carried out on a cable. It consists of four seven segment display. The display was multiplex to save all the numerous number of wires needed to interface the segment to the controller. Multiplexing was done on a time slide allocation of the port of the common data port i:e the data to be displayed is placed on the common transmission path (P 0) for a period of time, the associated digit driver turn on briefly and off. Software control was involved in this basically, display multiplexing involved.

I. Switch off all digit drivers.

II. Placing the data to display on pin zero

III. Turning on the digit driver associated with display position

IV. Delaying for persistence of vision

V. Turning off the digit driver that was on in step III

VI. If the above code is executed frequently (greater than 5 time per seconds), there is illusion of vision in which the four digit comes on and off continuously but, in reality only a single digit is on at a particular time.

The display was interfaced to the controller with port zero (segment to dp), and the digit drivers over P 2

The display is shown in the fig 3.9 below.

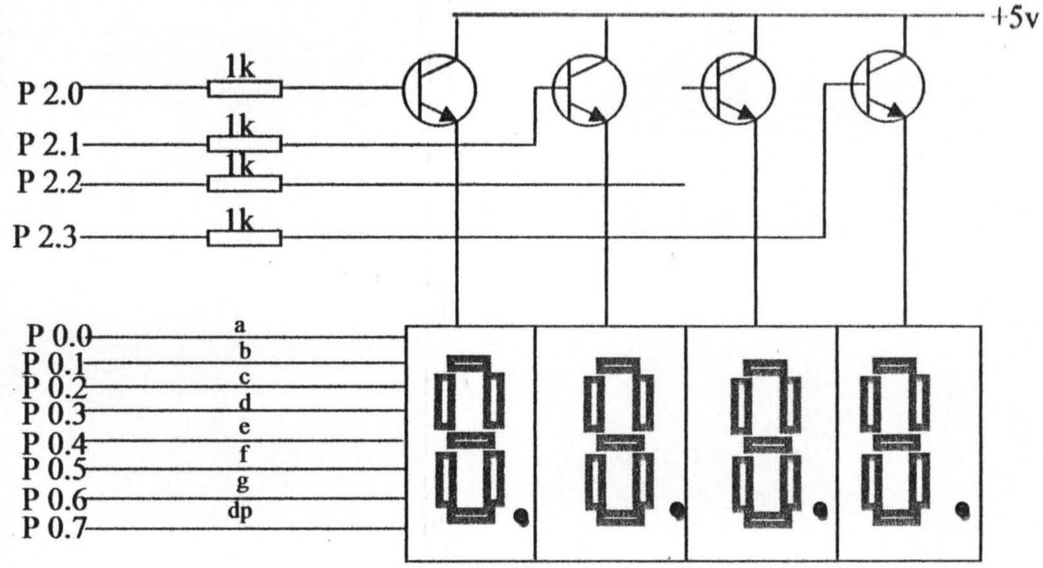


Fig 3.9 four digit visual display

T1-T4 controls the digit display positions. Clearing the port pin associated with a digit driver forward-bias the pnp transistor, sourcing current into the segments. A current return path is provided over P0 of the controller.

3.10 DESIGN CALCULATION

For an n-digit display, the current through each segment is n *IF where IF is the forward current through each segment. For a 10mA continuous segment current, a 4-digit system 40mA through each digit to produce the same brightness a 10mA segment current would (the 40Ma is pulsed in a multiplexed display).

For an 8-segment display, the peak current through the display is (8*40mA)= 320mA

.IC= 320Ma.

The gain of the digit drivers is typically 200,

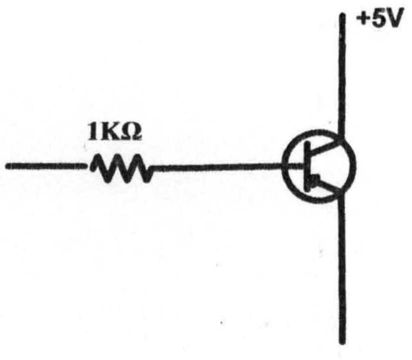
IB= IB/HFE= 0.32/200= 0.0016A

RB=VCC-VBE/IB= 5-0.7/0.0016

= 4.3/0.0016

= 2.7KΩ

A 1kΩ base resistance wasused toallow for a fairly brighter display.



CIRCUIT DIAGRAM

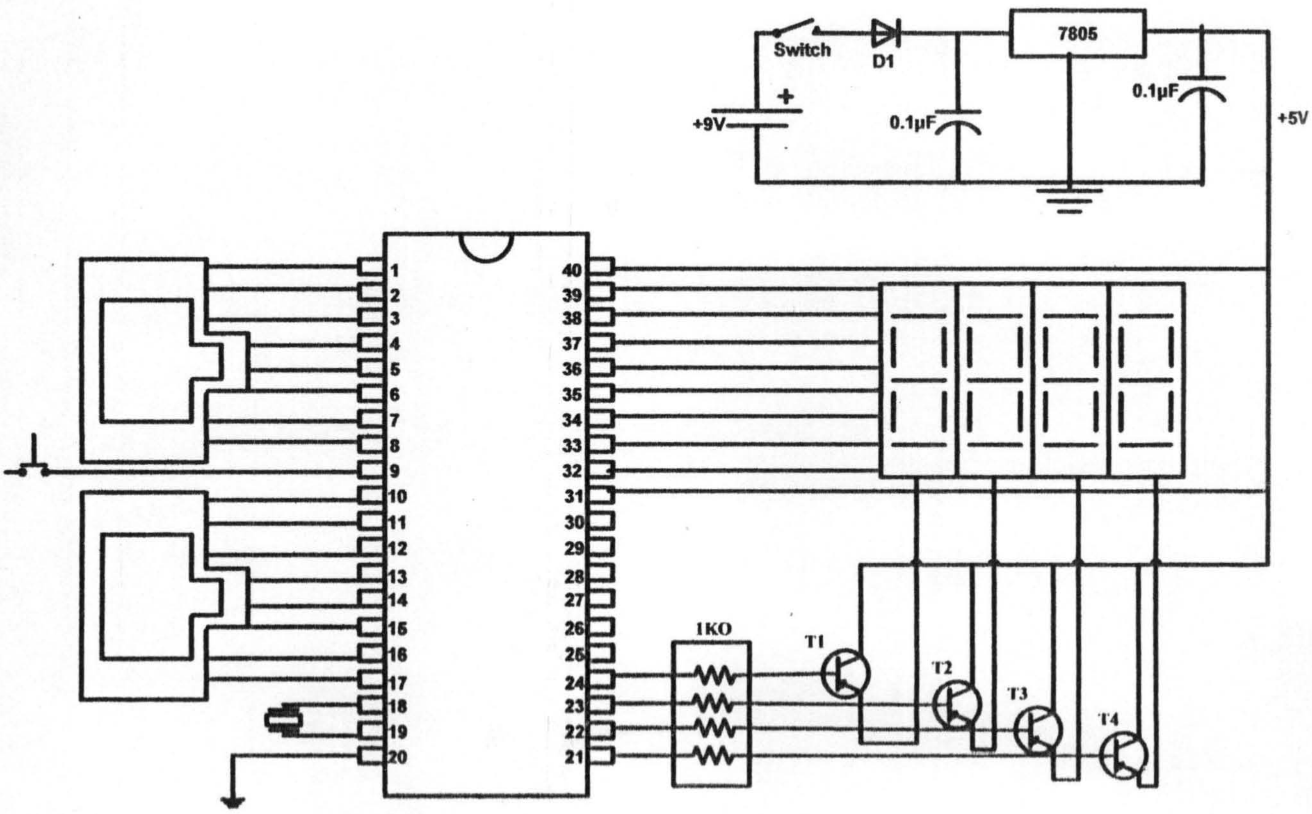


Figure 3.10 Circuit diagram

CHAPTER FOUR

TESTING, RESULT AND DISCUSSION

4.1 CRIMPING OF THE NETWORKING CABLE

A shielded twisted pair (STP) cable used in Ethernet today was purchased with the crimping device. The cable pairs were arranged based on the cable type configuration. The three types of cable configurations are given below;

Table 4.1 Cable configuration

CABLE TYPE	TRANSMITTING END	RECEIVING END
STRAIGHT	1	1
	2	2
	3	3
	4	4
	5	5
	6	6
	7	7
	8	8
CROSS	1	3
	2	6
	3	1

	4	4
	5	5
	6	2
	7	7
	8	8
ROLL OVER/THROUGH	1	8
	2	7
	3	6
	4	5
	5	4
	6	3
	7	2
	8	1

After the cable was crimped base on the cable type shown in figure 4.1 Above, and some other test was carried out on some of the sections of the device to ensure continuity.

4.2 TESTS ON THE POWER SUPPLY MODULE

The automatic networking cable tester is being powered from 9Vbattery source to supply a 5V to the system through a 5V voltage regulator. When the device is powered on by pressing the switch button, the LAN cable tester comes on, showing that the power section is well connected. Based on this test, I was cleared that the display part, which is of the seven segments was working perfectly.

4.3. TESTING OF THE CABLE

The well crimped cable, based on its configuration was tested by inserting one of the ends (or terminals) into the first port and the other into the second port. The result is given in the table below.

TABLE 4.2 RESULT OF THE TEST

Cable name	Connect ion type	Cable Detected	Cable not detected	Cable not detected
RJ 45	STRAI GHT	detected	not detected	not detected
RJ 45	CROSS	detected	not detected	not detected
RJ 45	ROLL OVER/ THROUGH	detected	not detected	not detected

4.3.1 MAKING OF NETWORKING CABLE

Material requirement:

- RJ 45 jack
- Crimping device
- CAT 5 cable
- Wire cutters

4.4: TESTING

The device is tested with a multi meter to ensure that there was on open or short circuit during soldering. The RJ 45 cables was crimped and plugged into the RJ45 female port of the device. The switch was pressed and the out put was display on the seven segments. This was carried out on all the three types of cables.

Finally, a cable with no standard was crimped and tested with this device, on pressing the reset button, the device did not detect the cable.

4.5 RESULT

After all this test the objective has been achieved, the out put on the seven segment indicate that the project design and construction was successful.

4.6 SUMMARY OF THE RESULT

The output display on the seven segment is based on the nature of the crimped cable plugged into the RJ45 female port. Any time a cable is inserted into the port, the seven segment is required to display the type of cable. Already programmed in the microcontroller chip. This is done to reduce the time spent by a networking engineer in the field.

4.7. LIMITATIONS

First of all, one needs to understand that the device described above is a continuity tester, which is used to test a networking cable. In purchasing some of these components, was very difficult, due to the fact that the locality in which we are in is not a commercial city. And as a result, if a device goes bad, like the LCD I used before settling for the use of seven segement was change four times yet all to no avail. This was my initial problem during the construction of this device.

Secondly, other problems encountered were to write a proper program that will assist this device to work properly, without any malfunctioning when a particular cable is being inserted into the port.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1. CONCLUSION

The automatic LAN cable tester is an inevitable continuity testing device in the world of computer system networking, especially in the local area network. It will serve a great deal when systems are to be connected together without any time wastage and gives a better engineering approach to the networking work. The local area networking (LAN) tester comes in a digital display on a seven segment and it is also very handy, which can be used to check the correctness of a crimped cable that a networking personnel has crimped for a particular purpose.

The automatic LAN cable tester employs the use of a microcontroller which serves as the main brain of this device and in order to control the input signals and give the appropriate output signal based on what has been programmed on the microchip. The seven segment displays will display the test result.

5.2. RECOMMENDATION

This project can be improved by introducing a program on the microchip that can also test for RJ 11 and by introducing a remote control censor on it in order that it can be operated from a far distance by pressing a remote to switch it on and select a cable that is plugged for testing.

CONCLUSION

This chapter clearly explained in details the actual components of the design of Automatic LAN cable tester. The function and connectivity between functional parts including the application design with the basic theory is well specified.

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2. Mr A.Ola, A Power Point Presentation on Networking,Excel Cybertect and communication Ltd, Minna.
3. Sybex, CISCO CERTIFIED NETWORING ASSOCIATE,2005.by Todd Lammle
4. .http//www.dux.com
5. http//www.wikepedia.com
6. Encarta Microsoft student 2007
7. Cisco interactive CD 2005
8. 89C51 Instruction set

```
INCLUDE 89c51.mc
;**************************************************************
                ;DESIGNED_BY: BENOR OTULOGBO
                ;MATRIC. NUMBER: 2003|15344EE
                ;PROJECT: AUTO LAN CABLE TESTER
                ;PROGRAMMER SOFT: BATRONIX PROG_STUDIO

;***************************************************************
; ADDRESS LOCATION
;***************************************************************
data_0 DATA 08h
data_1 DATA 09h
data_2 DATA 0ah
data_3 DATA 0bh
data_4 DATA 0ch
mask DATA 0dh


;******************************************************************
; DEFINED PARAMETERS
;******************************************************************
digit_1_Dx BIT p2.1
digit_2_dx BIT p2.2
digit_3_dx BIT p2.3
digit_4_Dx BIT p2.4
data_port EQU p0
master_port EQU p1
slave_port EQU p3
s_mask EQU 10010010b
t_mask EQU 10000111b
r_mask EQU 11001110b
c_mask EQU 11000110b
p_mask EQU 10001100b
a_mask EQU 10001000b
f_mask EQU 10001110b
i_mask EQU 11001111b
l_maks EQU 11000111b
j_mask EQU 11100001b
4_mask EQU 10011001b
5_mask EQU 10010010b
1_mask EQU 11111001b
2_mask EQU 10100100b
3_mask EQU 10110000b
e_mask EQU 10000110b
0_mask EQU 11000000b
o_mask EQU 10100011b
g_mask EQU 10010000b
h_mask EQU 10001011b
b_mask EQU 10000011b
l_mask EQU 11000111b
d_mask EQU 10100001b
u_mask EQU 11100011b
n_mask EQU 10101011b
;******************************************************************
; BIT ADDRESS
;*********************************************************************
cable_detected BIT 00h
stack EQU 60
45_Cross_Detected BIT 01h
45_Straight_Detected BIT 02h
```

```
11_Detected BIT 03h
rollover_detected BIT 04h


;*******************************************************

org 0000h
LJMP start_up

;****************************************************************************
**********
org 0030h
start_up:    CLR ea
             MOV sp,#stack
             ACALL sys_init
;****************************************************************************
*********
Main:        ACALL show_id
             ACALL re_init
             ACALL test_Cable
             JNB cable_detected,main
             ACALL show_cable_detected
             ACALL show_Result
             SJMP main

;****************************************************************************
*******
re_init:     CLR 45_cross_detected
             CLR 11_detected
             CLR 45_straight_detected
             CLR rollover_detected
             CLR cable_detected
             RET

;****************************************************************************
***********
show_cable_Detected:    CLR cable_Detected
                        MOV DPTR,#cable_detected_msg
                        MOV R5,#15
                        ACALL write_data
                        RET
;****************************************************************************
***********
cable_detected_msg:     DB 0ffh
                        DB c_mask
                        DB a_mask
                        DB b_mask
                        DB l_mask
                        DB e_mask
                        DB 0ffh
                        DB d_mask
                        DB e_mask
                        DB t_mask
                        DB e_mask
                        DB c_mask
                        DB t_mask
                        DB e_mask
                        DB d_mask
```

```
                    CLR master_port.2
                    ACALL debounce_key
                    JB slave_port.0, flag_Error2
                    SETB master_port.2
                    CLR master_port.5
                    ACALL debounce_key
                    JB slave_port.1, flag_Error2
                    SETB master_port.5
                    SETB 45_cross_detected
                    SETB cable_detected
flag_error2:    RET

;*************************************************************************************88
test_45_straight: CLR master_port.0
                    ACALL debounce_key
                    JB slave_port.0, flag_error
                    SETB master_port.0
                    CLR master_port.1
                    ACALL debounce_key
                    JB slave_port.1, flag_error
                    SETB master_port.1
                    CLR master_port.2
                    ACALL debounce_key
                    JB slave_port.2, flag_Error
                    SETB master_port.2
                    CLR master_port.5
                    ACALL debounce_key
                    JB slave_port.5, flag_Error
                    SETB master_port.5
                    SETB 45_straight_detected
                    SETB cable_detected
flag_error:         RET

;**************************************************************************

show_id:            MOV DPTR,#id_msg
                    MOV R5,#50
                    ACALL write_data
                    RET
;****************************************************************************************
**

id_msg: DB 0ffh
                DB o_mask
                DB t_mask
                DB u_mask
                DB l_mask
                DB u_mask
                DB g_mask
                DB b_mask
                DB u_mask
                DB 0ffh
                DB b_mask
                DB e_mask
                DB n_mask
                DB o_mask
                DB r_mask
                DB 0ffh
                DB 2_mask
                DB 0_mask
                DB 0_mask
                DB 3_mask
                DB 0ffh
```

```
            DB 1_mask
            DB 5_mask
            DB 3_mask
            DB 4_mask
            DB 4_mask
            DB e_mask
            DB e_mask
            DB 0ffh
*****************************************************
d2_msg:                 DB a_mask
                        DB u_mask
                        DB t_mask
                        DB o_mask
                        DB 0ffh
                        DB l_mask
                        DB a_mask
                        DB n_mask
                        DB 0ffh
                        DB c_mask
                        DB a_mask
                        DB b_mask
                        DB l_mask
                        DB e_mask
                        DB 0ffh
                        DB t_mask
                        DB e_mask
                        DB s_mask
                        DB t_mask
                        DB e_mask
                        DB r_mask

********************************************************************************
**8

how_Result:     JBC 45_cross_detected, go_Show_45_cross
                        JBC 45_straight_detected, go_show_45_straight
                        JBC rollover_Detected, go_Show_rollover
                        RET

o_Show_11a:     AJMP go_Show_11
**************;*****************************************************************
o_show_rollover:        MOV DPTR,#rollover_msg
                        MOV R5,#14
                        call write_Data
                        RET

ollover_msg:    DB 0ffh
                        DB      t_mask
                        DB      h_mask
                        DB      r_mask
                        DB      o_mask
                        DB      u_mask
                        DB      g_mask
                        DB      h_mask
                        DB 0ffh
                        DB c_mask
                        DB a_mask
                        DB b_mask
                        DB l_mask
                        DB e_mask
*****************************************************************************

o_Show_45_cross:        MOV DPTR,#45_cross_msg
```

```
                    MOV R5,#17
                    ACALL write_data
                    RET

45_Cross_msg:   DB 0ffh
                DB r_mask
                DB j_mask
                DB 4_mask
                DB 5_mask
                DB 0ffh
                DB c_mask
                DB r_mask
                DB o_mask
                DB s_mask
                DB s_mask
                DB 0ffh
                DB c_mask
                DB a_mask
                DB b_mask
                DB l_mask
                DB e_mask

;*****************************************************************************

go_Show_45_straight:    MOV DPTR,#45_straight_msg
                        MOV R5,#20
                        ACALL write_data
                        RET

45_straight_msg:db 0ffh
                DB r_mask
                DB j_mask
                DB 4_mask
                DB 5_mask
                DB 0ffh
                DB s_mask
                DB t_mask
                DB r_mask
                DB a_mask
                DB i_mask
                DB g_mask
                DB h_mask
                DB t_mask
                DB 0ffh
                DB c_mask
                DB a_mask
                DB b_mask
                DB l_mask
                DB e_mask


go_Show_11:             MOV DPTR,#11_msg
                        MOV R5,#11
                        ACALL write_data
                        RET
11_msg:         DB 0ffh
                DB r_mask
                DB j_mask
                DB 1_mask
                DB 1_mask
                DB 0ffh
                DB c_mask
                DB a_mask
```

```
                DB b_mask
                DB l_mask
                DB e_mask

;*******************************************************************************8

write_display:  MOV data_port, data_0
                CLR digit_1_dx
                ACALL delay_2_show
                SETB digit_1_dx
                MOV data_port, data_1
                CLR digit_2_Dx
                ACALL delay_2_Show
                SETB digit_2_Dx
                MOV data_port, data_2
                CLR digit_3_dx
                ACALL delay_2_Show
                SETB digit_3_dx
                MOV data_port, data_3
                CLR digit_4_dx
                ACALL delay_2_show
                SETB digit_4_Dx
                RET
;********************************************************************************
888

write_data:             MOV R1,#1
write_data_loop:        CLR A
main_loop:              PUSH acc
                        MOVC A,@a+dptr
                        MOV mask, A
                        ACALL shift_now
                        POP acc
                        INC A
                        DJNZ R5, main_loop
                        MOV mask,#0ffh
                        ACALL shift_now
                        MOV mask,#0ffh
                        ACALL shift_now
                        MOV mask,#0ffh
                        ACALL shift_now
                        MOV mask,#0ffh
                        ACALL shift_now
                        MOV mask,#0ffh
                        ACALL shift_now
                        ACALL blank_display
                        DJNZ R1, write_data_loop
                        RET
;********************************************************************************
88
shift_now:              MOV data_0, data_1
                        MOV data_1, data_2
                        MOV data_2, data_3
                        MOV data_3, mask
                        MOV R2,#30
re_Write:               ACALL write_display
                        DJNZ R2, re_write
                        RET
;*******************************************************************************8
88
```

```
blank_display:  MOV data_0,#0ffh
                MOV data_1, #0ffh
                MOV data_2, #0ffh
                MOV data_3, #0ffh
                ACALL write_display
                RET
;***************************************************************************8
sys_init:       MOV master_port,#0ffh
                MOV slave_port, #0ffh
                CLR 45_cross_detected
                CLR 11_detected
                CLR 45_straight_detected
                CLR rollover_detected
                CLR cable_detected
                RET
;***************************************************************************88
delay_2_Show:
debounce_key:   MOV R7,#5
reload:         MOV R6,#0
                DJNZ R6, $
                DJNZ R7, reload
                RET

;**************************************************************
TEST_ROLLOVER:  CLR master_port.0
                ACALL debounce_key
                JB slave_port.7, flag_error3
                SETB master_port.0
                CLR master_port.1
                ACALL debounce_key
                JB slave_port.6, flag_error3
                SETB master_port.1
                CLR master_port.2
                ACALL debounce_key
                JB slave_port.5, flag_Error3
                SETB master_port.2
                CLR master_port.3
                ACALL debounce_key
                JB slave_port.4, flag_Error3
                SETB master_port.3
                CLR master_port.4
                ACALL debounce_key
                JB slave_port.3, flag_error3
                SETB master_port.4
                CLR master_port.5
                ACALL debounce_key
                JB slave_port.2, flag_error3
                SETB master_port.5
                CLR master_port.6
                ACALL debounce_key
                JB slave_port.1, flag_Error3
                SETB master_port.6
                CLR master_port.7
                ACALL debounce_key
                JB slave_port.0, fla_Error3
                SETB master_port.7
                SETB ROLLOVER_deteced
flag_error3:    RET             SETB cable_detectec
;
```