DESIGN AND CONSTRUCTION OF A VISIBLE LIGHT FOUR DIGIT DIGITAL MONITORING SYSTEM

BY
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2003/15362EE

A THESIS SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG)
SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGER STATE

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DECLARATION

I, Eyioluse Bunmlola Bosede, hereby declare that this project work is wholly and solely written by me under the supervision of Engr. A.S. Mohammed and submitted to the Department of Electrical and Computer Engineering of Federal University of Technology, Minna for the award of Bachelor of engineering (B.ENG) degree in Electrical and Computer Engineering.

EYIOLUSE BUNMILOLA BOSEDE — 10/11/08

(Name of student) — Date and Signature

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(Supervisor) — Date and Signature

PROF. Y.A ADEDIRAN — _____

(Head of Department) — Date and Signature

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(External Supervisor) — Date and Signature

CERTIFICATION

I hereby certify that this project work titled 'THE DESIGN AND CONSRUCTION OF VISIBLE LIGHT FOUR DIGIT DIGITAL MONITORING SYSTEM', was carried out by EYIOLUSE BUNMILOLA BOSEDE under the supervision of ENGR. A.S. MOHAMMED and submitted to the Department of Electrical/Computer Engineering, Federal University of Technology Minna, in partial fulfillment of the requirement for the award of Bachelor of Engineering (B.ENG), degree in Electrical and computer Engineering.

EYIOLUSE BUNMILOLA BOSEDE _____

(Name of student) Date and Signature

ENGR. A.S. MOHAMMED _____

(Supervisor) Date and Signature

DEDICATION

I dedicate this work to the Glory of God and to my parents, brother and sisters, who God used to bless me with a Bachelor of engineering, love you all.

ACKNOWLEDGEMENT

I wish to express my profound gratitude to the Almighty God without whose provision, guidance and inspiration, this work would have been a failure.

I also wish to record my indebtedness to my H.O.D; PROF. Y.A ADEDIRAN and my supervisor ENGR. A.S. MOHAMMED for his cooperation and guidance during the write up. I do acknowledge with sincerity and gratitude the tremendous assistance of my beloved parents; Mr and Mrs Eyioluse and my loving brother Solomon Eyioluse for their effort both morally and financially towards the success of completing my course.

Worth mentioning is my beloved brother James Eyioluse, Adebayo Eyioluse and Folorunsho Eyioluse for their prayer and financial support. Sincere thanks to my dearest Olaofe odofin for his love and financial support through out my duration of study.

I also wish to acknowledge all my lecturer, class mates and friends that have contributed in one way or the other to the success of this project. My special thanks goes to my friends; Bolajoko and her family, Simisola and Timi for always been there for me. May God bless them all.

ABSTRACT

A comprehensive and concise report on the Design and Construction of a Visible Light Four Digit Digital Monitoring System. This system is composed of the power supply unit, the transmitter, the receiver, the counting circuit and the display unit. The aim of the project is to have a system that will be able to monitor the objects that break the beam of visible light between the transmitter and the receiver by counting. The monitoring system can be used in the manufacturing industries to count the number of goods produced passing on a conveyor belt, in stadium to count the number of spectators going in or coming out, in toll gates e t c. This system is designed using visible light as a transmitter to transmit light signal that will be received by a receiver through a photo conductive cell and any object that breaks the beam from the transmitter will be counted.

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CHAPTER ONE

1.0 INTRODUCTION

In the time past there was no much problem of counting either vehicles passing through the tollgate or goods produced in the local industries then, since they were few, people were simply assigned the task and it was carried out well at intervals.

Nowadays, there is a serious need for a faster means of counting, and at the same time not just at intervals but also round the clock. This is due to the fact that now, we have faster moving vehicles passing through the tollgate and also the goods flowing on conveyor belts in modern industries flow at an appreciable speed that makes it uneasy, inconvenient, burdensome and in accurate for a person to monitor without mistakes.

Few years back an infrared digital monitoring system was designed, to perform that function of counting in which transmitter, receiver and a counting circuit was used but it could only count a thousand objects within a very short distance. But for the advancement in technology, there is need for modification. Therefore a more reliable and efficient digital monitoring system that can count thousands at a wider distance is needed.

The above limitations prompted me to design this infrared digital monitoring system for a better reliability and higher efficiency.

Infrared is the part of electromagnetic spectrum lying between the visible and microwave region. Occur in the region of the greater practical importance for infrared

instrumentation between 2 and 5 micrometers. (0.00008 and 0.00006 inches) in wavelength. The strongest absorption occurs at a specific character order as the directions change. By using appropriate detector, it can be seen that the visible light from a mercury lamp is always deviated into the region beyond the violet and the light from a hot iron goes into the other region of the spectrum "below" the red hence the names ultraviolet and infrared which means "extreme violet" and "beneath the red" respectively.

Nevertheless, where visible light is and the invisible, either infrared or ultraviolet begins on the detector being used.

1.1 ADVANTAGES OF THE MONITORING SYSTEM

It is designed to automatically count any object that breaks the beam between the transmitter and receiver. Care has been taken to ensure that the user can operate it easily without any problem. Hence, it was designed with selected components of high efficiency and this makes the system more reliable for this.

1.2 SIGNIFICANCE OF THE MONITORING SYSTEM

The infrared digital monitoring system was designed to be used as a counting system. The system can be used in any industry that uses conveyor belts, for the flow of its products such as cement industry and bottling companies just to mention a few. It can also be used in tollgates to count vehicles passing, as well as in stadium to count the spectators entering and leaving the stadium.

1.3 LIMITATIONS

It can only be used to count 9,999 people or objects. It is not useful where counting beyond 10,000 is required.

1.4 ORGANIZATION OF THE REPORT

This project is organized in the manner described below, reflecting the five chapters contained in the project.

Chapter one dealt with the general introduction of the entire work, the background of the study was fully discussed, the significant, what problem the project would solve was elaborated; advantages and limitations of the project were also clearly explained.

Chapter two was essentially Literature Review of Digital system and Theoretical review of visible light.

Chapter three dealt with system design analysis, operation and circuit diagram of each module.

Chapter four includes the step taken in testing the work, result obtained, limitations of the work and possible remedies.

Finally, the chapter five contains summary of result obtained and problem encountered. It also include possible improvements and recommendations.

CHAPTER TWO

2.0 LITERATURE REVIEW

Digital monitoring system, counts and display the number of object that breaks the beam between the transmitter and receiver.

2.1 HISTORY OF DIGITAL SYSTEM

Digital circuits are made from analog components. The design must assure that the analog nature of the components doesn't dominate the desired digital behavior. Digital systems must manage noise and timing margins, parasitic inductances and capacitances, and filter power connections

Since digital circuits are made from analog components, digital circuits calculate more slowly than low-precision analog circuits that use a similar amount of space and power. However, the digital circuit will calculate more repeatably, because of its high noise immunity. On the other hand, in the high-precision domain (for example, where 14 or more bits of precision are needed), analog circuits require much more power and area than digital equivalents. A digital circuit is often constructed from small electronic circuits called logic gate. Each logic gate represents a function of Boolean gate. A logic gate is an arrangement of electrically controlled switches

Another form of digital circuit is constructed from lookup tables, (many sold as "programmable logic devices", though other kinds of PLDs exist). Lookup tables can

perform the same functions as machines based on logic gates, but can be easily reprogrammed without changing the wiring. This means that a designer can often repair design errors without changing the arrangement of wires. Therefore, in small volume products, programmable logic devices are often the preferred solution. They are usually designed by engineers using electronic design automation software

Engineers use many methods to minimize logic functions, in order to reduce the circuit's complexity. When the complexity is less, the circuit also has fewer errors and less electronics, and is therefore less expensive.

The classical way to represent a digital circuit is with an equivalent set of logic gates. Another way, often with the least electronics, is to construct an equivalent system of electronic switches (usually transistor). One of the easiest ways is to simply have a memory containing a truth table. The inputs are fed into the address of the memory, and the data outputs of the memory become the output

A sequential system is a combinatorial system with some of the outputs fed back as inputs. This makes the digital machine perform a "sequence" of operations. The simplest sequential system is probably a flip flop, a mechanism that represents a binary digit or "bit". Sequential systems are often designed as state machines. In this way, engineers can design a system's gross behavior, and even test it in a simulation, without considering all the details of the logic functions.

Sequential systems divide into two further subcategories. "Synchronous" sequential systems change state all at once, when a "clock" signal changes state. " asynchronous sequential systems propagate changes whenever inputs change. Synchronous sequential systems are made of well-characterized asynchronous circuits such as flip-flops, that change only when the clock changes, and which have carefully designed timing margins.

The usual way to implement a synchronous sequential state machine is divide it into a piece of combinatorial logic and a set of flip flops called a "state register." Each time a clock signal ticks, the state register captures the feedback generated from the previous state of the combinatorial logic, and feeds it back as an unchanging input to the combinatorial part of the state machine. The fastest rate of the clock is set by the most time-consuming logic calculation in the combinatorial logic.

The state register is just a representation of a binary number. If the states in the state machine are numbered (easy to arrange), the logic function is some combinatorial logic that produces the number of the next state.

In comparison, asynchronous systems are very hard to design because all possible states, in all possible timings must be considered. The usual method is to construct a table of the minimum and maximum time that each such state can exist, and then adjust the circuit to minimize the number of such states, and force the circuit to periodically wait for all of its parts to enter a compatible state. (This is called "self-resynchronization.") Without such careful design, it is easy to accidentally produce asynchronous logic that is "unstable",

that is, real electronics will have unpredictable results because of the cumulative delays caused by small variations in the values of the electronic components. Certain circuits (such as the synchronizer flip-flops, switch debouncers, and the like which allow external unsynchronized signals to enter synchronous logic circuits) are inherently asynchronous in their design and must be analyzed as such.

As of 2005, almost all digital machines are synchronous designs because it is much easier to create and verify a synchronous design -- the software currently used to simulate digital machines does not yet handle asynchronous designs. However, asynchronous logic is thought to be superior, if it can be made to work, because its speed is not constrained by an arbitrary clock; instead, it simply runs at the maximum speed permitted by the propagation rates of the logic gates from which it is constructed. Building an asynchronous circuit using faster parts implicitly makes the circuit "go" faster.

In register transfer logic, binary number are stored in groups of flip flops called registers. The outputs of each register are a bundle of wires called a "bus" that carries that number to other calculations. A calculation is simply a piece of combinatorial logic. Each calculation also has an output bus, and these may be connected to the inputs of several registers. Sometimes a register will have a multiplexer on its input, so that it can store a number from any one of several buses. Alternatively, the outputs of several items may be connected to a bus through buffers that can turn off the output of all of the devices except

one. A sequential state machine controls when each register accepts new data from its input.

In the 1980s, some researchers discovered that almost all synchronous register-transfer machines could be converted to asynchronous designs by using first-in-first-out synchronization logic. In this scheme, the digital machine is characterized as a set of data flows. In each step of the flow, an asynchronous "synchronization circuit" determines when the outputs of that step are valid, and presents a signal that says, "grab the data" to the stages that use that stage's inputs. It turns out that just a few relatively simple synchronization circuits are needed.

2.1.1 APPLICATIONS AND ADVANTAGES OF DIGITAL SYSTEM

1. The device used in Digital Circuits generally operate in one of the two states, known as, ON & OFF resulting in a very simple operation.
2. There are only a few basic operations in digital Circuit which are very easy to understand.
3. Digital Technique requires Boolean Algebra which is very simple and easily be learnt.
4. Digital Circuit requires basic concept of Electrical Network Analysis which is easily learnt.

5. A large number of Integrated Circuits (IC)are available for performing various operations. These are highly reliable, accurate and the speed of operations is very high.

6. The effect of fluctuations in the characteristics of the components, ageing of components, temperature and noise etc. is very small in Digital Circuit.

7. Digital Circuit have capability of memory which makes these circuit highly suitable for Computers, Calculators, Electronic Watches etc.

8. It is very fascinating & challenging field of study because most of the latest Electronics systems are Digital in nature.

2.2 THEORETICAL REVIEW

2.3 VISIBLE LIGHT

White light dispersed by a prism into the colors of the optical spectrum.

The visible spectrum (or sometimes called the optical spectrum) is the portion of the electromagnetic spectrum that is visible to (can be detected by) the human eye. Electromagnetic radiation in this range of wavelengths is called visible light or simply light. A typical human eye will respond to wavelengths in air from about380 to 750mn.The corresponding wavelengths in water and other media are reduced by a factor equal to the refractive index. In terms of frequency, this corresponds to a band in the vicinity of 400–790 terahertz. A light-adapted eye generally has its maximum sensitivity

at around 555 nm(540 THz), in the green region of the optical spectrum. The spectrum does not, however, contain all the colors that the human eyes and brain can distinguish. Unsaturated colors such as pink and purple colors such as magenta are absent, for example, because they can only be made by a mix of multiple wavelengths.

Wavelengths visible to the eye also pass through the "optical window", the region of the electromagnetic spectrum which passes largely unattenuated through the Earth's atmosphere (although blue light is scattered more than red light, which is the reason the sky appears blue). The response of the human eye is defined by subjective testing, but the atmospheric windows are defined by physical measurement. The "visible window" is so called because it overlaps the human visible response spectrum; the near infrared (NIR) windows lie just out of human response window, and the Medium Wavelength IR (MWIR) and Long Wavelength or Far Infrared (LWIR or FIR) are far beyond the human response region.

The eyes of many species perceive wavelengths different from the spectrum visible to the human eye. For example, many insects, such as bees, can see light in the ultraviolet, which is useful for finding nectar in flowers. For this reason, plant species whose life cycles are linked to insect pollination may owe their reproductive success to their appearance in ultraviolet light, rather than how colorful they appear to our eyes. Birds are also said to be able to see into the ultraviolet (300-400 nm) and oddly enough, the sex-dependent markings on some bird plumage is only visible in the ultraviolet range.

2.4 COUNTERS

Digital counters are integrated circuits (ICs) that count events in computers and other digital systems. Because they must remember past states, digital counters include memory. Generally, digital counters consist of bistable devices or bistable multivibrators called flip-flops. The number of flip-flops and the way in which they are connected determines the number of states and the sequence of states that digital counters complete in each full cycle. The way in which devices are clocked determines whether digital counters are categorized as synchronous or asynchronous. In synchronous devices, one clock triggers all of the flip-flops simultaneously. With asynchronous or ripple counters, an external clock pulse triggers only the first first-flop. Each successive flip-flop is then clocked by one of the outputs (Q or Q') of the previous flip-flop. Some digital counters can operate either synchronously or asynchronously. Devices can count in an increasing sequence, a decreasing sequence, or in either increasing or decreasing sequences [4]. Several types of digital counters are available they include;

i. Johnson counter

ii Decade Counter

iii Up-Down Counters

iv Ring Counters

2.4.1 JOHNSON COUNTERS

A Johnson counter is a special case of shift register, where the output from the last stage is inverted and fed back as input to the first stage. A pattern of bits equal in length to the shift register thus circulates indefinitely. These counters are sometimes called "walking ring" counters, and find specialist applications, including those similar to the decade counter, digital to analogue conversion, etc [8].

2.4.2 DECADE COUNTERS

Decade counters are a kind of counter that counts in tens rather than having a binary representation. Each output will go high in turn, starting over after ten outputs have occurred (then, all the flip-flops are cleared/reset). This type of circuit finds applications in multiplexers and demultiplexers, or wherever a scanning type of behaviour is useful. Similar counters with different numbers of outputs are also common . are counters with different numbers of outputs are also common.

2.4.3 UP-DOWN COUNTERS

It is a combination of up counter and down counter, counting in straight binary sequence. There is an up-down selector. If this value is kept high, counter increments binary value and if the value is low, then counter starts decrementing the count. The Down counters are made by using the complemented output to act as the clock for the next flip-flop in

the case of Asynchronous counters. An Up counter is constructed by linking the Q out of the J-K Flip flop and putting it into a Negative Edge Triggered Clock input [8].

2.4.4 RING COUNTERS

A ring counter is a counter that counts up and when it reaches the last number that is designed to count up to, it will reset itself back to the first number. For example, a ring counter that is designed using 3 JK Flip Flops will count starting from 001 to 010 to 100 and back to 001. It will repeat itself in a 'Ring' shape and thus the name Ring Counter is given [8].

CHAPTER THREE

3.0 SYSTEM DESIGN ANALYSIS AND OPERATON

3.1 DESIGN PRINCIPLES

The design of the digital monitoring system is to count any object that breaks the beam between the transmitter and the receiver. The design will be considered under the following units; power supply unit, transmitter unit (unit light) receiver unit, counting unit and the display unit.

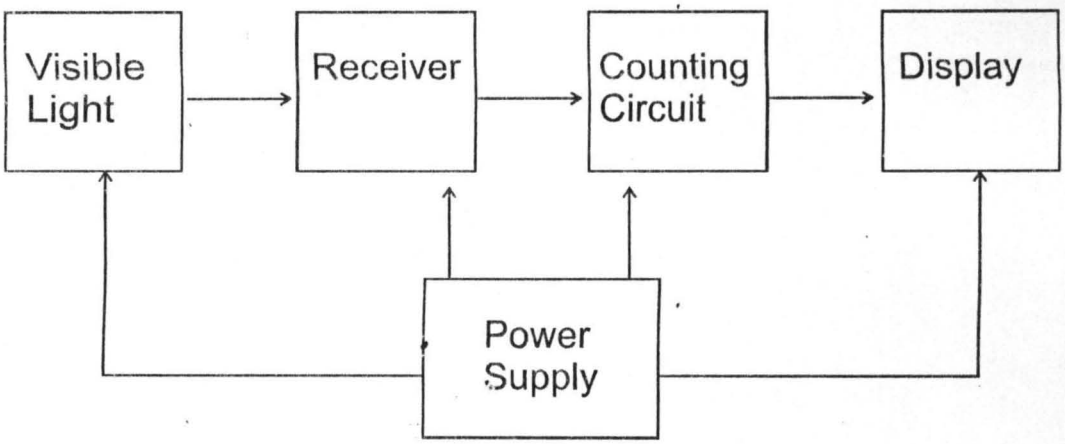

Fig 3.1 The Block Diagram Of The Monitoring System.

3.2 POWER SUPPLY UNIT

Power supply unit is one of the most important requirements in any design and it must be of required magnitude that effectively operates the system. The transmitter rectifier, filter and regulator are the most important components of the power supply. A regulated

voltage of 5V was used to power the receiver and the counting circuits because of the Transistor logic (TTL) family integrated circuit used which require an input voltage between 4.75V and 5.25V on the other hand a 9V battery powers the transmitter circuit.

Below is the block diagram of the power supply unit.

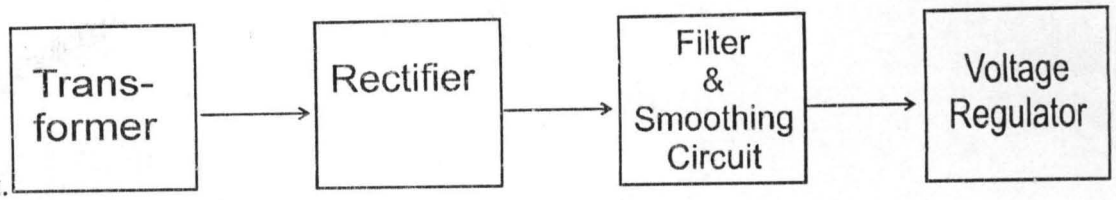

fig 3.2 Block Diagram Of The Power Supply Unit.

3.2.1 TRANSFORMER

In the choice of transformer, care was taken and appropriate calculations done to ensure that the power supply unit works efficiently. This was achieved by making sure that the rating of the transformer does not fall below the required rating for the unit with special consideration given to the 5V regulator used which requires a minimum of 7V and a maximum of 25V for perfect and effective regulation.

The normal mains supply is meant to be 240V. In order to cater for fluctuation range between ±42% of this value i.e. fluctuation as low as 140V and as high as 340V. In order to main the minimum supply voltage to the regulator then the transformer ratio of primary to the secondary N1:N2 must be a maximum of N1/N2 = 140/7 =20 so that when the voltage falls as low as 140v, 7V output can still be obtained for the regulator input.

Since the mains supply fluctuate between 220V and 240V for a fairly constant source, therefore the average voltage supply is given by (240+220)/2 = 230V

From the transformer equation we have N1/N2 =V1/V2

N1 =Number of turns in the primary

N2=Number of turns in the secondary

V1=Primary voltage from the main supply

V2=secondary voltage

The maximum turns ration N1/N2 has been determined to be 20 and the average supply voltage from mains, V1 was found to be 230V. the secondary voltage V2 can therefore be calculated this:

$N1/N2 = V1/V2$

$20 = 230/V2$

$V2 = 230/20$

$V2 = 11.5V$

From the above analysis and calculations, the transformer rating should be 11.5V, 500mA but there is no standard rating like this, therefore 12V, 500mA transformer was selected because it was close to the calculated values.

3.2.2 RECTIFICATION

The next component on the block diagram of the power supply is the rectifier. The component selected for the rectification is the diode. It was used to rectify the output

voltage from the transformer as well as the type of rectification used, i.e. whether half wave, full wave or bridge rectification. Below is the circuit diagram of the bridge rectification.

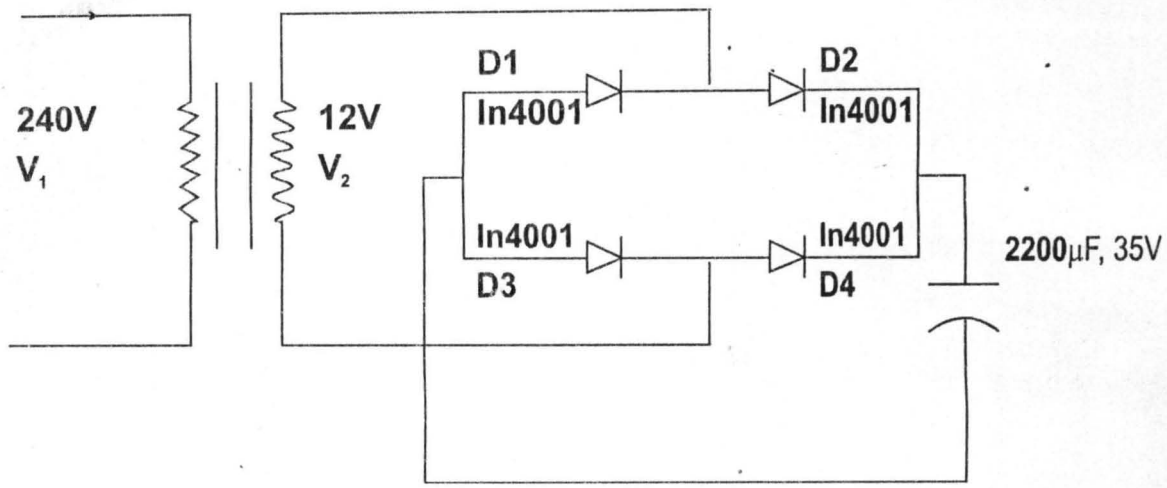

FIG 3.3 Bridge Rectification

V2 = 12V

$V_{out\ (peak)} = V2_{peak} = V2/0.7071=12/0.7071=17$

$V_{d.c.} = 2\ V_{out\ (peak)}/\pi = 2(17)/\ \pi = 34/\ \pi = 10.8V$

During the positive half cycle of the secondary voltage, diode D2 and D3 are forward biased and current flows through the load. In the negative half cycle of the secondary voltage, diodes D1 and D4 are forward biased therefore current flows through the load as

well. Since the load current is in the same direction, the full wave rectified signal appears across the load as seen in the figure below.

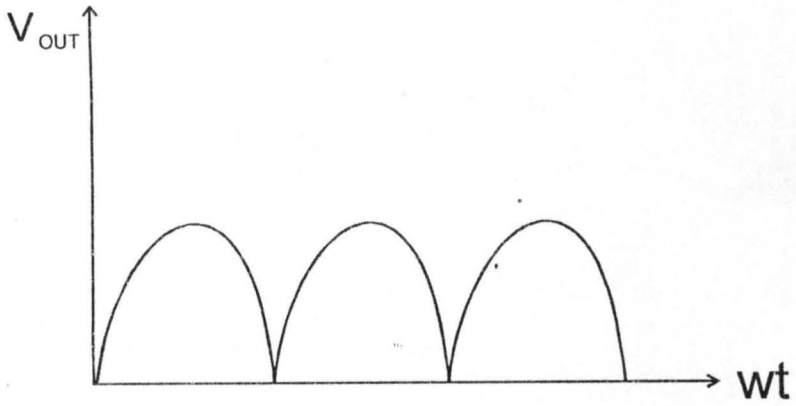

Fig. 3.4 full wave bridge rectified output

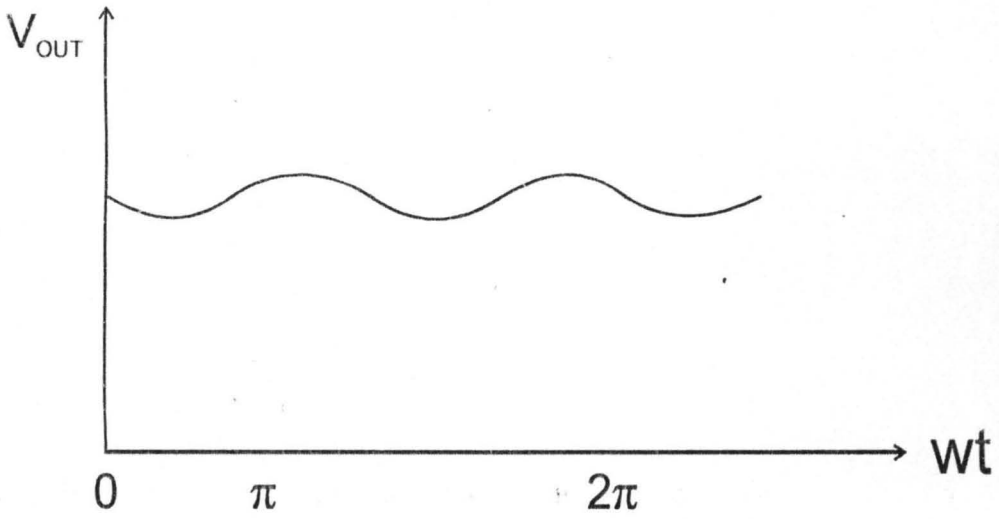

Fig. 3.5: Filtered Output

The bridge rectification was chosen for the design because the frequency F at the output of a half wave rectifier is the same as the line input frequency where as that of the bridge

and full wave rectifier is twice the line input frequency thereby reducing the ripple. Also the half wave rectification uses only the positive half cycle but it was desired that both the positive and the negative half cycles be used. For this reasons the half wave rectification was not used. The ripple voltage is calculated thus;

$V_{ripp} = I/(FC)$

I = D.C. load circuit

F= ripple frequency

C= capacitance

For half wave rectification $V_{ripp} = I/FC$

For bridge and full wave rectification $V_{ripp}=I/(2FC) = 0.5I/(FC)$

This shows that V_{ripp} is smaller for bridge and full wave rectification than for half wave rectification and the smaller the ripple the better as illustrated below.

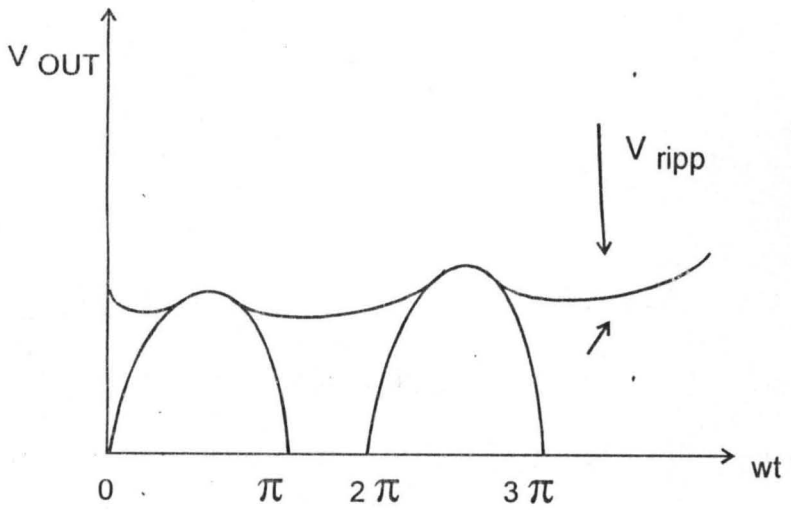

Fig. 3.6 Half wave rectification

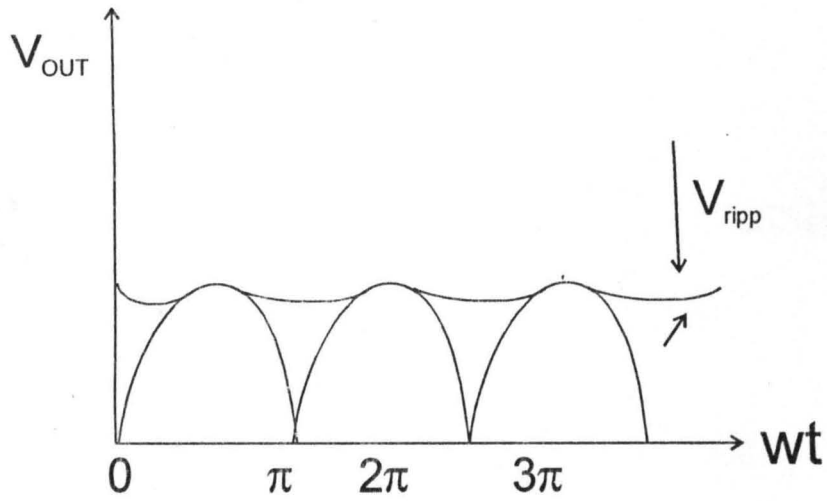

Fig. 3.7 Full or bridge rectification

The following are the analysis and calculations that actually led to the choosing of bridge rectification for the design.

V2 = secondary voltage (V_{rms})

V_{rms}= 0.707$V2_{peak}$

$V2_{peak}$ = V2/0.707=17V

For full wave rectification

IF V1=240.....1

V2=V1/(N1/N2)

IF N1/N2=20.....2

V2 = 240/20=12V

V2 = 12V 3

$V2_{peak} = V2/0.707$

$V2_{peak}=12/0.707$

$V2_{peak}=16.97V$.....4

If VI falls as low as 140V

i.e V1=140.....5

and N1/N2=20 from.....2

V2 = V1(N1/N2)

V2= 140/20

V2= 7V.....6

$V2_{peak} = V2/0.707$

$V2_{peak}=7/0.707$

$V2_{peak}= 10V$.....7

From the calculation above, it was observed that for bridge rectification the peak voltage $V_{(peak)}$ at 240V which is calculated as16.97V from equation 4 and 140V mains supply peak voltage calculated as 10V from equation 8 all fall within the range of input for regulation by the voltage regulator. Due to the above considerations, calculations and analysis, a bridge rectifier was used and the diodes used were four IN4001 which have PIV ratings of 50V each. Since the PIV rating of these diodes are greater than the peak secondary voltage $V2_{peak}$ even at higher voltage than the required 240V mains supply, hence they are suitable for the project work

3.2.3. FILTERING

A very high value of capacitor is needed to filter the rectified output and reduce the ripple as much as possible. The voltage rating of that capacitor which should be electrolytic should be greater than $1.44V2_{peak}$ where $V2_{peak}$ = peak out put secondary voltage and this is given as 17V from equation 4.

$1.414V2_{peak} = 1.414(17) = 24V.$

For perfect filtering and smoothing of the output voltage, a 2200μF, 35V electrolytic capacitor was used as the filtering capacitor. The output wave form is shown in FIG 5 above.

3.3 TRANSMITTER UNIT

The transmitter unit is made up of switching transistor, visible light and a variable resistor.

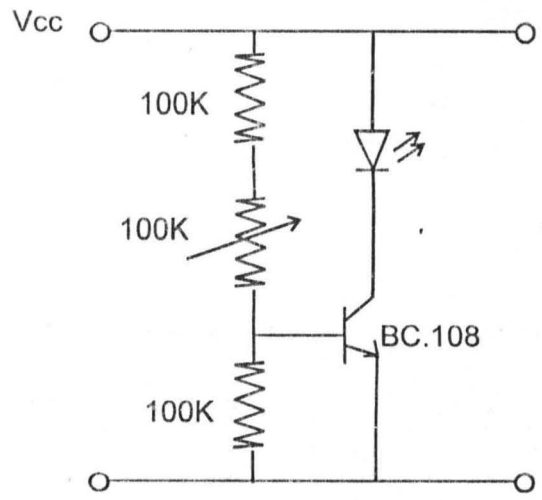

FIG 3.8 Transmitter Circuit

3.4 RECEIVER UNIT

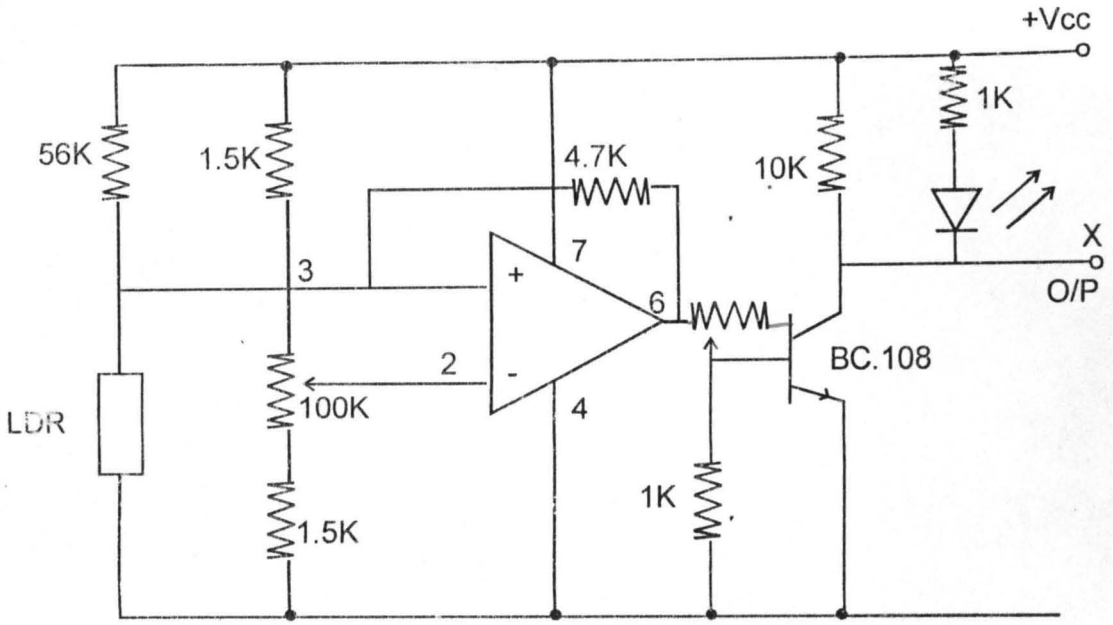

FIG 9 Receiver Circuit

Light from the transmitting unit is directed to the receiving unit ,and Light Dependent Resistor [LDR] from the receiving unit senses the light. LDR is a resistor whose resistance varies with the intensity of light that falls on it. The higher the intensity of light that falls on it the lower the resistance of the LDR when an object obstruct the light from the transmitter to the receive, the resistance of the LDR increases which then send a voltage to the operational amplifier which amplifies that signal to trigger the transistor into conduction. And output from the transistor is fed into the decade counter [7490] as pulse signal. There is always a count at the decade counter each time there is an obstruction of the light coming to the receiver and the seven segment display displays a digit corresponding to the number of time the light coming to the receiver is obstructed.

3.5 COUNTING UNIT

The counting unit consists of four counters, four BCD to seven segment decoder drivers, four seven segment displays. This is to enable the readout display up to four digits, which means that the numbers start from 0000 and end at 9999 before recycling back to the starting point.

3.5.1 DECADE COUNTER

A counter is made up of cascaded flip flops that count the number of clock pulses that arrive at the input. It can consist of any number of flip flops depending on its MOD number as derived by the formula below.

$MOD=2^N$

MOD= mode number

N= number of flip flops

Mode number is the maximum number of counts before recycling back to the starting point. If there is no integer value that gives the mode number exactly, the next integer that is just above it is chosen. A decade counter is a MOD 10 counter, hence the number of flip-flops can be calculated thus.

$10=2^N$, there is no integer that gives this value exactly. $2^3= 8$ and $2^4=16$ are closet to 10, therefore N=4 since $2^4=16$ is the closet above 10. There are two types of counters they are, synchronous or parallel counters and asynchronous or ripple counters. In

synchronous counters all the flip-flops are triggered simultaneously by the clock input pulses applied. Since the input is applied to all the flip-flops, some means are used to control when the flip-flop is to toggle and when it is to remain unaffected. Synchronous counters do not have propagation delay as seen in asynchronous counter. They can operate as a very high frequency but the circuit is complex. In asynchronous counter, flip-flops are cascaded in such a way that the output of one flip-flop is the clock input of the next flip-flop. All the flip flops do not change stage in exact synchronism. Thus, there is delay between the responses of consecutive flip-flops but at low frequencies this is not noticed. Nevertheless the simplicity of its circuit as well as the few number of components required per operation has led to the used of asynchronous or ripple counter for this design. The counter used in designing this system is 74LS90, which is a four but ripple type decade counter. The design consist of four master – slave flip-flop internally connected to provide a divided by five section. Each section has a separate clock input to initiate state changes of the counter on the HIGH – TO – LOW clock transition. State changes of the outputs do not occur simultaneously because of the internal ripple delays. Therefore decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. In the 7490 PIN OUT shown in FIG 10 below, the Q_0 output is designed and specified to drive the rate fan out plus the CP input of the device. A gated AND asynchronous master reset (MR1 MR2) is provided which over rides both clock and resets (clears) all the flip-flops. Also a gated AND asynchronous set (MS1 MS2) which overrides the clock and the MR inputs, setting the outputs to nine (HLLH).

In a BCD counter, the CP1 input must be externally connected to the Q_o output. The CPo input count is then applied to the CP1 input, and a divided by 10 square wave is obtained. Mode 10 counter was achieved by a divide by two and a divide by five counter, no external interconnections are required. The first flip-flop is used as a binary element for the divide by two function (CP_o as the input and Q_o as the output). The CP1 input is used to obtain divide by five operation at the Q_3 output.

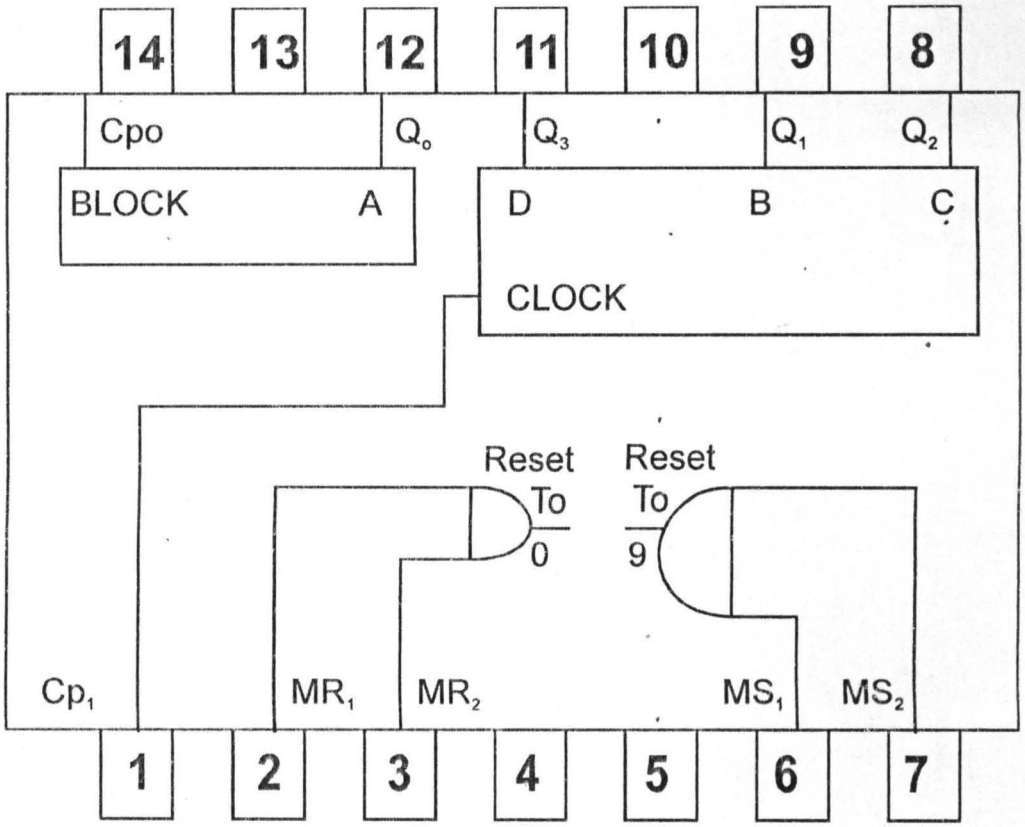

Fig. 3.10 7490 Pin out

TABLE 3.1 Table of 7490 pin out output.

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Table 3.2 **Truth Table For Count Sequence**

RESET/SET INPUTS				OUTPUTS			
MR1	MR2	MS1	MS2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	COUNT			
X	L	X	L	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

N.B. Output Q_o is connected to input CP1

H = high voltage level

L= low voltage level

X=Don't care

3.5.2 BCD TO SEVEN SEGMENT DECODER DRIVER

A BCD to seven – segment decoder driver is used to accept a four at BCD input code and provide the appropriate outputs that will pass current through the appropriate segment to display the decimal digit 0-9 in a seven segment display. The term "driver" is added to its description because it has open collector outputs that can operate at higher current and voltage limits than a normal TTL output. The IC used for this design is the SN 7447AN. This IC has active low open collector outputs, which can be pulled up to 30V in the HIGH state.

This makes it suitable for directly driving loads such as indicator LEDs on lamps, relays or DC motors. The logic for this decoder is more complicated than others because each output is activated for more than one combination of inputs.

Seven segment decoder drivers such as the 7447 are exceptions to the rule that decoder circuits activate only one output for each combination of inputs. Rather they activate a unique pattern of outputs for each combination of inputs.

The 7447 decoder/driver are designed as common anode types. Since the anodes of the seven segment display LEDs are tied to V_{cc} while a low output from the decoder driver activates the required segments on the other hand the 7448 is a common cathode type because the cathodes of the seven – segment display LEDs connected to ground while a high output from the decoder driver activates the required segment. The most significant decoder stage should have the RBI input grounded and because suppression of the least significant integer zero in a number is not usually desired. The RBI input of this decoder stage should be left open.

A similar procedure for the fractural part of a display will provide automatic suppression of trailing edges zeros. The decoder has an active low input lamp test which overrides all other input combinations and enables a check to be made on possible display malfunctions shown be is the truth table and the activated segment patters for all possible input codes from 0000 to 1111 Note that an input code of 111 (i.e. 15) will blank out all the segment.

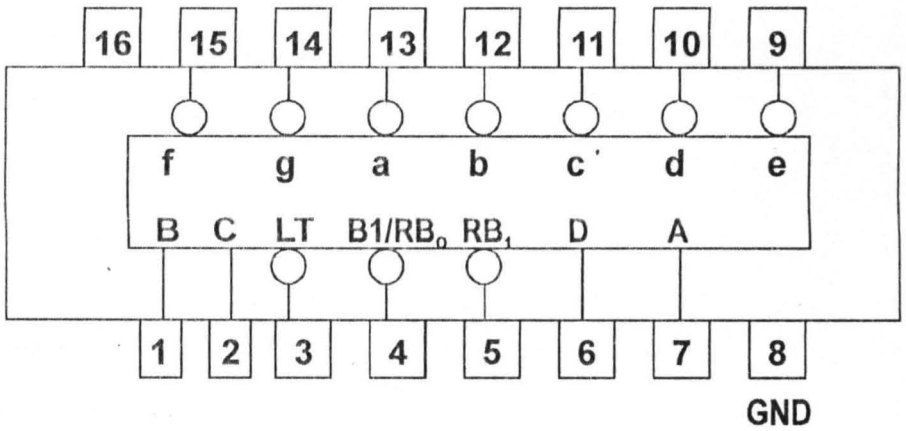

FIG 3.11 7447 Pin out

TABLE 3.3 Truth table and activated segment pattern for all possible input codes

No	Q3	Q2	Q1	Qo	LT	RBI	RB0	a	B	c	D	e	f	g	Display
0	L	L	L	L		X	x	H	L	L	L	L	L	H	0
1	L	L	L	H	H	X	X	H	L	L	H	H	H	H	1
2	L	L	H	L	H	X	X	L	L	H	L	L	H	L	2
3	L	L	H	H	H	X	X	L	L	L	L	H	H	L	3
4	L	H	L	L	H	X	X	L	H	L	L	H	H	L	4
5	L	H	L	H	H	X	X	L	H	L	L	H	L	L	5
6	L	H	H	L	H	X	X	H	H	L	L	L	L	L	6
7	L	H	H	H	H	X	X	L	L	L	H	H	H	H	7
8	L	L	L	H	L	X	X	L	L	L	L	L	L	L	8
9	H	L	L	H	H	X	X	L	L	L	H	H	L	L	9
10	H	L	H	L	H	X	X	H	H	H	L	L	H	L	5
11	H	L	H	L	H	X	X	H	H	L	L	H	H	L	2
12	H	H	L	L	H	X	X	H	L	H	H	H	L	L	4
13	H	H	L	L	H	X	X	L	H	H	L	H	L	L	5
14	H	H	H	L	H	X	X	H	H	H	L	L	L	L	6
15	H	H	H	H	H	X	X	H	H	H	H	H	H	H	.
B1	X	X	X	X	X	X	X	H	H	H	H	H	H	H	
RB1	L	L	L	L	H	X	x	H	H	H	H	H	H	H	
LT	X	X	X	X	L	X	X	L	L	L	L	L	L	L	

H= High voltage level

L= Low voltage level

X= Don't Care

3.5.3 SEVEN SEGMENT DISPLAY

Most digital equipment has some means for displaying information in a form that can be understood readily by the user or operator.

This information is often numerical data, but can also be alphanumeric (numbers and letters) one of the simplest and most popular methods for displaying numeric digit uses a seven segment configuration to form the decimal characters 0 through 9 and some times the hex characters A through F. One common arrangement uses light emitting diodes (LEDs) for each segment. By controlling the current through each LED some segments will light up while others will be dark so that desired character pattern will be generated.

For the purpose of this design, given 3 inches common cathode right hand decimal point seven – segment display was used. It has high brightness, high legibility, bold solid segment, fast sunteling, low power consumption and compatibility with integrated circuits.

It has a forward voltage V_f of 2V at a forward current of 20mA per segment. It also has a reverse voltage of 3V per segment.

The pin configuration is as shown in FIG 12 below.

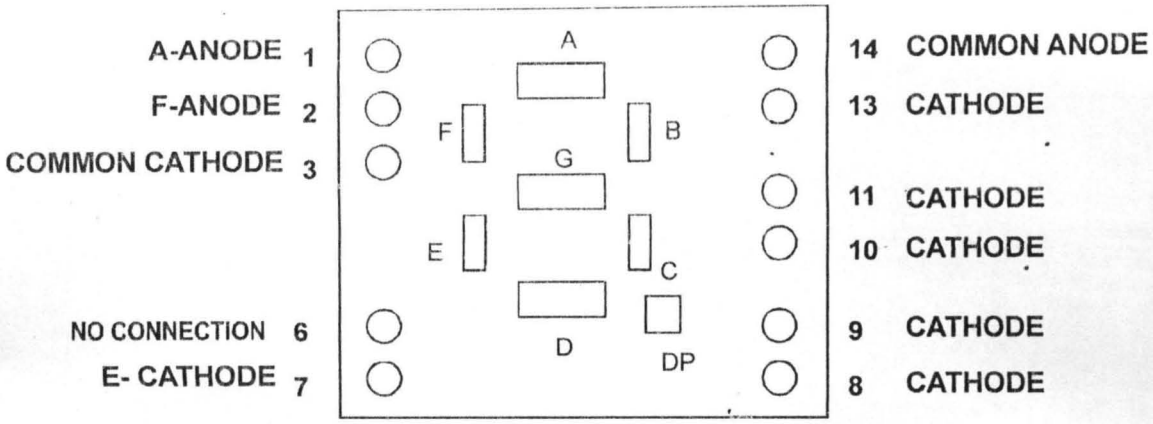

FIG. 3.12 GREEN 3" COMMON ANODE RIGHT HAND DECIMAL POINT PIN OUT

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CHAPTER FOUR

4.0 TEST, RESULTS AND DISCUSSION OF RESULTS

4.1 TESTING

On successful completion of the construction, the first thing that was done was to carry out a thorough test of the circuit to make sure that there was no misconnection resulting in short circuit or bridging components before it is powered. Other test were still carried out after powered to ascertain the proper operation of the system. This test involves a number of different procedures ranging from visual to equipment checks to cater for a perfect working condition. The visual checks were performed before power was connected to the circuit while the equipment checks were performed when power was connected to the circuit.

4.2 RESULTS

On completion and testing of the system, the following results were obtained.

The output of the voltage regulator 7805 was measured to be 5V. The transmitter and the receiver were tested with the receiver having a maximum distance of 30cm.The counting circuit also responsible to the clocked signals from the receiver thereby counting each time there's a blockage at the visible light with the number of blockage registered by the unit displayed.

The Display unit displays the number of blockage that is registered.

4.3 DISCUSSION OF RESULT

The Display unit displays the number of biockage that is registered which indicates the total number of object counted.

CHAPTER FIVE

5.0 CONCLUSION AND RECOMMENDATIONS.

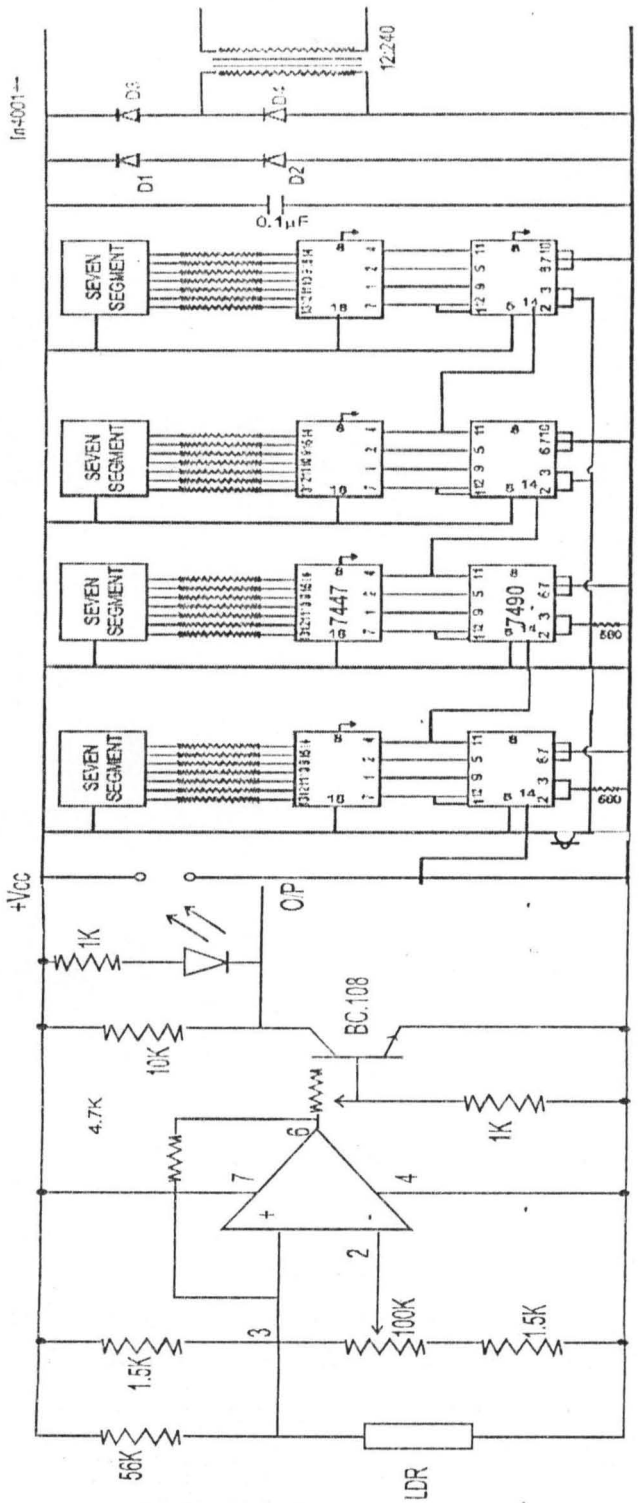
5.1 CONCLUSION

It can be observed from this project that the design and construction of an infrared digital monitoring system worked accordingly to specification and quite satisfactory, it is relatively affordable and reliable. It is easy to operate.

5.2 RECOMMENDATION.

Since it is known that this project can count only a limited number, and within a short distance, It is recommended that anybody that wish to embark on this project should make use of a microcontroller to produce a more effective result. That is to have a system that can count above 10,000 and at a wider distance.

GENERALIZED CIRCUIT DIAGRAM



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