

**FEDERAL UNIVERSITY OF TECHNOLOGY**  
**SCHOOL OF SCIENCE AND TECHNOLOGY EDUCATION**  
**DEPARTMENT OF INDUSTRIAL AND TECHNOLOGY EDUCATION**  
**SECOND SEMESTER EXAMINATION 2017/2018 SESSION**

**COURSE TITLE: DIGITAL ELECTRONICS**

COURSE (I)

DIGITAL ELECTRONICS

**COURSE CODE: IET 522**

**TIME ALLOWED: 2HOURS**

**INSTRUCTION: ATTEMPT FOUR QUESTIONS ONLY**

- Q1a. State the main stages to creating a logic expression using karnaugh map  
b. Draw karnaugh maps for the following expressions and obtain a simplified expression for the maps:

$$X = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + ABC\bar{D} + ABCD$$

$$X = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + ABC\bar{D} + ABCD$$

- Q2a. Convert the following binary numbers to hexadecimal  
(i) 1100101001010111 (ii) 1111110001011010  
b. Design a logic circuit to implement the following expressions:  
(i)  $X = (\bar{A}\bar{B}\bar{C})(B+C) + \bar{A}\bar{B}C$ . (ii)  $X = \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$   
(iii)  $X = ABCD + ABC\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD$

- Q3a. Prove the following Boolean expressions by means of truth table  
(i)  $A + \bar{A}B = A + B$  (ii)  $A + AB = A$  (iii)  $(A+B)(A+C) = A + BC$   
b. Simplify the following expressions  
(i)  $AB + A(B+C) + B(B+C)$  (ii)  $AB + AC + ABC$

- Q4a. Define and state the truth table of the following logic gates: (i) AND (ii) OR (iii) NOT  
(iv) NAND (v) NOR (vi) XOR (vii) XNOR  
b. State six advantage of digital systems over analogue

- Q5a State the difference between TTL, ECL and CMOS logic families with regards to their design rules, power consumption and speed  
b. Draw the logic symbols of 4-input AND and 4-input NOR gates and present their respective truth tables