COMPUTER SIMULATION OF DIGITAL SYSTEMS FOR CURRENCY PROCESSING:
(A CASE STUDY OF CENTRAL BANK OF NIGERIA)

By

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A PROJECT SUBMITTED TO THE DEPARTMENT OF MATHS/COMPUTER SCIENCE FOR THE AWARD OF A POST GRADUATE DIPLOMA IN COMPUTER SCIENCE AT THE FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

MARCH, 1998

CERTIFICATION

This is to certify that the work reported in this project was carried out by `Bayo Falekulo under my supervision and it has been approved by me.

APPROVAL

This project is hereby approved in partial fulfilment of the requirement for the award of Post Graduate Diploma in Computer Science in the Mathematics and Computer Science Department of the Federal University of Technology Minna. By

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SUPERVISOR

HEAD OF DEPARTMENT

ABSTRACT

Computer simulation represents the application of mathematical modelling techniques to real system thus, enabling information on systems characteristic and parameters to be gained without either constructing or operating the full scale system under consideration.

Earlier application of computer simulation in Engineering was focused at Analogue computer to study continuous systems by generating numerical equations, defining the model for a giving initial conditions by the use of some standard step-by-step method of analysis.

Development in simulation techniques have led to the rapid development in computers and most system simulations are currently based on large general purpose computers.

Consequently, training and operation planning are usually performed with specialised computers.

This project is to simulate currency processing whereby they are sorted into FIT,UNFIT, SHREDDED, Manual inspection and rejected using computer aided modes.

ACKNOWLEDGEMENT

First and foremost, my unqualified gratitude goes to almighty God, our father, who despite my inadequate and short comings saw me through this course successfully.

My special thanks and appreciation goes to my supervisor and course co-ordinator, Mr. Badmos who took the pains and time to go through my manuscript despite the over whelming pressure of academic work accessioned by the unprecedented strike action.

My heartfelt appreciation equally goes to my lecturers Dr. K. R. Adeboye, Dr. S. A. Reju, Mrs. N. Ngbachi, Mr. Kola, Mr. Kobara for all they did to make us pass through the course successfully.

In addition, I am grateful to Joy Olisadebe Tayo and Pastor Biodur for allowing me to learn on them intermittently through the two-years of the course.

A. O. FALEKULO

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His contribution, understanding and directives were certainly the bedrock on which this write up became a reality. In addition, I'm grateful to Joy Olisadebe, Tayo, and Pastor Biodun for allowing me to lean on them intermittently through the two-years of the course and especially during the project.

BAYO FALEKULO

CHAPTER ONE

INTRODUCTION

1.1 **PROBLEM DEFINITION** :- Computer simulation should begin with formulation of a problem since there is little benefit to be derived from experiments that solve simulations. Thus this project is to simulate a sorting process in the processing method of Bank notes using a computer system. It is to determine how this Banknotes can be sorted in clean and unclean pockets of 100 pieces during processing and not only just the normal counting and shielding that is the case now.

1.2 **Objective :-** To simulate Digital devices for currency processing by a computer system in such a way that Bank Notes sorted into clean and unclean pockets of 100 pieces during counting. This will make the system to be completed in the sense that it can now count, sort and shred at the same time.

Since a simulation model is a simplified representation of a system mathematical/logical relations and operational rules built in the computer program,

using a specific computer code, the truth tables of all the logical devices involved in modelling will be written out explicitly.

SCOPE OF LIMITATIONS :- To plan computer simulation, applicable to Digital systems, one must, draw heavily on the tools of experimental modelling logical computation, circuit realization and computer programming. Thus this project will cover Analysis of Digital Devices and circuits, sequential and combinational circuits, logic gates and up to electronic devices.

It is ideal that information are obtained about the SIMULATION requirements before its actual planning. It is essential to collect and reduce date about the system to suitable form for use in simulation respectively in descriptive form.

The data processed can be used to formulate mathematical/logical models that describe the behaviour of the system concern.

Some problems may be encountered during the process of data collection and processing.

1.4 **Sequence + Methodology** :- The sequence and methodology involved in this project will be in the order of Data generation and collection, Definition of the Technology involved in the project and it availability, in case of necessity to fully design and produce.

The project will simulate Digital logic devices parallel on a computer system to generate outputs that will create a sorting level for Bank notes during processing. Basically sensors will be applicable in this process depend solely on data generation and analysis. Below are the important functions of data processing for implementing computer simulation experiments:-

(a) Collection and processing of real world data.

(b) Estimation of Simulation parameters from real world data.

(c) Evaluation of the model and parameter estimate

(d) Formulation of computer program.

(e) Analysis of simulated data.

CHAPTER TWO

2.0 LITERATURE REVIEW

A Central Bank is a major institution in any modern economy and it is quit important to the functioning of both the private sector and fiscal operations of the government. Central Banking is an activity separated from ordinary commercial banking in that a central bank, in general, does not have little transaction with the public, dealing mainly with the government and commercial banks.

The Central Bank of Nigeria was

2.0 LITERATURE REVIEW

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The Central Bank of Nigeria was established in 1958 under an Act of Parliament known Central banking functions and serve

as the pivotal national financial institution. These traditional functions are

(i) The issuance of legal tender currency in Nigeria.

(ii) Maintenance of external reserves to safeguard the international value of that currency.

iii) Promotion of monetary stability and a sound financial structure in Nigeria and acting as banker and financial adviser to the Federal Government of Nigeria.

The developmental roles of the CBN embrace surveillance of the economy and active promotion of capital formation necessary for acceleration of the above functions of the Central Bank of Nigeria is under the Governor who is the HEAD of the Bank assisted by 5(five) DEPUTY GOVERNOR and 18(eighteen) departmental directors.

One of the departmental Directors, DIRECTOR CURRENCY OPERATIONS. Department Controls the currency processing office.

2.1 The main functions of the currency processing office is to process all currency notes deposited by the commercial Banks at all Central Bank offices for processing. The office is expected not only to ascertain the correctness of notes as lodged, but also to defect forged notes as well as dirty notes for destruction.

2.2 There are automatic currency processing machines ISS300P(S) installed in branches to process these notes. To simulate DIGITAL SYSTEMS for currency processing encompasses knowing the analysis of some Digital Devices, circuits. Sequential and combinational circuits, logic gates and opto-electronics devices.

Computer simulation and modelling is directed towards finding satisfactory solution to practical problems. Computer simulation is a numerical techniques used to conduct experiments on digital computers which involves certain types of mathematical and logical models that describe the behaviour of some components over an extended period. A simulation model is a simplified representation of system mathematical and logical relations and operational rules built in the computer program using a specific computer code. language of the simulation languages), thus either the general purpose compiler or the special purpose simulation language.

Computer simulation os therefore a technique by which programs are written and used in a computer system desired language to solve some problems of interest; like the behaviour of some machines ranging form small components (integrated circuits) to the most complicated industrial machineries.

2.3 WHY COMPUTER SIMULATION

It would be wise for a simulation engineer to ask some few questions as the basis for his experimental verification. Thee questions are:

(a) Can the exact or satisfactory approximation to the solution of the problem be obtained.

(b) Would compute simulation cost less to solve the problem?

(c) Would it be easily interpreted by those who are likely to use the simulation result

These questions should however be answered almost correctly before choosing computer simulation as the basis for using simulation in any discipline is man's increasing quest for knowledge about the future. This search for knowledge consists of problems ranging from observation of physical system formulation of a model, production of the output up to conducting experiments to test the validity od the model.

Due to the ability of computer simulation to overcome the difficulties mentioned above, it is chosen for the fact that:

(a) Makes it possible to study and experiment with the complex environments;

(b) Makes it possible to study the effect of certain components changes in the operation of a system by making alterations on the system behaviour;

(c) Observation of the stimulated system may lead to its better understanding.

(d) Designing simulation model suggest possible effect of changes which can be tested vice simulation before implementation;

(e) It makes the study of dynamic system possible at all times.

(f) It helps to foresee the bottlenecks behind the operation of new systems.

2.4 PLANNING COMPUTER SIMULATION

To plan computer simulation applicable to Digital Systems, one must, draw heavily on the tools of experimental modelling logical computation circuit realization and computer programming.

(i) Formulation of the Problem: Computer simulation should begin with formulation of a problem since there is little benefit to be derived from experiments that solve simulations. Thus, before one can begin work on any simulation experiment, one must decide on the objective of our research and on a set of criteria for valuating the degree to which our objectives are fulfilled by the experiments.

(ii) **COLLECTION AND PROCESSING OF REAL WORLD DATA**

It is ideal that information are obtained about the simulation requirements before its actual planning. Some problems involved in collecting and reducing data to a suitable form for use in simulation experiments include a descriptive and quantitative information (DATA) about the system to be investigated. The data processed can be used to formulate mathematical/logical models that describe the behaviour of a given system. Existing models of the system to be stimulated can be improved. Data that have been reduced to a final form can be used to estimate parameters of the operating characteristics of the system Data helps to test the validity of a simulation model. However, some of the important functions of data processing for implementing computer experiments are:

(a) Data collection

(b) Data recording

(c) Data conversion

(d) Data transmission

(e) Data manipulation

(f) Output data report

(iii) ESTIMATION OF SIMULATION PARAMETERS FROM REAL WORLD DATA

Once the appropriate data have been collected from the system with a number of logical models describing the behaviour of the system being formulated, then the significance of the estimated values of the parameters of the models are tested.

(iv) EVALUATION OF THE MODEL AND PARAMETER ESTIMATE

Having collected the set of logical models describing the behaviour of our system and estimated the parameters of the operating characteristics on the basis of observation taken from readily available information and then go ahead to make initial values judgement of the simulation model, this represent first stage in testing simulation experiments prior to the actual computer runs. Thus, testing the assumptions made or the input that will be programmed into the computer.

(v) FORMULATION OF COMPUTER PROGRAMME

The formulation of computer programme for the purpose of conducting computer simulation experiments wit models of the system under study. It requires that special considerations be given to the items below

(a) Flow chart

(b) Computer code

(c) Error checking

(d) Data input and starting conditions

(e) Data generation

(f) Output report.

The step in writing a computer simulation program involves formulating a flowchart, outlining the logical sequence of events to be carried out by the computer in generating the time path of the endogenous variable of our model.

The actual computer code for which to run the experiments on a computer is considered.

Finally, the most important consideration is made on the types of output report needed as an information about the behaviour of our simulated system.

3.3 BINARY NUMBER SYSEM

This is a number that contains only two permissible digits or states. The two states are 1 and 0, switch position. The 1 and 0 binary correspond to the possibilities ON and OFF.

In electronic logic circuits, the numbers 1 and 0 usually corepsond to two esily distinguished coltage levels. Other number systems are the decimal, binary codd decimals, HEXA-Decimal code numbers among others.

Digital computers use binary words such as 32 or even 64 bits put into groups of 8-bits called bytes. Intermediate printouts may then be presented in hexadecimal numbers for diagnostic purpose without going through binary-to-decimal conversion.

3.4 BINARY DIGITAL SYSTEMS

Binary digital system are for switching circuits capable of making logical decisions that have only two states. The basic logic units are define as AND, OR and NOT gates.

The basic logic gates configuration is given below

(a) AND gate: This is equivalent to connecting switching in SERIES. All the switches must be closed for the light to glow, i.e for a positive output. This can be expressed

in logic form as A.B = X; where the dot (.) sign stands for AND see diagram and table below.

(b) OR gate: This is equivalent to connecting switvhes in parallel. Only one of the swithes or all are needed to be closed for the light to glow.
It is represented as A+B = X; where A + B = stands for A or B. See diagram and table below.

(c) NOT gate: This acts as an inverter. It negates whra state the input has; it is single gate whose output is the opposite of the input. It is expressed X = A where A = NOT A. See diagram and table below.

FLIP - FLOP: Any devices with two stable states is called a bi-stable. A flip-flop is a bistable with a circuit that has two stable states.

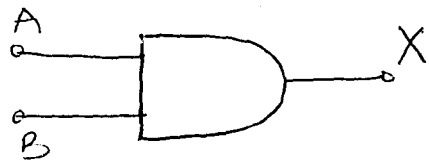
It can be constructed by connecting two NAND gates or two NOR gates in series with a feedback. A flip-flop is regarded as a memory device use to store a binary data depending on the output, see diagram and table below.

AND gate

Truth Table

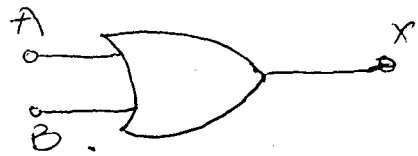
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Circuit diagram



OR gate

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1



NOT gate

A	X
0	1
1	0

FLIP FLOPS

CLOCKED RS FLIP FLOPS:

CLOCKED FLIP FLOPS: A flip-flop can be clocked to be able to store information (either set it or reset it) at any time and hold the stored information for any length of time. See diagram which?

Since the R/S has two inputs only, it becomes disadvantageous to implement R/S for storing high bits data.

D-Flip-Flop: A delay flip-flop is used with a single data input. It however prevents the D-input from reaching the Q-output the clock pulse occurs.

A mathematical tool needed for the manipulation, simplification and understanding of complex logic operations and then solving for the unknown is the BOOLEAN ALGEBRA. Boolean Algebra is meant to reduce complexity in construction and cost of digital equipments.

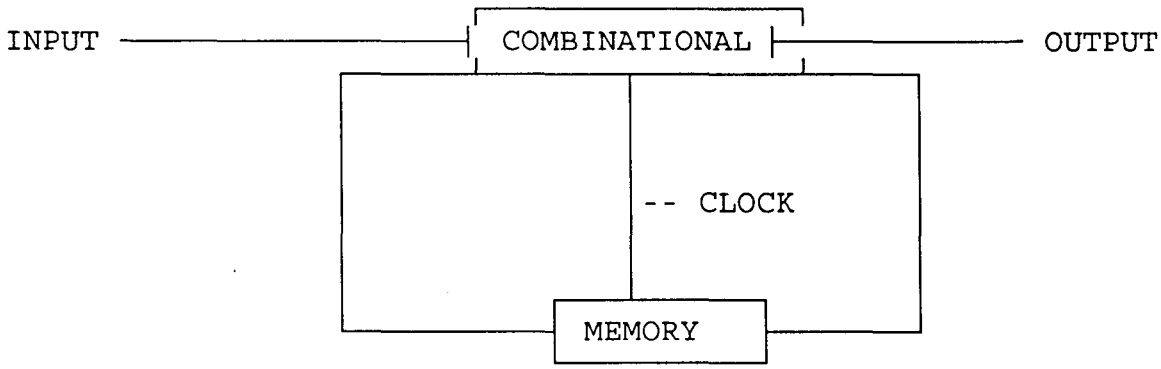
3.5 COMBINATIONAL AND SEQUENCIAL CIRCUITS

Considering the best possible approach to designing circuits with maximum output it's necessary to determine whether to use combinational circuits or sequential circuits. Since information can be stored in a sequential circuit, it becomes important to consider reasons why it is chosen for most applications.

COMBINATIONAL CIRCUITS: A group of interconnected logic gates comprises a combinational circuit whose output values at any particular time depends only on the combination of the input values at the same time. Although some gates may attain this

final value at slightly different times than others because of the propagation delay. The combinational circuits reach a final state determined entirely until the input changes.

SEQUENTIAL CIRCUITS: If a memory unit is added to a combinational circuit, a sequential circuit is formed. The memory unit accepts some outputs fromt he combinational circuits, stores them for some amount of time and feed them back into the combinational circuits as additional inputs. A into the combinational circuuits as additional inputs. A current output state depends on previous one or more inputs as well as on current input state.



There are several methods of implementing flip-flops and each involves cross-coupled configuration to provide the feedback that creates latching effect. Most seqential circuits contain many flip-flops that are synchronised together by a

master clock to provide no time intervals between clock pulses at the final states and to provide system timing to accomodate both short and long operations.

3.5 **REGISTERS** : These are group of flip-flops connected together internally to operate as a single unit device for temporary storage of binary data. There are two types of registers classified according to their mode of operations. These are COUNTERS AND SHIFT REGISTERS.

(a) SHIFT REGISTERS: These are made of group flip-flops that respond to a set of control signal. All the elements are clocked at the same time.

(b) COUNTERS : These are made of flip-flops of N possible states; each state is associated with a number. Contents of the counters are interpreted as numbers mostly in binary or BCD codes. The counter can decrement or increment the count after N counts by reverting to its initial state and thus repeating the counting cycle.

CHAPTER FOUR

FLOWCHARTS

FLOWCHARTS:- Is a diagrammatic representation of an algorithm i.e. Its a visual picture which gives the steps of an algorithm and also the flow of control between the various steps.

Flowchart symbol

Special symbols are used to depict different operations specified in an algorithm.

(i) **Terminal Symbols**

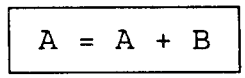
start

It is used for starting, halting or terminating a process. These must be only one starting point in a flowchart and at least (and preferably only) one stopping pt.

(ii) **I/O symbol**

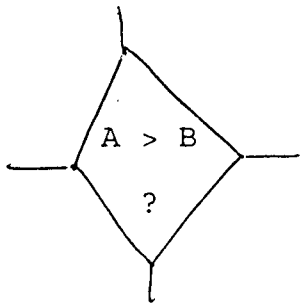
It is used for input or output operation

(iii) **Process symbol**



It is used for an operation that caused a change in some value. This includes arithmetic operations, assignment operation e.g. initialising a variable with a value or exchanging the value of 2 variables.

(iv) **Decision Symbol**



Used to indicate point in the flow chart when decision are to be made.

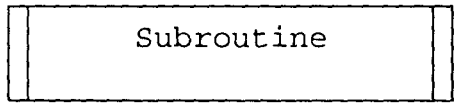
(v) Connecting Symbol

This is used to indicate a connection to another part of the chart and can be used for both entry or exit points within a flowchart.

(vi) **Arrow Symbol**

This indicate direction or flow of logic

(vii) **Pre-defined process symbol**



This symbol represents computer processing which is comples enough to require a separate flowchart to describe it. The block contains the names of a separately charted routine(generally called a subroutine).

The approach where hardware and its algorithms are tested by means of real-time simulation is in some fields known as HARDWARE-in-the-loop simulation. Hardware-in-the-loop computer simulation studies are frequently used in some areas of industry.(e.g. aerospace) for testing system components when full system tests may be limited in scope because of constraints in terms of safety or availability of the complete system for testing purposes.

The basis for hardware-in- the-loop realization is real-time simulation. If we have a computer software with real-time simulation capabilities and a computer with the necessary communications abilities (A/D, D/A converters for communications with analogue signals or a digital part for communication with digital systems). then we have, together with the chosen hardware for testing, all the necessary items to perform hardware-in-the-loop simulation.

Control Algorithm testing via hardware-in-the-loop Simulation study

Real-time abilities if a process control system are limited by the hardware (pc). It enables a sampling time of 50ms or more (depending on problem sampling size) which is satisfactory for many process control applications especially in process control applications where time constants are

generally larger than in, for example, many applications in the aerospace area. The purpose of the extension of the SIMCOS language with real-time simulation capabilities was to enable inexpensive real-time simulation on personal computers

Simulation in real-time and hardware-in-the-loop

Simulation within the SIMCOS simulation language is made possible by:Simulation

(i) Synchronization of the Simulation algorithm with the real-time.

(ii) Use of less time consuming integration methods,

iii) Realization of input/output data acquisition.

The real-time Simulation concept

The basic concept of real-time simulation which is illustrated above, can be explained as follows.

The Synchronization of the simulation algorithm is introduced in the simulation procedure (continuous time integration method) which controls the time loop. The

synchronization initialization is executed before the time loop starts while the real-time is executed at the beginning of the time loop. the synchronized with the computer clock and thus with the real-time at the first synchronization procedure. The synchronization modules enables the receiving and transmitting of signals within the communication intervals on the other hand, the sorting algorithm ensures that at every time loop, data acquisition is the first operation and then operations on the data follows.

Input and output data acquisition facilities are provided through the use of suitable peripherals unit such as: instrument modules for data acquisition (A/D and D/A converters, digital input-output modules) and a time base generator. Therefore the configuration of the personal computer must be expanded with suitable hardware for data acquisition involving peripheral units such as those mentioned above.

The MMC-90 controller with the implemented control algorithm was connected to a PC computer which simulated the process model through AD/ and D/A converters (in our case PCI 20000 hardware of the Burr Brown Company was used).

The MMC -90 controller is a digital controller which means that it operates with digital signals. However, because it is aimed for the industrial environment it has inputs and outputs for analogue signals which are converted in discrete signals (and from discrete signals for outputs) within the controller. The total hardware-in-the-loop procedure is as follows. The personal computer generates digital signals which are converted into analogue form by external converters. These analogue signals are then sampled by MMC-90 converters. The MMC-90 controller by the aid of its own converters generate analogue outputs signals which are discretised by external converters and transmitted to the simulation program.

The sampling of external and internal MMC-90 converters were no synchronized. The controllers sampling period was 10 times larger than sampling period of external converters which was 100 ms. This was done to ensure that the MMC-90 controller "feels" the simulated process like continuous one which means that the information contained in signal from computer should be equal (or comparable) to the information from the real plant. The process model does not exhibit large dynamic complexity and consequently there were no numerical problems associated with the D/A and A/D converter resolution.

A/D and D/A software routines for hardware-in-the-loop simulation have been included in the SIMCOS language library. They were written in FORTRAN and partially in assembler in the form of functional subroutines.

Time synchronization of A/D and D/A conversions is ensured through system variable checking with the SMICOS language. The sampling time which is defined in the simulation program by the user himself has to be executed on multiples of integration routines computation time .

As stated above, there are two possible ways to simulate the process : By an Euler integration method as a continuous system or as a discrete system. The Euler integration method and continuous system simulation was chosen because the complexity of the model does not require more simple discrete system simulation (with shift operators only). Beside this, the process model is developed as continuous model. Before the application of Euler integration method with a stepwise which equals the sampling rate of external converters the comparative simulation study of the nonlinear process model behaviour with different integration methods and stepwise was performed. It showed that the necessary accuracy is achieved with the selected integration method and stepwise.

One could conclude that according to simple integration within and chosen stepsize the simulation can be realized also in some standard programming language. However, the general purpose simulation language with the real-time abilities assures the user friendly environment for the hardware-in-the-

loop simulation and minimize computer programming effort.

An example of the control system simulation results which illustrate control objectives specified by designers as shown in figs.4 and 5.Disturbance rejection control to a step disturbance at 5000s on both inputs was simulated. The set points for both outputs were determine as the values of the process outputs without disturbances. The molar compositions of distillate obtained by the real-time simulation with hardware-in-the-loop are given in fig.4 while the control signals are given in fig.5. From simulation results it can be concluded that SIMCOS simulation programme is a successful replacement of distillation column for the control testing purpose. A further discussion about results from the control point of view is here omitted because it is not the issue of this paper.

During the building up an running of the hardware-in-the-loop testing procedure many advantages as well as some considerations for the testing procedure were observed .

The advantages are as follows:

(i) The ability to test the controller without having to use the plant itself .

(ii) The possibility of controller parameter turning is given without involving the plant itself.

iii) The influence of hardware limitations can be observed.

Some consideration for the described testing procedure are as follows . The process constraints (including actuators and sensors) and other nonlinearities of importance are to be included into control testing.

Normalizing of input and output controller signals because of converter resolutions and domain is necessary.

The computer simulates a continuous time process and controller has to receive signals from computer which contain the same information as would signals from the actual process otherwise unexpected results can be obtained at the stage of control commissioning. Consequently, he controller sampling time has to be longer than the integration routines computation time of the real-time simulation.

The simulation and controller can be run faster than real time at a predetermined fixed multiple provided that the time scale required is within the range of the controller and converters (e.g. sampling time is not too fast).

CHAPTER FIVE

5.0 CONCLUSION

The use of a general purpose simulation for real time hardware-in-the-loop simulation studies offers in expensive possibilities for multi variable and other complex algorithm testing. A lot of implementation issues can be encountered and solved, before the control system is implemented on the real system.

While in other fields, hardware in than loop testing of control algorithms and hardware is not uncommon, this approach is not frequently used in process control. However, it gives some advantages to control design, especially with implementations of more advanced control Algorithms as shown above. The loop procedure is to replace and connect the control Hardware to be tested to the computer via recess any converters.

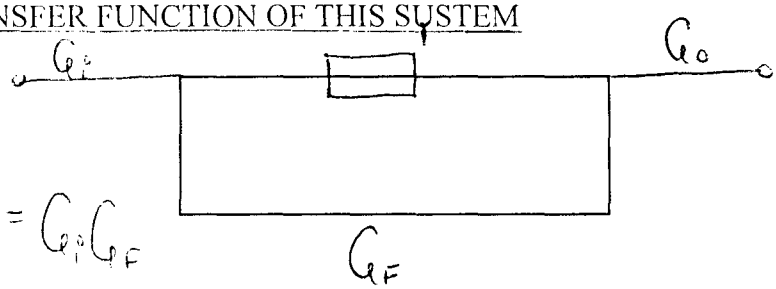
Furthermore, the speed up factor in real time simulation using multi processor resources strongly depends on the architecture of the multiproccessor system, on the interconnection between parallel processors.

Therefore the asynchronisation I/O communication bus has been paid attention. Parallel signal processors TMS 320C4o allow simultaneous CPU and I/O operations using high-speed 8-bits communication ports and 6-channels DMA coproccessor. DMA coproccessor maximises sustained CPUs performance providing continuous data transfer between processors over I/O ports without any CPU intervention.

PERFORM 'CE OF THE DEVELOPED

ALGORITH AND PROGRAMME

THE TRANSFER FUNCTION OF THIS SYSTEM



is $G_o = G_i G_F$

where go = T function of the output Go= T.F of input from the above, it can be noticed that

The efficiency of the paralled simulation algorithm is higher than the efficiency of the sequental algorithm. Information exhange during Bank notes (BN) processing in the paralled is more efficient, since messa s are volved.

The output Go happened to be an improvement on the old system.

Simulation analysis showed that hardware in the loop systems go a long way in system evelopment and appraisal.

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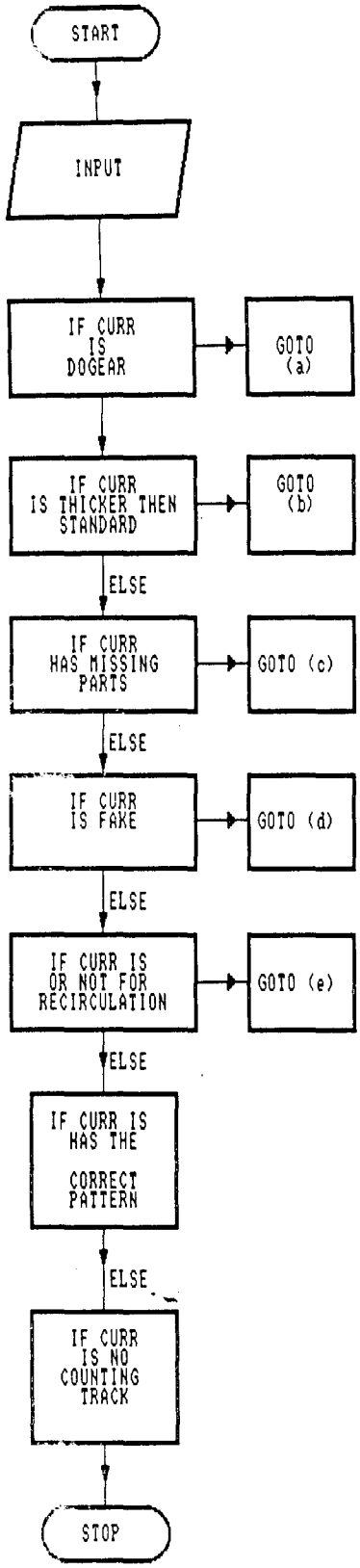
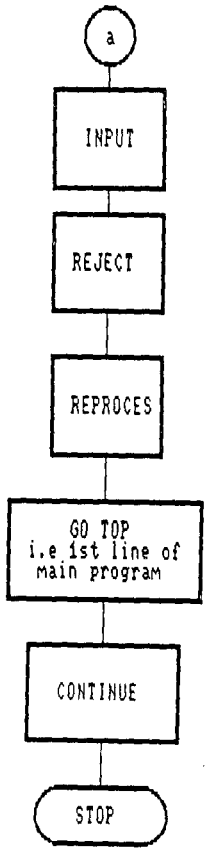
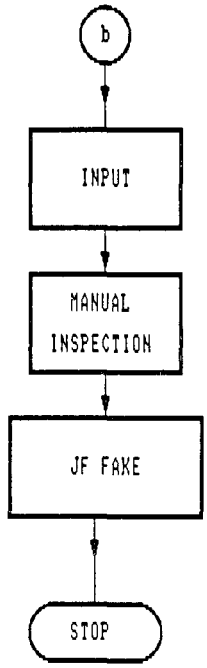
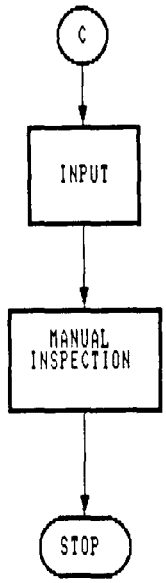
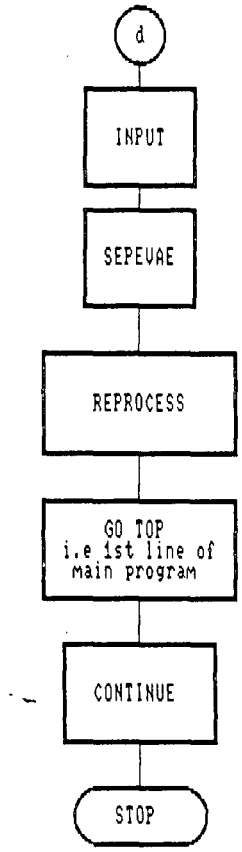

START
INPUT
IF CURR IS DOGEAR
GOTO (a)
IF CURR IS THICKER THEN STANDARD
GOTO (b)
ELSE
IF CURR HAS MISSING PARTS
GOTO (c)
ELSE
IF CURR IS FAKE
GOTO (d)
ELSE
IF CURR IS OR NOT FOR RECIRCULATION
GOTO (e)
ELSE
IF CURR IS HAS THE CORRECT PATTERN
ELSE
IF CURR IS NO COUNTING TRACK
STOP


a
INPUT
REJECT
REPROCES
GO TOP
i.e ist line of
main program
CONTINUE
STOP


b
INPUT
MANUAL
INSPECTION
JF FAKE
STOP


C
INPUT
MANUAL INSPECTION
STOP


d
INPUT
SEPEVAE
REPROCESS
GO TOP
i.e ist line of
main program
CONTINUE
STOP

Therefore the asynchronisation I/O communication bus has been paid attention. Parallel signal processors TMS 320C4o allow simultaneous CPU and I/O operations using high-speed 8-bits communication ports and 6-channels DMA coproccessor. DMA coproccessor maximises sustained CPUs performance providing continuous data transfer between processors over I/O

CHAPTER FIVE

5.0 CONCLUSION

The use of a general purpose simulation for real time hardware-in-the-loop simulation studies offers in expensive possibilities for multi variable and other complex algorithm testing. A lot of implementation issues can be encountered and solved, before the control system is implemented on the real system.

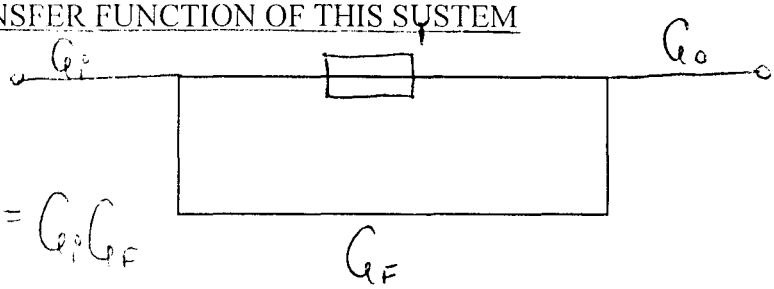
While in other fields, hardware in than loop testing of control algorithms and hardware is not uncommon, this approach is not frequently used in process control. However, it gives some advantages to control design, especially with implementations of more advanced control Algorithms as shown above. The loop procedure is to replace and connect the control Hardware to be tested to the computer via recess any converters.

Furthermore, the speed up factor in real time simulation using multi processor resources strongly depends on the architecture of the multiproccessor system, on the

PERFORM 'CE OF THE DEVELOPED

ALGORITH. AND PROGRAMME

THE TRANSFER FUNCTION OF THIS SYSTEM



is $G_o = G_i G_F$

where go = T function of the output Go= T.F of input from the above, it can be noticed that

The efficiency of the paralled simulation algorithm is higher than the efficiency of the sequental algorithm. Information exhange during Bank notes (BN) processing in the paralled is more efficient, since messa_ s arc volved.

The output Go happened to be an improvement on the old system.

Simulation analysis showed that hardware in the loop systems go a long way in system evelopment and appraisal.

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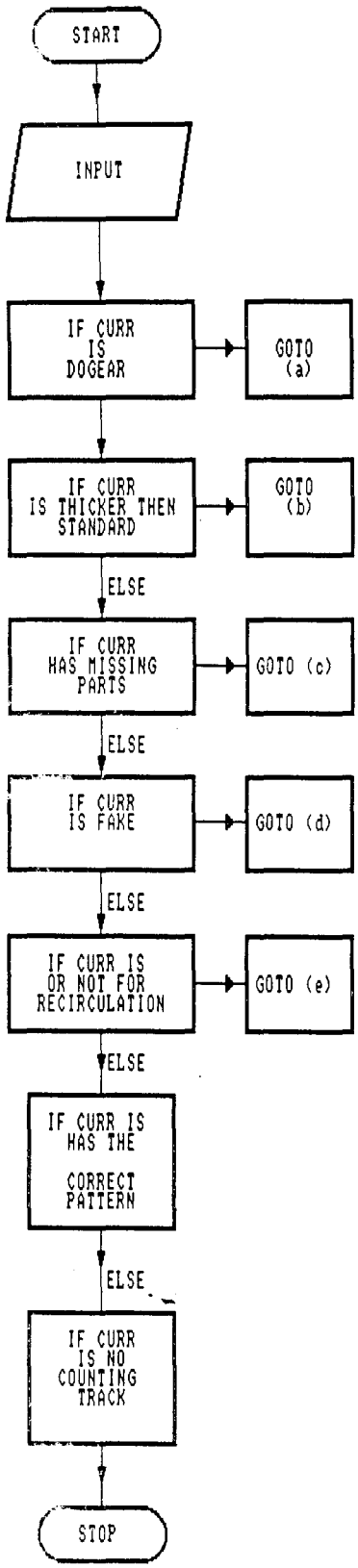
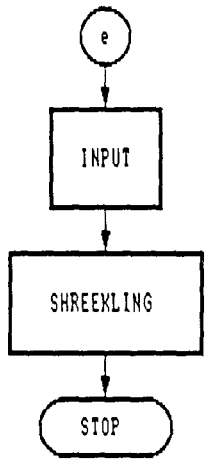
2. Computer standards and Interphase by Prof. S. Takaba Dept. of Communications networks. Tokyo Engineering University, Japan.

3. Service information for automatic Sensors of ISS 300 P(S) by Giescke & Devrient of Germany.

4. Introduction to Simulation practice by J. Idler.

5. Digital Technology by M.R. Tortler


START
INPUT
IF CURR IS DOGEAR
GOTO (a)
IF CURR IS THICKER THEN STANDARD
GOTO (b)
ELSE
IF CURR HAS MISSING PARTS
GOTO (c)
ELSE
IF CURR IS FAKE
GOTO (d)
ELSE
IF CURR IS OR NOT FOR RECIRCULATION
GOTO (e)
ELSE
IF CURR IS HAS THE CORRECT PATTERN
ELSE
IF CURR IS NO COUNTING TRACK
STOP


e
INPUT
SHREEKLING
STOP

```
1 REM THIS PROGRAM IS ABOUT AUTOMATIC BANK NOTES PROCESSING AND
SHREDDING.
REM    IT INVOLVES USING A SIMULATION TECHNIQUE REFERRED TO AS
REM     HARDWARE-IN-THE-LOOP METHOD
REM    IT SORTS BANK NOTES INTO FIT, UNFIT, MANUAL INSPECTION
REM             AND SHREDDING COMPACTMENTS.
REM *** THIS PROGRAM IS WRITTEN BY ADEBAYO FALEKULO *****
COLOR 14, 6
PRINT "THIS PROGRAM IS ABOUT AUTOMATIC BANK NOTES PROCESSING AND
SHREDDING."
PRINT "IT INVOLVES USING A SIMULATION TECHNIQUE REFERRED TO AS"
PRINT "HARDWARE-IN-THE-LOOP METHOD"
PRINT "IT SORTS BANK NOTES INTO FIT, UNFIT, MANUAL INSPECTION"
PRINT "           AND SHREDDING COMPACTMENTS."
SLEEP 3
REM SECTION TO TEST IF THE CURRENCY IS DOGEAR
CLS
LOCATE 10, 26
PRINT "IS THE CURRENCY DOGEAR [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
15  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 15
END IF

IF UCASE$(Q$) = "Y" THEN
    GOSUB 100
END IF

REM SECTION TO TEST IF THE CURRENCY IS THICKER THAN STANDARD
CLS
LOCATE 10, 18
PRINT "IS THE CURRENCY THICKER THAN STANDARD [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
16  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 16
END IF
IF UCASE$(Q$) = "Y" THEN
    GOSUB 200
END IF

REM SECTION TO TEST IF THE CURRENCY HAS ANY MISSING PART
CLS
LOCATE 10, 19
PRINT "IS THE CURRENCY HAS ANY MISSING PART [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
17  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 17
END IF
```

```
IF UCASE$(Q$) = "Y" THEN
    GOSUB 300
END IF

REM SECTION TO TEST IF THE CURRENCY IS FAKE
CLS
LOCATE 10, 27
PRINT "IS THE CURRENCY FAKE [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
18  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 18
END IF
IF UCASE$(Q$) = "Y" THEN
    GOSUB 300
END IF

REM SECTION TO TEST IF THE CURRENCY IS FIT FOR CIRCULATION
CLS
LOCATE 10, 21
PRINT "IS THE CURRENCY FIT FOR CIRCULATION [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
19  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 19
END IF
IF UCASE$(Q$) = "N" THEN
    GOSUB 500
END IF

REM SECTION TO TEST IF THE CURRENCY HAS THE CORRECT PATTERN
CLS
LOCATE 10, 18
PRINT "IS THE CURRENCY WITH THE CORRECT PATTERN [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
20  Q$ = INPUT$(1)
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 20
END IF
IF UCASE$(Q$) = "N" THEN
    GOSUB 500
END IF

REM SECTION TO TEST IF THE CURRENCY IS ON THE COUNTING TRACK
CLS
LOCATE 10, 21
PRINT "IS CURRENCY ON THE COUNTING TRACK [Y/N]"
REM SECTION TO CHECK IF THE ANSWER IS CORRECT
21  Q$ = INPUT$(1)
```

```
IF UCASE$(Q$) <> "Y" AND UCASE$(Q$) <> "N" THEN
   PRINT CHR$(7)
   GOTO 21
END IF
IF UCASE$(Q$) = "N" THEN
    GOSUB 500
END IF
GOSUB 600
103 CLS
COLOR 30
LOCATE 12, 24: PRINT "THANK YON FOR USING THIS PACKAGE"
CLS
104 END

100 REM SUBROUTINE FOR DOGEAR
CLS
LOCATE 12, 9
PRINT "...Since the currency is dogear, Please Reject and Reprocess."
REM SECTION TO HOLD DOWN THE EXECUTION
SLEEP 1
LOCATE 14, 26
PRINT "Press any key to continue..."
K$ = INPUT$(1)
RETURN 1

200 REM SUBROUTINE FOR THICKNESS
CLS
LOCATE 12, 12
PRINT "...Please seperate the currencies and Reprocess."
REM SECTION TO HOLD DOWN THE EXECUTION
SLEEP 1
LOCATE 14, 26
PRINT "Press any key to continue..."
$ = INPUT$(1)
ETURN 1

00 REM SUBROUTINE
LS
OCATE 12, 19
RINT "...Please rémove the currency from others."
EM SECTION TO HOLD DOWN THE EXECUTION
LEEP 1
OCATE 14, 26
RINT "Press any key to continue..."
$ = INPUT$(1)
ETURN 104

)0 REM SUBROUTINE FOR SHREDDING
LS
)CATE 12, 4
INT "...the currency is not fit for recirculation, Please shred it."
```

```
REM SECTION TO HOLD DOWN THE EXECUTION
SLEEP 1
LOCATE 14, 26
PRINT "Press any key to continue..."
K$ = INPUT$(1)
RETURN 104

600 REM SUBROUTINE FOR COUNTING
CLS
LOCATE 12, 27
PRINT "Please count it in hunderds"
REM SECTION TO HOLD DOWN THE EXECUTION
SLEEP 1
LOCATE 14, 26
PRINT "Press any key to continue..."
K$ = INPUT$(1)
RETURN 103
```