DESIGN AND CONSTRUCTION OF A REGULATED MULTIPLE OUTPUT DC POWER SUPPLY

BY

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(M.ENG/SEET/2008/1930)

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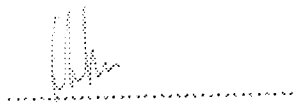
THESIS SUBMITTED TO THE POSTGRADUATE SCHOOL, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGERIA IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF THE DEGREE OF MASTER OF ENGINEERING (M.ENG) IN ELECTRICAL AND ELECTRONICS ENGINEERING (ELETRICAL POWER AND MACHINES)

APRIL, 2012

DECLARATION

I, EMELOGU, Godswill Chikezie (M.Eng./SEET/2008/1930) hereby declare that this thesis titled 'Design and Construction of a Regulated Multiple Output DC power supply' is a collection of my original research work and it has not been presented for any other qualification anywhere. Information from other sources (Published or Unpublished) has been duly acknowledged.



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CERTIFICATION

This thesis titled : Design and Construction of a Regulated Multiple Output DC Power Supply' by EMELOGU, Godswill Chikezie (M.ENG/SEET/2008/1930) meets the regulations governing the award of the degree of Master of Engineering (M.ENG) of the Federal University of Technology, Minna and is approved for its contribution to scientific knowledge and literary presentation.

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ABSTRACT

The project presents the design and construction of a regulated multiple DC output power supply based on the principle of pulse width modulation. Pulse width modulation involves variation of ON and OFF times of a switching element in response to variation in either load demand or input voltage. DC power supplies based on this principle are called switch mode power supplies and have become the dormant architecture for DC power supplies, due to their capability to handle variable large loads, high efficiency, relatively small size and weight. Switch mode power supplies have many variants. In this project, a DC power supply circuit, using forward converter topology and utilizing a power MOSFET for switching was designed simulated in MULTISIM environment and constructed. The forward converter which was designed for a maximum output of 222W made up of three DC outputs performed satisfactorily under standard test conditions.

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CHAPTER ONE

1.0 INTRODUCTION

Every electronic appliance or circuit requires a DC power supply. But the most commonly available power supply is the alternating power supply at 240-V (single phase) 50Hz. This alternating power supply therefore has to be rectified to DC. Two most common methods of obtaining the DC power supply include:

i. Use of linear regulators

ii. Switch Mode Power Supply (SMPS)

Historically linear regulator was the primary method of producing a regulated output voltage. It operates by reducing a higher input voltage down to the lower output voltage by linearly controlling the conductivity of a series pass power device in response to changes in its load. This result in a large voltage being placed across the pass unit with the load current flowing through it and consequent high I^2R loss. This loss causes the linear regulator to only be 30 to 50 percent efficient. That means that for each watt delivered to the load, at least half a watt has to be dissipated in heat. The cost of the heat sink actually makes the linear regulator uneconomical above 10-watts for small applications. Below that point, however they are cost effective in step down applications. Furthermore it can only be used as a step down regulator which means that the output voltage can never be greater than the input voltage (Brown, 1990).

The switch mode power supply operates by chopping up the applied DC input voltage into rectangular AC waveforms whose frequency equals the switching frequency. The switch can be a power MOSFET or a bipolar transistor .The ON and OFF times of the switch is determined by the width of the gate control pulse generated by an IC

controller. The ratio of the ON time to the total operating time (on time plus off time in a cycle is called the duty cycle of the switch.

The problem of low efficiency , heavy weight, single output and large space requirement of power equipments based on linear regulator principle, due to use of iron core transformers , has led to the development of D.C power supplies based on switch mode techniques. These power supplies are called switch mode power supplies (SMPS).Switch mode power supplies circumvent all of the linear regulator's short comings according to (Brown, 1990) , as follows:

i. The switch mode power supply exhibits efficiencies of 68 to 90% regardless of input voltage, thus drastically reducing the size requirement of the heat-sink and hence its cost.

ii. Because the power switches used operate at their most efficient points, saturation and cut off, the power switches can deliver many times their power rating to the load and the less expensive components can be used.

iii. Since the input voltage is chopped into an ac wave form and placed into a magnetic element, additional windings can be added to provide for more than one output voltage.

iv. For transformer isolated switching supplies ,the output voltages are independent of input voltage which means that the input voltage can vary above and /or below the level of the output voltages without affecting the operation of the supply.

v. Since the frequency of operation is very much greater than 50/60Hz line frequency, the magnetic and capacitive elements used for energy storage are much smaller and the cost to build the switching supply becomes less than the linear supply at the higher power levels.

The fundamental difference between linear and switching regulator is that a linear regulator regulates a continuous flow of current from the input to the load in order to maintain a constant load voltage,. The switching regulator regulates the same current flow by chopping up the input voltage and controlling the average current by means of the duty cycle.

The technique for controlling the on and off times of the switch mode power supply is *pulse width modulation.* In this technique, the time of switching ON and OFF of the power switch is controlled in such a way that the output voltage is determined by the ratio of 'ON' time to total time (ON time + off time).When a higher load current is required, the percentage of on time is increased to accommodate the change (Brown, 1990).

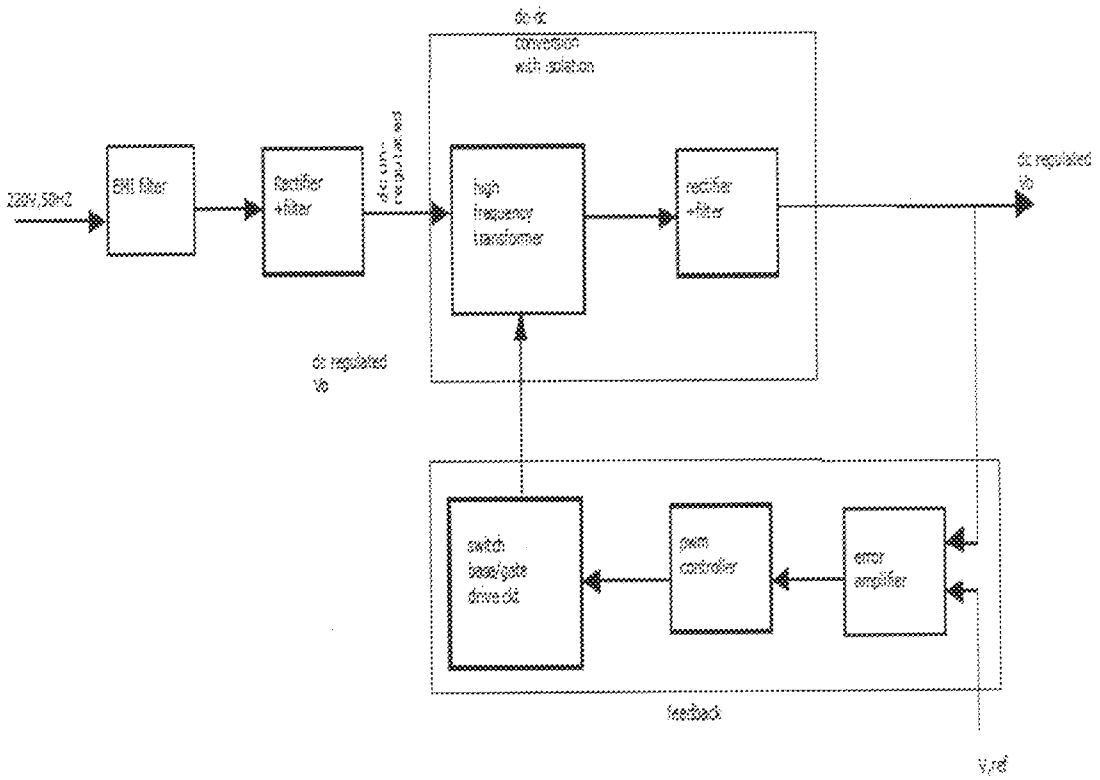

Figure 1.1 Schematic of a Switch Mode Power Supply

1.1 Statement of the problem

From the brief description of the two methods of obtaining DC power supply it has been found out that the performance of switch mode supplies in terms of efficiency, size, weight and possibility of multiple outputs outweighs the linear electronics based DC power supplies. This project will therefore be based on Switch Mode Power Supply technique.

1.2 Aim of the project

The aim of this project is to develop a SMPS that can produce regulated multiple DC output voltages of 6V, 12V, 24V using a switching element driven by pulse width modulation technique.

1.3 Motivation

There is so much demand for switch mode power supplies all over the world Nigeria inclusive. Further- more the heart of any switch mode power supply is the pulse transformer. But pulse transformers are not available in the market as ready- made but must be designed and built for each power supply. In Nigeria there are so many burnt pulse transformers found in both computer and television power packs that are treated as wastes.

The project aims at rewinding the burnt pulse transformer to meet specific requirements and to develop local capacity for building switch mode power supply at a reduced cost that are suitable for use in laboratories in secondary schools and universities.

1.4 Scope of Work and Limitations

This work shall be limited to the design and construction of a 222W DC power supply having three DC outputs of 6V, 12V and 24V, using a forward converter topology. The topology chosen is the forward converter. This is because the forward converter is capable of handling the calculated power of 222 watts efficiently.

1.5 Organization of Report

This report deals with the design, simulation and construction of a forward

Converter and has been divided into five chapters.

i. Chapter one deals with the general introduction of regulated AC to DC conversion with emphasis on pulse width modulation technique.

ii. Chapter two highlights various topologies of a switch mode power supply and their important features. The chapter therefore deals with a review of relevant literatures on switched mode power supplies.

iii. Chapter three concentrates on the theory and design of switch mode power supply using pulse width modulation technique and using forward converter topology. Design of the various sub-circuits making up the forward converter was made and the component values of each calculated.

iv. Chapter four deals with the simulation and construction of the designed circuit and testing of same.

v. Chapter five discusses the results obtained above in addition to making recommendations and conclusions there from.

CHAPTER TWO

2.0 LITERATURE REVIEW

The alternating current supplied to homes and businesses is practical and useful for many reasons. Power can be generated at whatever voltage that is most convenient, stepped up to a higher voltage for efficient transmission and then stepped back down to a level appropriate for consumers through the use of transformers. As an ever increasing number of applications are taken over by electronic methods, the need arises for the efficient conversion to DC voltage levels required by semi-conductor based devices. The conversion from AC Power Supply to DC Power Supply is carried out using appropriate DC Power Supply circuits.

DC Power Supplies are circuits that generate a fixed or controllable magnitude of DC voltage from the available alternating current power. Integrated circuit chips used in electronic circuits needs standard DC voltage of fixed magnitude.

The proper operation of electronic devices ranging from personal computers to military equipment and industrial machinery depends on the performance and reliability of DC Power Supplies.

2.1 Pulse Width Modulation (PWM)

Switch mode power supplies are dynamic systems, which mean that they do not assume an operating point instantly when an input parameter is changed. In view of this, if we want the switch mode power supply to have a dynamic behavior different from the natural behavior, the duty cycle must be controlled. There are two common methods of

control for pulse width modulation switching power Supplies. They are either current or voltage based depending on what is sensed, to provide constant output voltages.

2.1.1 Voltage mode control:

This is where only the output voltage is sensed in order to maintain its required voltage level. This type of control can be recognized by the output Of the error amplifier going into a comparator that compares the error voltage with the ramp created by the oscillator section of the IC. The comparator converts the error voltage into a pulse width modulated waveform in order to drive the power switches in a pulse width modulated on/off fashion. The most common voltage mode control is a fixed frequency method of control shown below, (Brown 2000).

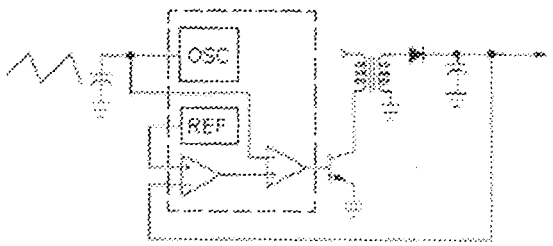

Figure 2.1 Voltage Mode Control (Brown, 2000)

2.1.2 Current Mode control :

Current mode control senses not only the output voltage, but the amount of current that flows through the inductor or transformer. When the output demands more power, the controller allows more current to enter the inductor or transformer. Conversely if the input voltage suddenly changes, it is immediately detected by the controller and appropriate response is given, keeping the output voltage at its required level. The common method of current mode control is called turn on with clock current mode

control. This means that the frequency of operation is determined by an oscillator whose only purpose is to start each ON cycle.

The current mode control is very fast and provides a very good transient response time. Examples of controllers used in this mode of control include UC 3842/3/4/5, and MC34023.

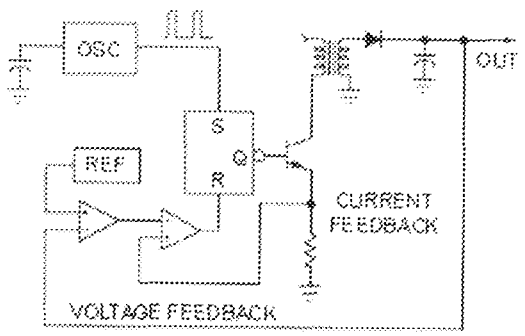

Figure 2.2 Current Mode Control (Brown, 2000)

2.1.3 Variable Frequency: Using variable frequency, the average output voltage can be varied in such a way that the ON time is fixed and OFF time is varied or the ON time is variable, OFF time is fixed and both ON time and OFF time are made variable. Variable frequency PWM poses a serious problem in output filter design, as it is difficult to design a filter if the desired frequency response is unknown. For this reason, fixed frequency form of PWM is preferred.

2.1.4 Fixed frequency: In fixed frequency pulse width modulation, the total time for a cycle is kept constant. Output is varied by changing both the ON time and OFF time for a switch such that $T_s = T_{on} + T_{off}$ (where T_s is the time for a full cycle).

Figureure 2.3a below shows the block diagram of a circuit for generating pulse width modulation (PWM). In the Figure, the fixed frequency PWM control signal to the

switches is generated by comparing an amplified error signal with some repetitive wave form which may be a saw tooth. The error signal is obtained by comparing the output voltage of the converter with some precise reference corresponding to the desired output value. From Figure 2.3b, it is seen that when the repetitive wave form is greater than the error signal the switches are turned on and when the error signal is of a lower value than the saw tooth wave form, the switches are turned off.

The fixed frequency PWM can be provided by a number of means such as:

i. Analogue circuit built up of individual components

ii. Analogue PWM IC

    i. Digital means, using micro Controllers (Mohan, *et al* 2003).

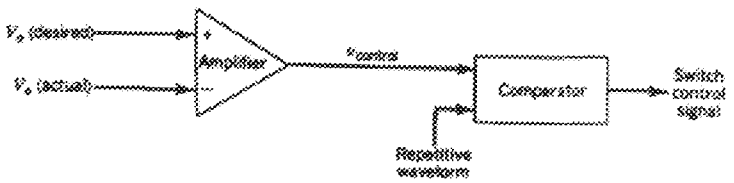

Figure 2.3a: Pulse Width Generation Circuit (Mohan *et al* 2003)

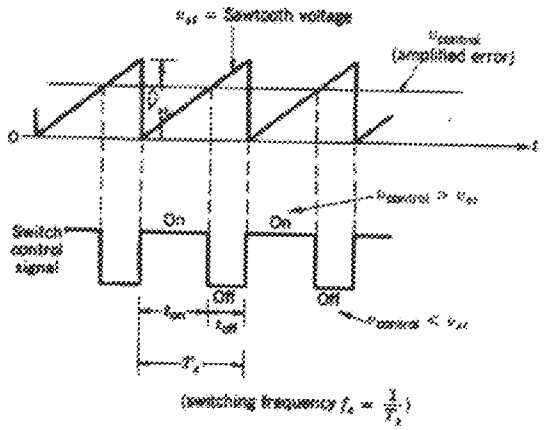

Figure 2.3b: Comparator Signals (Mohan *et al* 2003)

2.2 Continuous and Discontinuous Modes.

In continuous conducting mode current flows throughout the switching cycle and in the discontinuous mode the current through the inductor will drop to zero for a period of time during the switching cycle.

The choice of the mode of operation is dependent on individual application; discontinuous mode is preferred for low load currents and will utilize small inductor values.

On the other hand, continuous mode will provide greater output power, but the continued flow of current will require larger values of inductance for high input voltages.

Inductance value for a switching regulator must be high enough to prevent excessive current and low enough to store sufficient energy in the core.

2.3 Topologies of SMPS

Switch mode power supplies may be divided into isolated and non-isolated, with their principle of operation being broadly analogous,(Mohan ,*et al. 2003)*. In the non isolated topology only the semi-conductors provide the DC isolation from the input to the output. Semi-conductors have relatively low voltage breakdowns and exhibit the worst *meantime between failures (MTBF)* of the components within any given power supply.

The non isolated topologies include the following:

i. buck converter

ii. boost converter

iii. buck boost converter

The isolated topologies use transformers as a means of isolation and are therefore called transformer isolated topologies. The transformer isolated topology relies on a physical dielectric barrier provided by wire insulation and/or insulated tape. The energy passes through a non-conducting ferrite core material prior to reaching the output. The transformer insulation can withstand many thousands of volts before it fails and does provide a second dielectric barrier in the event of a semi-conductor failure. Other functions of the transformer include the following:

i. step up or step down function

ii. Possibility of adding multiple outputs to the power supply without additional separate regulators for each output.

The above factors make the transformer isolated switch mode power supply topology an attractive choice for virtually all applications.

There are many different architectures of the transformer isolated topology. All have general areas of optimization and include:

i. Fly-back

ii. Forward

iii. Push Pull

iv. Half bridge

v. Full bridge

The fly-back and the forward converter constitute the foundation of the switched mode power supplies while the rest are derived from them. We shall now examine each of the topologies as follows:

2.3.1 Forward Converter

The forward converter has four functional elements namely, a power switch for creating the rectangular waveform, a rectifier, a series inductor, and a capacitor as shown in Figure.2.4, (Brown, 1990). The power switch may be a power transistor or a MOSFET. In between the power switch and filter section there may be a transformer for stepping up or down the input voltage as in transformer isolated forward converters. The shunt diode, series inductor and shunt capacitor form an energy storage reservoir whose purpose is to store enough energy to maintain constant the load voltage and current over the entire off-time of the power switch. The power switch serves only to replenish the energy lost to the load during its off time.

The operation of the switch can be divided into two periods. The first is when the power switch is on. During this period the load current passes from the input source through the inductor to the load and back again through the return (ground) lines to the input source. During this time the diode is reverse biased. After the power switch turns off, the inductor still expects current to flow through it. The former current path through the input source is now open circuited and the freewheeling diode now begins to conduct, thus maintaining a closed current loop through the load. When the power switch now turns on again the voltage presented to the filter serves to turn off the free -wheeling diode. Because forward current is always flowing through the inductor, the topology is called forward *converter.*

The amount of energy being delivered to the load is controlled by the duty cycle of the power switch ON time. This may vary any -where between 5 and 95 % duty cycle.

$$V_{out} = V_{in} \times D \qquad (2.1)$$

Where V_{out} = output DC voltage

V_{in} = maximum input DC voltage

D= duty ratio of power switch

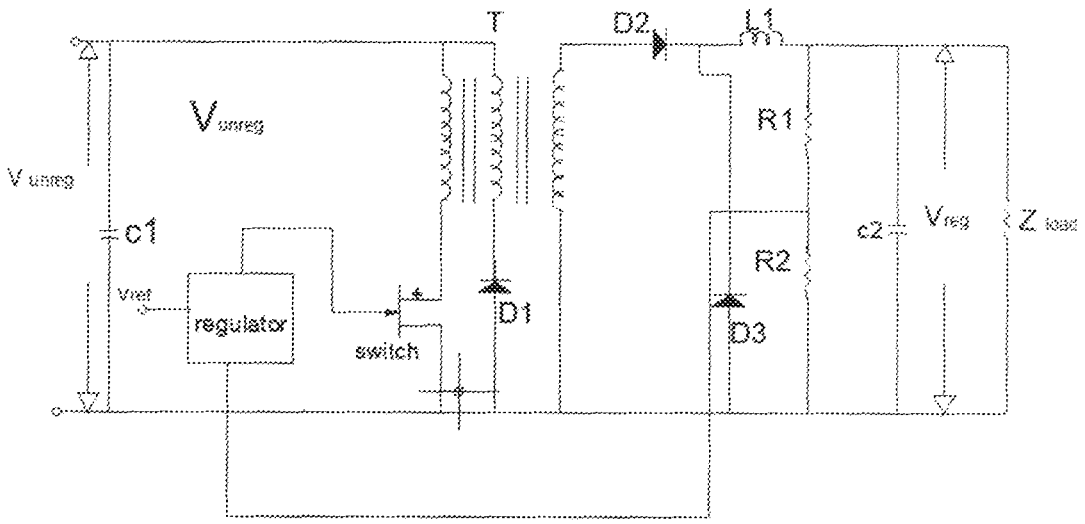

Figure 2.4: Forward converter (Mohan, *et al* 2003)

2.3.2 Push Pull

The push-pull topology is a transformer isolated forward mode converter and therefore has the buck style L-C filter network on its output Here the transformer is used to step down the chopped input voltage waveform before it is presented to the output L-C filters. The push pull transformer does not store any energy and the output current is drawn when either power switch is conducting. The push pull topology utilizes a centre tapped primary winding. The input line is connected to the centre tap and a power switch is connected to both ends of the winding. The secondary voltage is full wave-rectified and then presented to the out -put LC filter.

In push pull topology two power switches share the switching function. The switches do not simultaneously conduct but alternate back and forth on alternate cycles. The two

sides of the primary are wound in the same direction but the current flows in the opposite direction. This result in the flux generated within the core material being driven in both the positive and negative flux polarities, and therefore utilizes the core material most efficiently, and consequently uses a smaller core size. The two switches share the responsibility of eliminating the heat that is generated in them. This feature renders the push pull topology capable of generating many hundreds of watts in its output.

Parameters of the push pull converter can be calculated thus:

Peak drain current=I_{pk} = $\frac{1.4 \times P_{out}}{V_{in(min)}}$ (2.2)

Peak drain voltage = $V_{pk} = 2 \times V_{in\ (min)}$ (2.3)

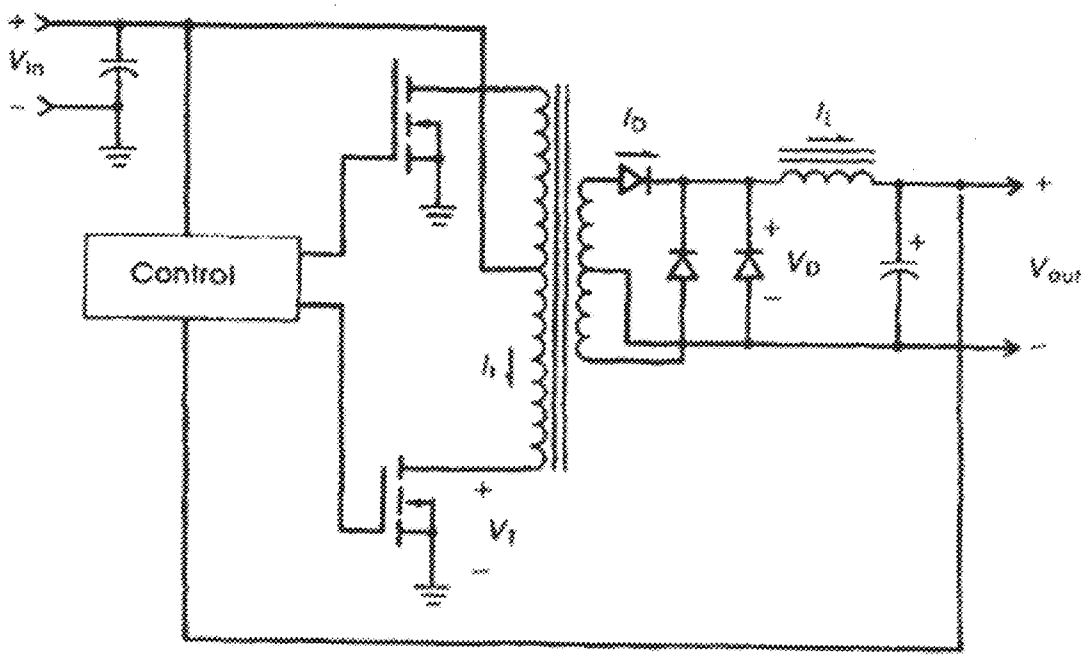

Figure 2.5 Push Pull Converter (Mohan, *et al.* 2003)

2.3.3 Fly Back Converter:

Fly back converters have the same four basic components as the forward converter except that they have been subtly re-arranged. The operation of the fly back can be broken into two periods. When the power switch is on, current is drawn through the inductor, which causes energy to be stored within its core material. The power switch then turns off. Since the current through an inductor cannot change instantaneously, the inductor voltage reverses (or flies back), this causes the rectifier to turn on, thus dumping the inductor's energy into the capacitor. This continues until all the energy stored in the inductor during the previous half-cycle is emptied. Since the inductor voltage flies back above the input voltage, the voltage that appears on the output capacitor is higher than the input voltage. Note that the only storage for the load is the output filter capacitor. This makes the output ripple voltage of fly back converters worse than their forward mode counterparts.

The duty cycle in an elementary fly back-mode supply is 0 to 50 percent. This restriction is due to the time required to empty the inductor's flux into the output capacitor. Duty cycles within transformer-isolated fly back regulators can sometimes be larger because of the effects of the turns ratio and the inductances of the primary and the secondary.

During the switch's off-time, the inductor will empty itself before the start of the next power switch conduction cycle. Since the volt-time products of the inductor charging and discharging cycles must be equal and the output of the non isolated fly back converter must be higher than the input voltage, the resulting relationship is

$$V_{out} = V_f + V_{fbk} \quad V_{in}\,(1+T_{on}/T_{fbk}) \qquad (2.4)$$

At the minimum operating voltage, the duty cycle reaches 50 percent and T_{fbk} equals the total operating period minus the "on-time".

Where:

V_{in} is input DC voltage

V_{out} is the converter output voltage

V_{fbk} is voltage across the transformer when the power switch is off.

T_{fbk} is time during which the power switch is not conducting.

T_{on} is time during which the power switch is conducting.

Parameters of the fly back topology can be calculated thus:

$$\text{Peak drain current} = I_{pk} = \frac{5.5P_{out}}{V_{in}} \tag{2.5}$$

$$\text{Peak drain voltage} = V_{pk} = V_{out}(N_1/N_2) + V_{in} \tag{2.6}$$

$$\text{Approximate primary inductance, } L_{pri} = \frac{V_{in(min)} \times DC}{I_{pk}} \tag{2.7}$$

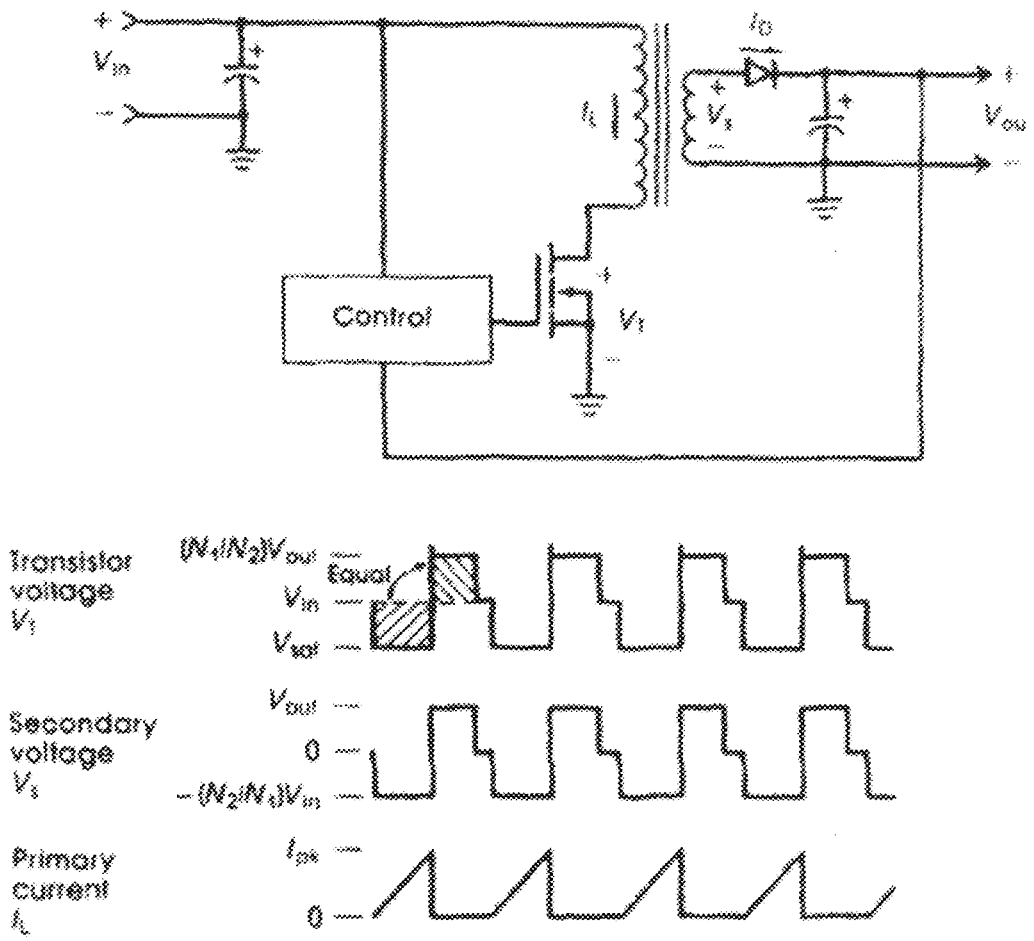

Figure 2.6: Fly Back Converter and Waveform (Mohan *et al* 2003)

2.3.4 Half Bridge Converter

The half bridge converter is another form of a transformer isolated forward converter. The half bridge converter has only one primary winding, which is connected between a pull up /pull down arrangement of power switches and the centre node between two series capacitors wired between the input voltage and ground. In this topology the transformer core is operated in the bipolar flux mode of operation. The capacitor centre node voltage sits at approximately one half of the input voltage, and the power switches present the other end of the primary winding with alternative input voltage and ground signal. This means only half of the input voltage appears across the primary winding.

This results in an average and hence peak current twice that of the push pull converter with similar output power. Thus the half bridge converter is not as suitable for very high power operation as the push pull converter .It however has the advantage of an intrinsic self core balancing. The core balancing is achieved by the capacitors. The centre node voltage will adjust in the direction of higher flux density within the transformer. This reduces the voltage across the primary in the direction of impending saturation, which in turn, centres the B-H excursions within the transformer, eliminating the need for an expensive high speed over current sensing circuit.

One major difficulty encountered in using the half bridge converter topology is how to drive the upper power switch whose emitter or source is riding on a high voltage AC waveform its drive signal must be referenced to this AC waveform. The common method is to drive the upper switch with an isolated pulse transformer and reference the secondary to the AC wave form. Parameters of the half bridge converter are calculated thus:

$$\text{Peak drain current, } I_{pk} = \frac{2.8P_{out}}{V_{in(min)}} \tag{2.8}$$

$$\text{Peak drain voltage, } V_{pk} = V_{in(max)} \tag{2.9}$$

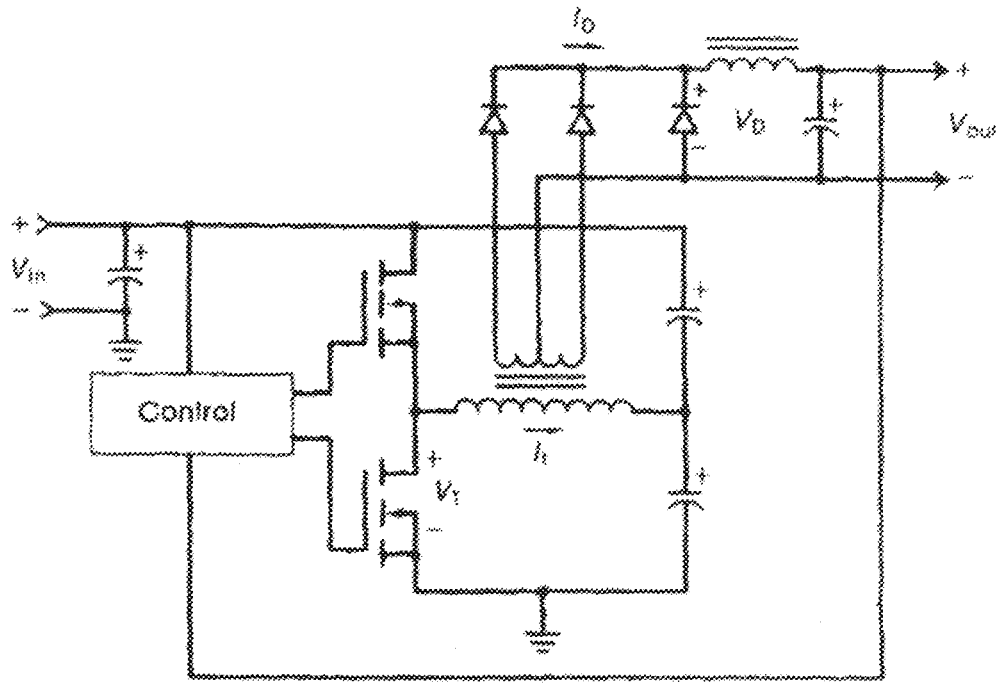

Figure 2.7: Half Bridge Converter (Brown, 1990)

2.3.5 Full Bridge

The transformer flux of the full bridge converter, like the other double ended converters, is driven in both the positive and the negative polarities. Its performance with respect to output power is significantly improved over that of the half bridge converter. This is because the balancing capacitors are replaced with another pair of half bridge style power switches identical to the first pair. This time two of the four power switches are turned ON simultaneously. During one conduction cycle either (1) the upper left and the lower right power switches or (2) the upper right and the lower left switches are turned ON. Each associated pair of switches conduct on alternate cycles. This place the full input voltage across the primary winding, thus reducing the peak currents in the primary for any output power compared to the half bridge converter. This effectively doubles the maximum power handling capability of this topology over the half bridge. Also since the power switches are driven in pairs, the designer needs only to add two more

secondary to the half bridge drive transformer to accommodate the added pair of switches. The control circuitry remains unchanged. Core balancing is achieved by placing a small non polarised capacitor in series with the primary winding. The average DC voltage across the capacitor reduces the voltage across the primary winding in the direction of impending saturation.

The parameters are calculated thus:

Peak drain current, $I_{pk} = \frac{1.4P_{out}}{V_{in(min)}}$ (2.10)

Peak drain voltage, $V_{pk} = V_{in}$

The problem of driving the upper power switches is present also in the full bridge topology.

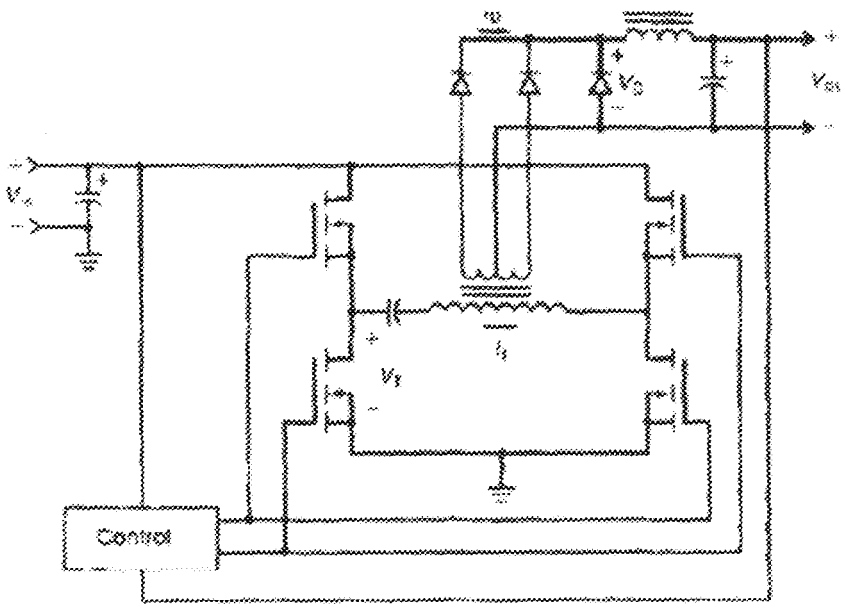

Figure 2.8 Full Bridge Converter (Brown, 1990)

2.4 Defining the Topology and Control Method

The cost benefits of a fly back design begin to diminish at power levels above 100W, a forward converter topology therefore appears an appropriate choice for the expected output power of 222W. A single switch or two switch forward converters is a good choice, (Walker, 2005).

A single switch forward converter is usually limited to a 50% duty cycle to allow time for the transformer to reset its volt-second product, and therefore uses either a reset winding or an RCD circuit to clamp the reset voltage to acceptable levels. The power switch (MOSFET) then sees approximately $2 \times V_{in}$. Push pull designs also have the problem of at least $2 \times V_{in}$ voltage rating. Since this requirement is expensive an alternative approach is preferred. This alternative is the use of two MOSFET switches each connected at each end of the transformer primary to connect to the positive rail and ground. When they turn off during the reset period, each end of the primary winding automatically traverses to the opposite rail thus placing the opposite polarity on the winding to satisfy the volt-second equalization. No clamp winding is needed and instead, only clamping diodes are required. Table 1 below shows a comparison of the different topologies, (Walker, 2005).

Table 2.1: Comparison of the Different Topologies

Topology	Power level	Benefits	Drawbacks	Cost
Fly-back	<100w	Low parts count, single magnetic, wide input voltage range, low output power.	Poor efficiency at high power levels, high peak currents, cross regulation problems, high voltage power switch.	Lowest.
1-switch forward	100w to 500w	Medium output power, good cross regulation with coupled inductor, potential for >5% duty cycle.	Limited input range, power switch $=2\times V_{in}$, transformer reset.	Moderate.
2-switch forward	100w-500w	Medium output power ,power switch= V_{in} , coupled inductor, transformer reset	Limited input range, TOP FET drive circuit required 5% duty cycle limit, larger inductor value.	Moderate.
Half bridge	100w to 500w	Medium output power, power switch= V_{in} , coupled inductor, max duty	Limited input range, TOP FET drive, volt-second balance of	moderate

		cycle<100%	transformer, centre tapped transformer.	
Full bridge	>500w	Resonant switching can improve efficiency, power switch=V_{in}, coupled inductor, very high output power, max duty cycle<100%, efficient transformer design.	4-power switches, high TOP FET drive, volt second balance	
Push pull	25w to 200w	Good core utilization, coupled inductor, both switches ground referenced, small output inductor, max duty cycle	Power switch $=2\times V_{in}$,limited input range, centre tapped primary, volt second balance	moderate

Forward converters offer a cost effective solution to fill the void created between the low power fly-back converter and the more complex high power bridge types. Utilizing continuous inductor current operation, the forward converter uses a much lower peak current than its fly-back counterpart. Considering all the above, a single switch forward converter is considered more appropriate for our power requirement of 222W and will therefore be discussed further.

Practical transformers have magnetizing inductance. When the MOSFET switch is off, both the primary and secondary of the transformer will have no current, only the magnetizing inductance has current which is now trapped due to the switch being off. A path must therefore be created during switch off times to bring the magnetizing current to zero. During this off times negative voltage polarity, large enough is applied to bring the magnetizing current back to zero. This has given rise to core reset techniques shown in Figure 2.9 below, (Michael, 2006) employed in forward converters to give either a conventional or RCD forward converter.

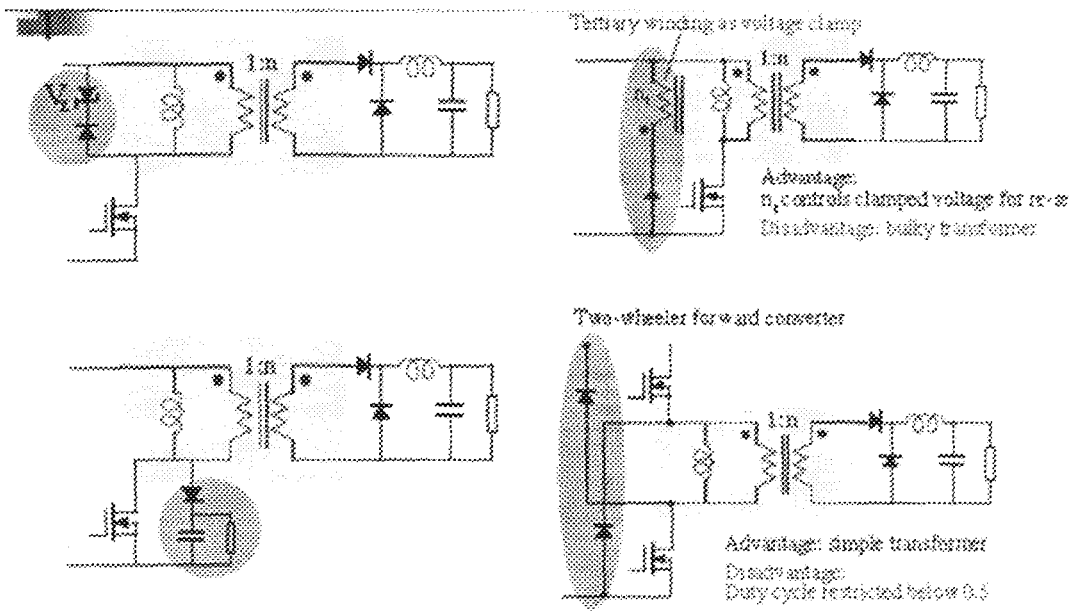

Figure 2.9: Transformer Core reset Techniques (Michael, 2006).

2.4.1 Conventional Forward Converter

The conventional single switch forward converter uses a reset winding which increases the size and weight of the forward converter. In conventional forward converters designing for operation over a wide input voltage range increases the problem of the converter and results in inefficient power supply. Therefore very narrow duty cycles are

needed at high line voltage to meet the 50% maximum duty cycle clamping at low line operations. The forward converter of Figure 2.4 is reproduced below.

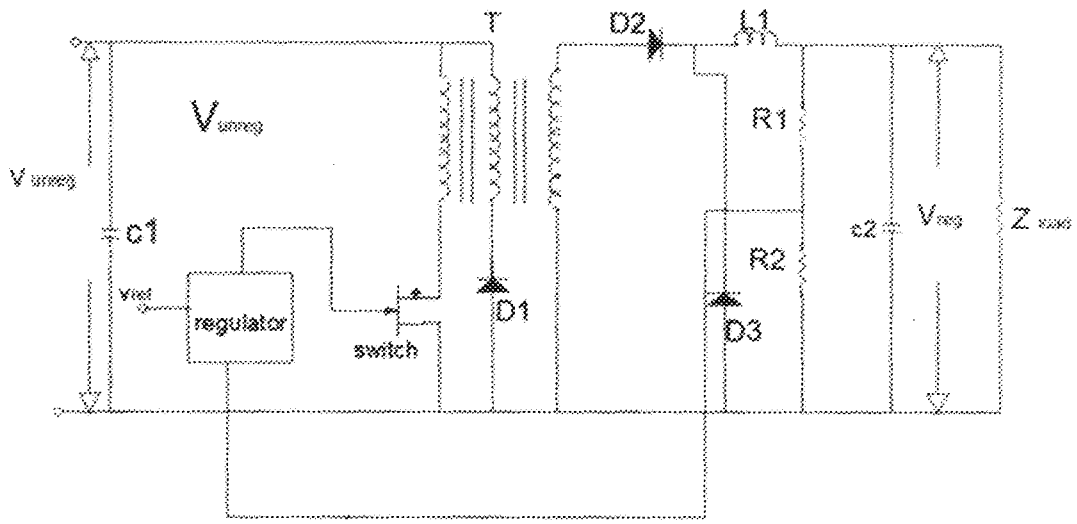

Figure 2.10: Forward Converter

2.4.2 RCD Type Forward Converter

This employs resistor, capacitor and diode to develop a varying clamp voltage into which the magnetising energy is dissipatively discharged. Generally the RCD is the preferred choice for wide input ranges especially low voltage input designs where a higher clamp/reset voltage still yields manageable low voltage semi conductors. It also facilitates maximum duty cycles which can stretch beyond the 50% milestone, useful in wide range input supply designs.

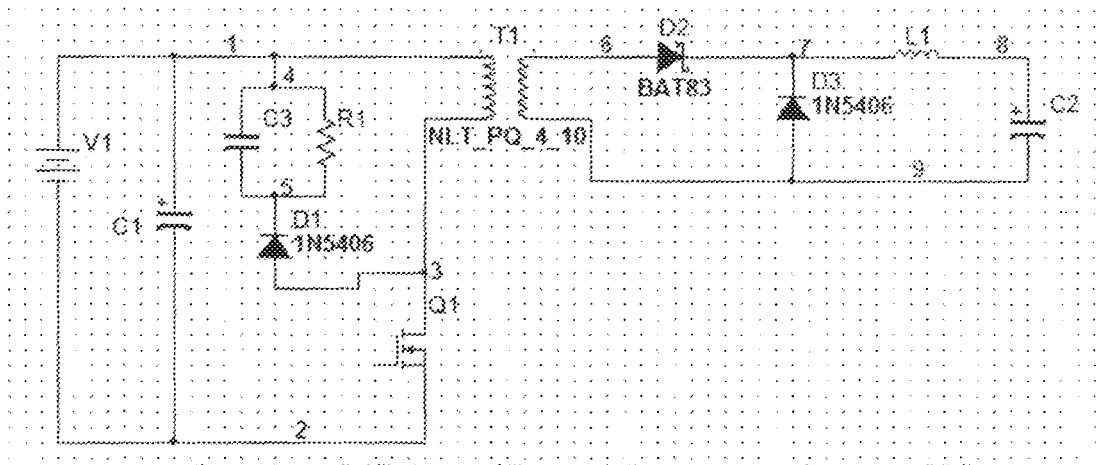

Figure 2.11: RCD Type of Forward Converter (Andreycak, 1994)

For RCD the applied volt-second product must be equal to the reset volt –second product according to the following relationships:

$$V \times D = V_{reset} \times (1 - D) \quad (2.11)$$

$$V_{reset} = \frac{V_{in(max)} \times D_{max}}{(1 - D_{max})} \quad (2.12)$$

$$V_{ds} = V_{in} + V_{reset} \quad (2.13)$$

So that for a maximum input voltage of 342V and maximum duty cycle of 0.45, reset voltage is $\frac{342 \times 0.45}{1 - 0.45} = 342$ V so that the reset voltage becomes:

V_{ds}, MOSFET drain to source voltage rating=342 +342 = 682V .A 10% margin is normally provided for increased safeguard, resulting in a 718.2V rating.

2.4.2.1 RCD Clamp Voltage

Low line voltage and light loads determine the clamp capacitor and resistor value needed for proper reset of transformer. The exact capacitance required is determined by the acceptable clamp capacitor ripple voltage as it causes heating due to the ripple current flowing in the capacitors' equivalent series resistance (ESR). A good initial

estimate for the analysis is 10V of ripple at light loads since the ripple will only increase with load.

Duty cycle will vary from the maximum at low input voltage to the minimum at high input voltage but the volt-second product remains constant Many combinations of clamp capacitance and resistance values are possible for a given application depending on the ratio of light to full load current, ratio of leakage to magnetising inductances, maximum clamp voltage, transformer primary capacitance and MOSFET switch capacitance (Andreycak , 2001).

2.5 Single Switch Forward Converter Design

Figure 2.12 below shows the block diagram of a single switch forward converter. Each of the component blocks will be discussed.

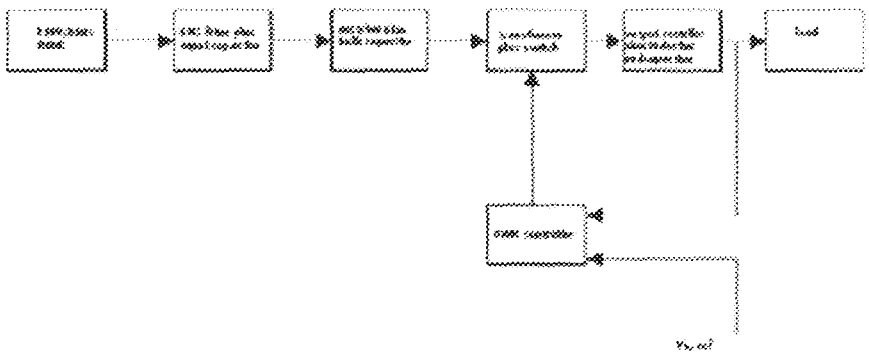

Figure 2.12 Block Diagram of a Forward Converter (Mohan *et al*, 2003)

2.5.1 Electromagnetic Interference (EMI) Filter

The EMI filter section is composed of a small L-C filter between the input line and the rectifier. L1 and C1 filter net-work acts as a high frequency radio –frequency interference filter, which reduces the conducted high frequency noise leaving the

switching supply back into the input line. The low pass cut off frequency of this filter should not be more than 2 to 3 times the supply's operating frequency. The second purpose of the L1-C1 filter is to add small impedance between the input line and the bulk input capacitor and mainly reduces any dangerous transient voltages and allows the bulk input filter capacitor to absorb the destructive energies from the input line spikes with little chance of exceeding any of the components voltage ratings (Brown 1990).

2.5.2 Bulk Input Filter Capacitor:

This capacitor is always large in value and has the responsibility of storing the high and low frequency energy required by the supply during each conduction cycle of the power switch. It is usually made up of at least two capacitors, an electrolytic or tantalum capacitor for the current components at the supply's switching frequency and a ceramic capacitor for the switching frequency harmonics. Without both a low frequency electrolytic and high frequency ceramic type capacitors, the supply would starve for high frequency current and voltage and adversely affect the supply's stability.

2.5.3 Full Wave Rectifier:

The first building block in the dc power supply is the full wave rectifier. The purpose of the full wave rectifier is to produce an uncontrolled rectified ac output from a sinusoidal ac input signal as shown in Figure 2.13 below.

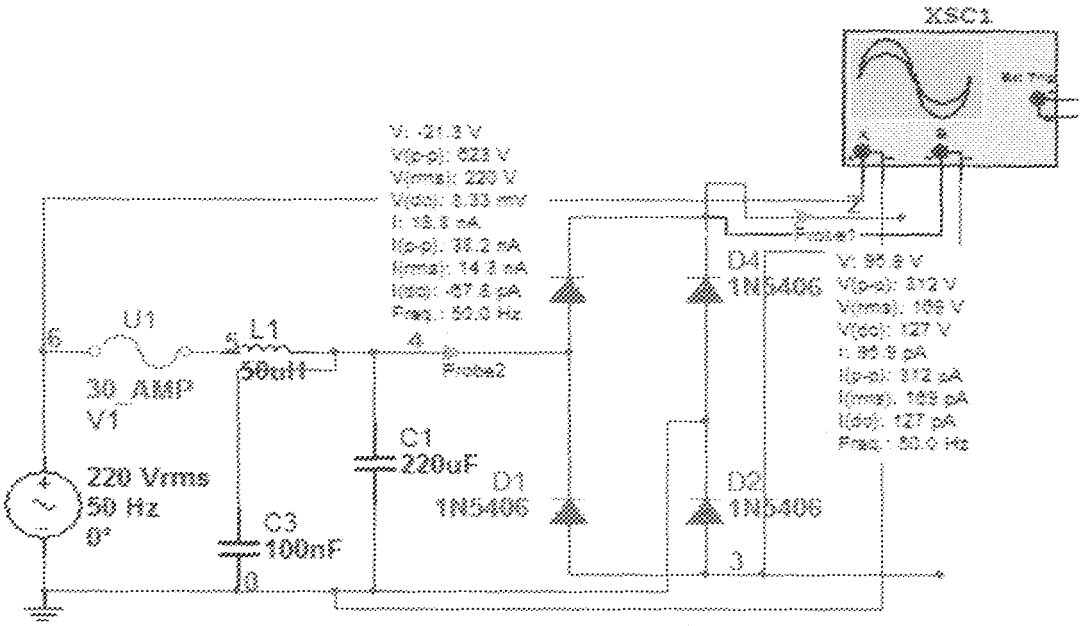

Figure 2.13a Unfiltered full wave rectifier Circuit

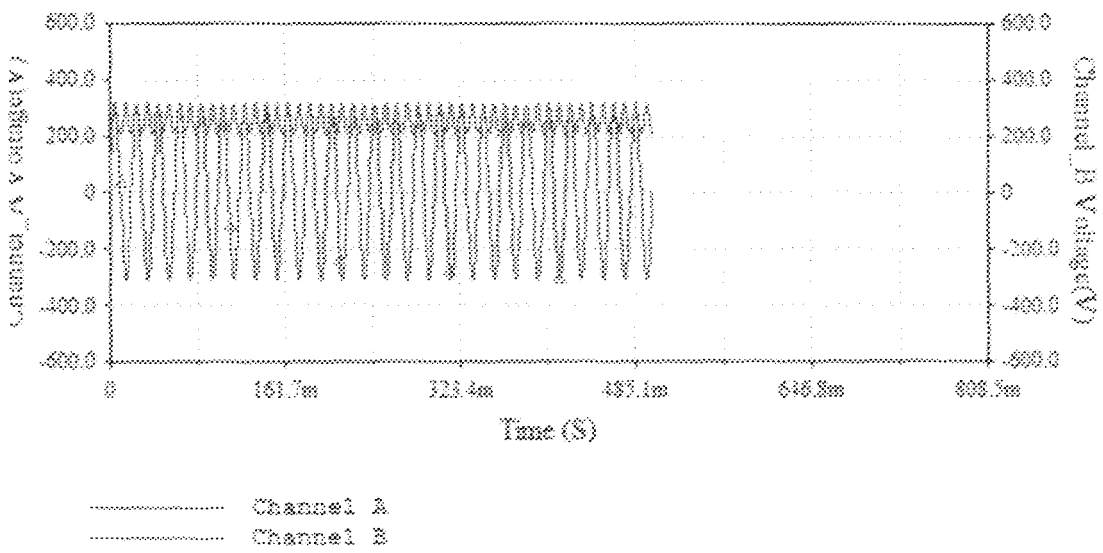

Figure 2.13b: Unfiltered full wave rectifier output waveform

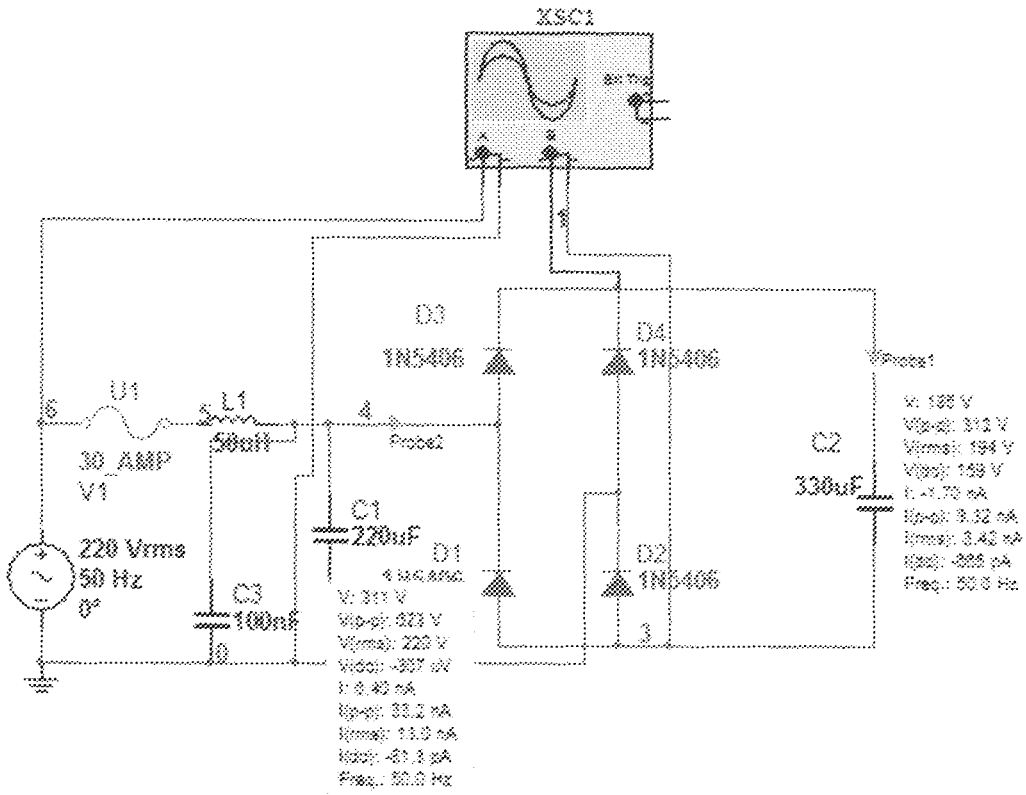

Figure 2.13c Filtered full wave rectifier

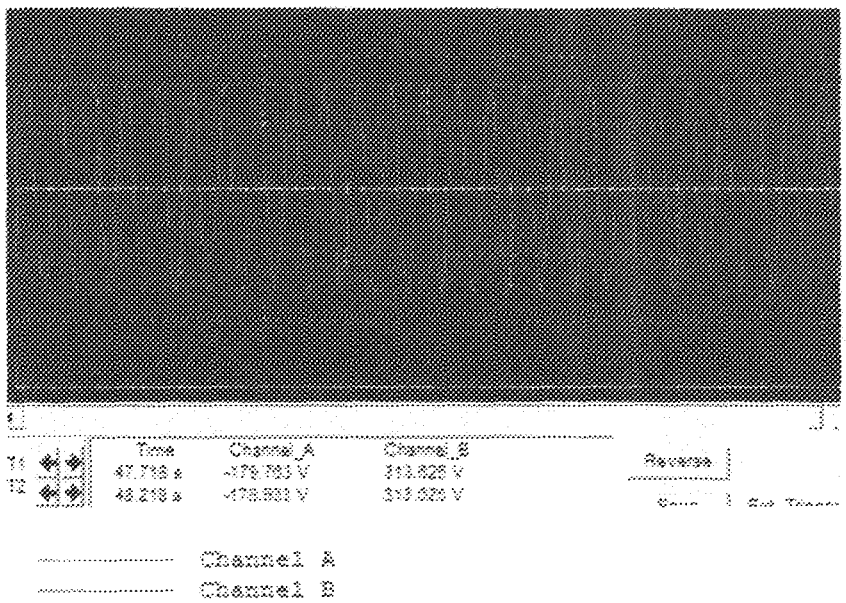

Figure 2.13d filtered full wave rectifier circuit waveform

2.5.3.1 Design Considerations:

i. Reverse voltage of the supply should not exceed the break down value of the diodes.

ii. Power dissipation should be limited to

$$P = V_d \times I_d \qquad (2.14)$$

Diode Voltages:

Forward bias: The diode has a thresh hold voltage of between 0.6Vand 0.8V beyond which the diode starts conduction of current. The current increases as the bias voltage increases beyond the thresh hold value of voltage. This results in a forward voltage drop of 0.6V to 0.7V across each forward biased diode. In the case of the full wave rectifier diode bridge, there are two forward biased diodes in series with the load in each half cycle of the input signal. This implies a maximum output voltage across load of:

$$V_o = V_{in} - 2V_{thresh\ hold} \qquad (2.15)$$

Or

$$V_o = V_{in} - 1.4\,V \qquad (2.16)$$

Reverse bias:

In specifying a diode for use in a circuit care must be taken to ensure that the limits for forward and reverse voltage and current are not exceeded. In reverse bias, the current through the diode is approximately the reverse saturation current, I_o. The voltage across the load during reverse is $V_{out} = I_o R_{load}$ (2.17)

The dc voltage produced by the circuit of Figure 2.13a is pulsating. To reduce these pulsations to a tolerable limit, a filter is applied in the output terminal of the basic rectifier. A commonly used filter is a capacitor. The full wave rectifier with a capacitor filter is shown in Figure 2.13b. The result of the addition of a capacitor is a smoothing

of the full wave rectifier output. The output is now a pulsating dc with a peak to peak variation called ripple. The magnitude of the ripple depends on the input voltage magnitude and frequency, the filter capacitance and the load resistance. Ripple is due to charging and discharging of the capacitor filter.

The voltage of a discharging capacitor is given by $V_{r(pp)} = V_{max} - V_{min}$

$$= V_{max}(1 - e^{-(t2-t1)/RC}) \qquad (2.18)$$

If C is large such that $RC >> t_2 - t_1$ the exponential in the above expression can be approximated as $1 - (t_2 - t_1)/RC$ and $V_{r(pp)}$ becomes $V_{max}(t_2 - t_1)/RC$. Since

$t_2 - t_1$ is approximately $\frac{T}{2}$, Where T is the period of the sine wave. $V_{r(pp)}$ becomes

$$V_{max}\frac{T}{2RC} = \frac{V_{MAX}}{2fRC} \qquad (2.19)$$

2.5.4 Power MOSFET Switch

Power MOSFETS are voltage controlled. Their gates appear as capacitances (of the order of pico- farads/nano-farads) and must be charged for on state and discharged for off state. This means the current need only flow during the short time it takes to charge/discharge the small gate capacitor.

This leads to very short switching times, making MOSFETS highly switchable for high frequency applications. Due to their construction, a MOSFETS's on resistance increases rapidly with the device's blocking rating. MOSFETS also have a positive temperature coefficient, (Balogh, 2001).

2.5.5 The High Frequency Transformer

The high frequency transformer in switch mode power supplies is used to isolate the primary from the secondary side. It is made up of cores of special ferrite materials, to meet specific requirements. Consequently there cannot be an off the shelf ferrite transformer that will perform as desired in all cases. They are therefore built to meet each specific application.

The transformer exhibits some losses in the ferrite cores especially at high frequencies. In order to reduce switching stresses and the accompanying losses the transformer is designed to operate at just under a 50% duty cycle on the switches. This allows for fluctuations in load and supply voltage to be dealt with by decreasing or increasing the switch duty ratio.

Ferrites have a higher electrical resistivity than their iron counter parts and hence exhibit no significant eddy current characteristics but mainly hysteresis losses, but then saturation flux densities are quite low. They are therefore the material of choice for high frequency applications. Care must however be taken to avoid saturation of the transformer, as this can result in damage to the transformer, switching transistors, control IC or other components in the circuit. Core saturation occurs when there are too few turns on a transformer or an inductor and causes the flux density to be too high. Put differently saturation is when the core's cross sectional area can no longer support additional lines of flux. This makes both the permeability of the core and inductance values to drop drastically. This makes the inductor to stop being an A.C current limiting device and it turns into a short circuit. Hence within microseconds a nice linear current

ramp can go from a few amps to tens or hundreds of amps thus causing the semi conductor switch to fail.

Parameters of the transformer serve as the backbone of the converter design. The first step is to select a core family that will house the transformer windings. This is done first by reviewing various core styles and their attributes. The most common off-line core is the EE core for which there are several variations.

Appropriate core size selection is based on the following:

i. The core must have a sufficient core cross sectional area A_C to contain the needed flux density to transport the power from the primary to the secondary windings.
ii. There must be enough winding area, W_a to contain the required number of turns of the needed wire gauges.

According to http//onsemi.com (AND8039/D) the product WaAc is provided by core manufacturers for each core size and is given by:

$$W_a A_c = \frac{0.7\left[P_{out} W_{d(pri)}\right]}{f B_{max}} \qquad (2.20)$$

where:

$W_d\ (_{pri})$ is the average wire diameter needed to carry the primary current in metres.

B_{max} is the maximum operating flux density in Wb/m². The core size selected should be equal to or greater than the calculated $W_a A_c$, and additional allowance in $W_a A_c$ made to accommodate insulation tape.

In switch mode forward converters, the operating flux density (B_{max}) dictates how much magnetization energy, which is not used that must be released by the core prior to the next power switch conduction cycle. This is a point of trade off, if B_{max} is set too low then there will be many turns on the transformer, thus making the transformer larger than it needs to be. Setting B_{max} too high makes the transformer smaller but increases the losses related to the core reset function. A good point of compromise is to set B_{sat} at about 25% of B_{max} at 100 kHz. This level should be reduced by a factor of 0.04 per 100khz above this frequency. One can then calculate the turns by:

$$N_{pri} = \frac{V_{in(max)}}{4 f B_{max} A_c} \qquad (2.21)$$

where: B_{max} is in Wb/m^2

Ac is the core cross sectional area in m^2.

In conventional forward converter the reset winding is identical in turns to the primary winding and usually about 3-4 wire gauges smaller than that of the primary winding as it carries the reset current for a short time only. It is phased oppositely from the primary so that it can discharge the magnetization energy when the power switch is off.

The secondary turns is found by realizing that the secondary voltage must provide an output wave form that will have a volt time average that will create the proper power output voltage when presented to the LC filter thus:

$$N_{sec} = \frac{1.1 N_{pri}\left(V_{out} + V_{fwd}\right)}{V_{in(min)} \times D_{max}} \qquad (2.22)$$

Where D_{Max} is the maximum duty cycle ratio of the system <0.5

V_{fwd} is the normal forward voltage drop of the rectifier. The 1.1 factor provides a 10% margin in the supply's low voltage drop out point and also provides margin for other variations in the circuit. The secondary output with the highest output power should be the main output which would then serve as the reference winding for all of the other secondary windings. When determining any additional secondary winding one must account for each of the forward voltage drops of their respective rectifiers. This can be done by:

$$N_{sec(n)} = \frac{N_{sec(1)}\left(V_{out(n)} + V_{fwd(n)}\right)}{V_{sec(1)}} \qquad (2.23)$$

The auxiliary winding which provides power to the control IC, need not be regulated or accurate. It needs only to exceed the low voltage inhibit limit of the controller IC which is 10.0V for UC3842 at the low input voltage.

A series resistor and a zener diode across the auxiliary winding voltage filter capacitor may be necessary to limit the maximum voltage, and therefore protect the gate of the power switch, (Walker).

2.5.6 Output Inductor

The inductor is used as an energy storage device in switching regulator applications. When the power switch is 'on' the current in the inductor ramps up and energy is saved. When the switch is off this energy is returned to the load and the amount of energy stored is given by:

$$E=1/2LI^2 J \qquad (2.24)$$

Where L – inductance in henry

I - peak value of inductor current

Inductors are used in forward converters for improved cross regulation .Each output of a forward converter requires an inductor and building on a common core greatly aids cross regulation and saves space.

Regulation and ripple current of inductors can be adjusted by the order of the windings on the core and by leakage inductance.

The inductor current is made up of the ripple current and dc load current. The ripple current being of high frequency will flow through the output capacitor as it has low impedance for high frequency currents. This will produce a ripple voltage in the capacitor due to the capacitors' equivalent series resistance that will appear at the output of the switching regulator. The ripple voltage has to be sufficiently low as not to affect the operation of the circuit the regulator is supplying.

Another effect of the ripple current is on the size of the inductor and output capacitor. High ripple current implies that the capacitor will be rated for a high ripple current, else it will over heat and dry up. A ripple current value of 10% to 30% of maximum inductor current is normally chosen.

2.5.7 Output Capacitor

Since the output capacitors current is equal to the inductor's ripple current, the output capacitor's value can be found using the inductor's ripple current. Starting with the current voltage relationship, the output capacitance is calculated.

2.5.8 Output Rectifier Snubbers

The purpose of the snubber circuit is to absorb energy from the leakage inductance in the circuit. The leakage inductance is part of the primary inductance that is not

mutually coupled with the secondary inductance. It is important to keep the leakage inductance as low as possible because it reduces the efficiency of the transformer and it causes spikes on the drain of the switching device.

The leakage inductance is normally taken as 2-5% of the inductance of the primary winding:

$$\text{Leakage} = 0.03L_p \text{ (assumed)} \tag{2.25}$$

$$\text{Total energy} = \frac{1}{2}LI^2 \tag{2.26}$$

$$E_{snubber} = \frac{1}{2}L_{leakage}I_{pk}^2 \tag{2.27}$$

There are different ways to dissipate this energy and reduce the spikes on the drain of the switching MOSFET. A typical snubber circuit is a resistance and a capacitor connected in series between the input voltage and the drain of the MOSFET (approximately half of the leakage inductance energy is dissipated on the snubber circuit).

The snubber capacitance can be calculated as follows:

$$C_{snubber} = \frac{E_{snubber}}{2f_{spike}VI_{max} + V^2 f_m} \tag{2.28}$$

Where:

The RC time has to be larger than the on-time switching period:

$VRC < T_{on}$

$$R_{snubber} = \frac{T_{on(min)}}{4C_{snubber}} \quad (2.29)$$

$$PR_{snubber} = Vi^2_{(max)} C_{snubber}. F_{sw} \quad (2.30)$$

For low output applications a clamp zener or a transient suppressor can be used.

2.5.9 Output Rectifiers

The reverse voltage rating of the rectifiers is determined using the maximum peak input voltage and transformer turns ratio using the formula, (Wakler, 2005):

$$V_R = \frac{V_{pk(max)} N_s}{N_p} \quad (2.31)$$

Rectifier current is the peak inductor ripple current (minimum load current) added to the maximum output current. To calculate the rectifier current we use:

$$I_{diode} = I_{out\,(Max)} + I_{ripple\,(peak)} \quad (2.32)$$

The design requires a diode that has a low forward voltage because diode losses are largely determined by the forward voltage and current.

$$P_{av} = I_{peak} + DV_f \quad (2.33)$$

Using the general formula for calculating diode losses we have:

$$P_{diode} = V_f I_{peak} \quad (2.34)$$

2.5.10 Start Up and Bias Circuit

The start up circuit shown in Figure 2.14 is made up of:

i. The starting resistor

ii. The bias winding that provides power to the controller IC as soon as its voltage is above the under voltage lock out thresh hold of the IC

iii. A capacitor that provides the hold-up power during the time the output inductor is discontinuous. Start up current should not be greater than 1mA, as the minimum trip voltage of the IC is 1V.

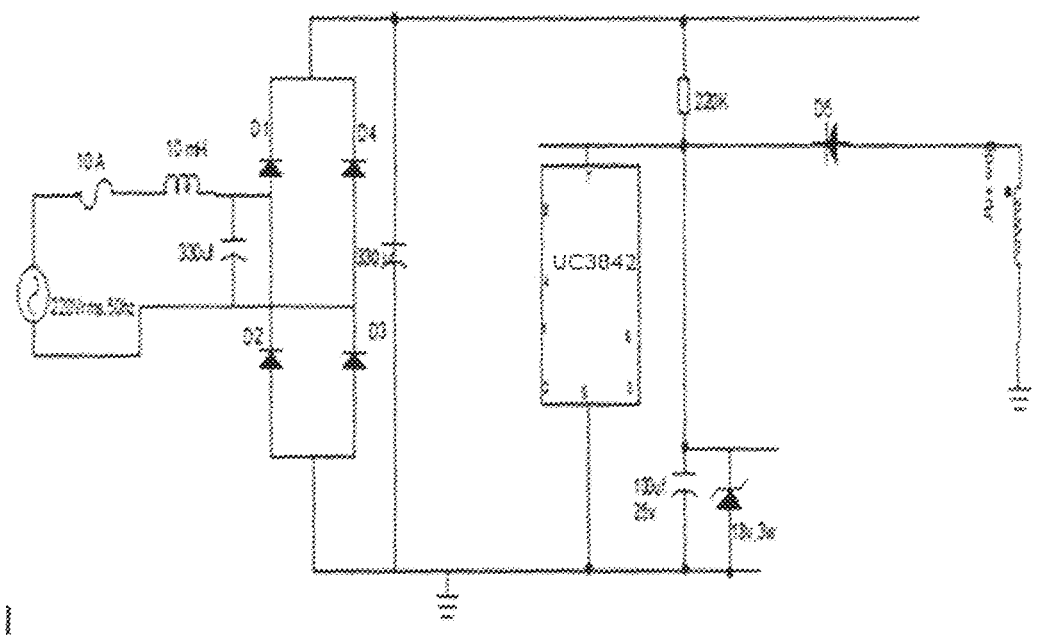

Figure 2.14 Starting and Bias Circuit

2.5.11 Drive Circuits For Power MOSFETS

During turn on and turn off switching, the gate voltage exhibits a step, remaining at a constant level while the drain voltage rises or falls during switching. This voltage at which the gate voltage remains during switching is known as Miller voltage V_{gm}. In

most applications, this voltage is around 4 to 6V, depending on the level of current switched. 15V is required to turn on the device, through switch.

The MOSFETS have current rise and voltage fall. Turn off losses can be reduced by reducing the size of the gate drive resistor Rg, as it allows the gate to charge more quickly. The turn off losses are proportional to the size of the gate resistor, e.g. from 10 to 100 according to (Balogh, 2001).

2.5.11.1 PWM Direct Drive

In power supply applications, the simplest way of driving the gate of the main switching transistor is to utilize the gate drive output of the PWM controller, as shown in Figure 2.15 below (Balogh, 2001):

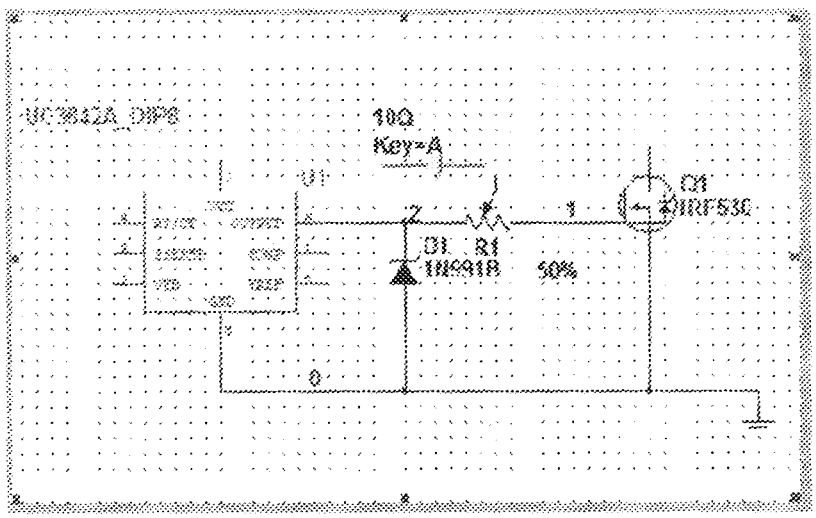

Figure 2.15 Direct MOSFETS Drive

The circuit above is used when the control IC is not electrically isolated from the MOSFET turn on and turn off and the drive current is 1A maximum. It also provides

damping for a parasitic tank circuit formed by the MOSFET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn off.

Disadvantages: - The most difficult task in direct gate drive is to optimize the circuit layout. There might be considerable distance between the PWM controller and the MOSFET. The distance introduces a parasitic inductance due to the loop formed by the gate drive and ground return traces which can slow down the switching speed and can cause ringing in the gate drive waveform.

(a) Another problem in direct gate drive is the limited drive current capability of the PWM controllers. Very few ICs offer more than 1A peak gate drive capability.

(b) Another limiting factor for MOSFET die size with direct gate drive is the power dissipation of the driver within the controller.

(c) When direct gate drive is absolutely necessary for space and or cost savings, special considerations are required to provide appropriate by passing for the controller. The high current spikes driving the gate of the MOSFET can disrupt the sensitive analogue circuitry inside the PWM controller, according to (Balogh, 2001).

2.5.11.2 Bipolar Totem Pole Driver

Another popular and cost effective drive circuit for driving MOSFET is a bipolar, non inverting totem pole driver whose circuit is shown below

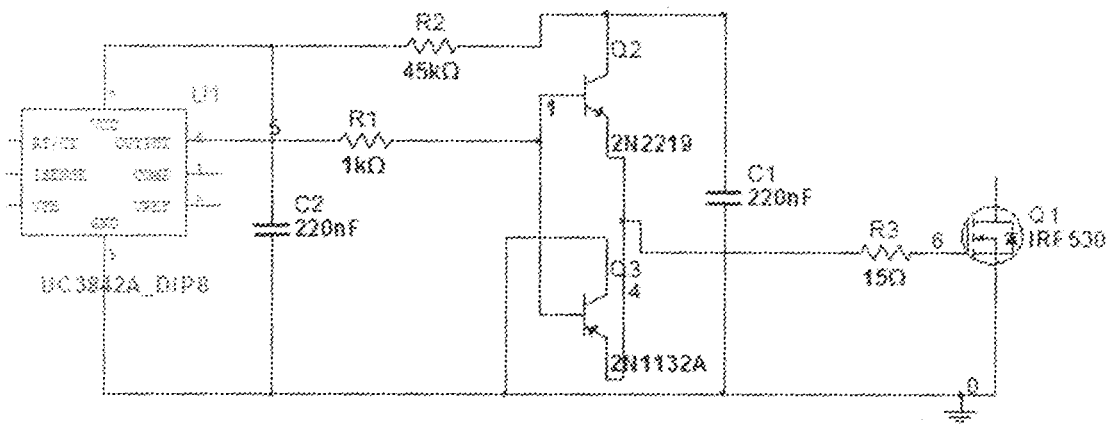

Figure 2.16 Totem Pole Driver Circuit

Like all external drivers, this circuit handles the current spikes and power losses making the operating conditions for the PWM controller more favourable. They can and should be placed right next to the power MOSFET they are driving. That way the high current transients of driving the gates are localized in a very small loop area, reducing the value of parasitic inductances.

2.5.11.3 Transformer Coupled Gate Drive

The transformer coupled gate drive is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. The properly designed transformer coupled gate driver can operate across higher Potential difference. Usually it takes more components and requires the design of a transformer. The gate drive transformer handles very low average power but it delivers high peak currents at turn-on and turn-off. To avoid time delays in the gate drive path, low leakage inductance is imperative.

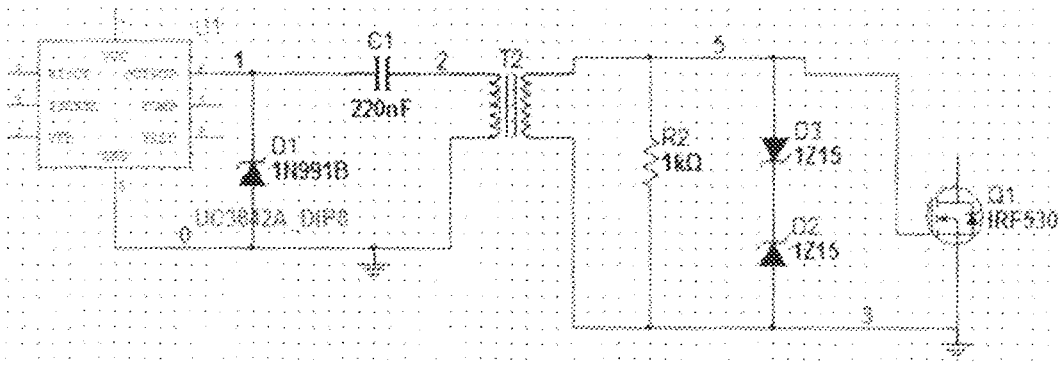

Figure 2.17 Transformer Coupled Gate Drive

2.5.12 IC CONTROLLERS UC3842

There are many commercially available IC chips/ controllers for achieving the pulse width modulation that avoids the use of stand-alone MOSFET drivers.

UC3842 is an example of such a device and has been chosen in this project due to its easy availability and low cost.

According to Unitrode application note U-100A, UC3842 control IC provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with minimal external parts count and has the following internally implemented circuits:

i. Under voltage lock out featuring start up current less than 1mA.

ii. A precision reference trimmed for accuracy at the error amplifier input.

iii. Logic to ensure latched operation.

iv. A PWM comparator which also provides current limit control.

v. A totem pole output stage designed to source or sink high peak current.

vi. UVLO start voltage is 16V with a maximum duty cycle of less than 100% and a UVLO turn off thresh hold of 10V

vii. Application includes forward and buck/boost converter circuits.

2.5.12.1 Under Voltage Lock Out

The UVLO circuit ensures that Vcc is adequate to make the UC3842 fully operational before enabling the output stage. The 6V hysteresis prevents Vcc oscillations during power sequencing. Start up current is less than 1mA for efficient bootstrapping from the rectified input of an off-line converter. During normal circuit operation, Vcc is developed from auxiliary winding W_{aux} with D1 and C_{in} .At start up however C_{in} must be charged to 16Vthrough R_{in}. With a start up current of 1mA R_{in} can be as large as 100kΩ and still charge C_{in} (Figure 2.12 above refers).

2.5.12.2 Oscillator

The UC3842 is programmed as shown in Figure 2.16 below: Timing capacitor C_T is charged from V_{ref} (5V) through the timing resistor R_T and discharged by an internal current source. The required circuit dead time is determined first and thereafter the value of C for the dead time is determined. Next the value of R_T is calculated by substituting the values of C_T and f into the formula:

$$f(KHz) = \frac{1.72}{R_t(k) \times C_t(uf)} \qquad (2.35)$$

The UC3842 runs at the switching frequency and can be used to a maximum frequency of 500 kHz.

For optimum IC performance the dead time should not exceed 15% of the oscillator clock period. During the discharge or dead time, the internal clock signal blanks the output to the low state. This limits maximum duty cycle D_{max} to:

D_{max} = 1-(t dead /t period), where t period $= \frac{1}{f}$ (2.36)

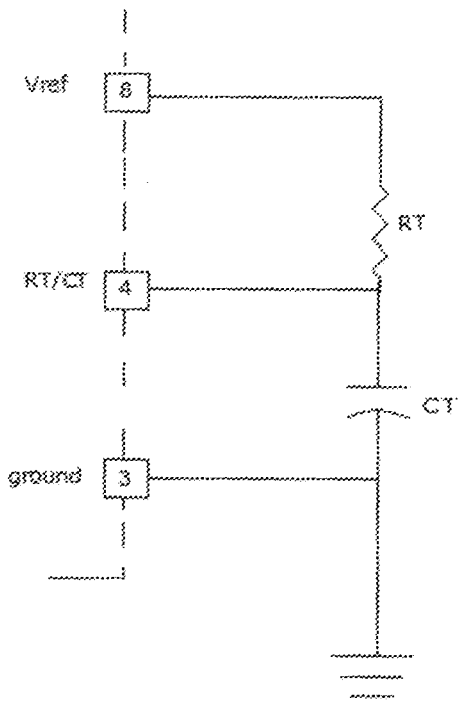

Figure 2.18 Timing Circuit

2.5.12.3 Current Sensing and Limiting:

The UC3842 current sense is configured as shown in Figure 2.17a below.

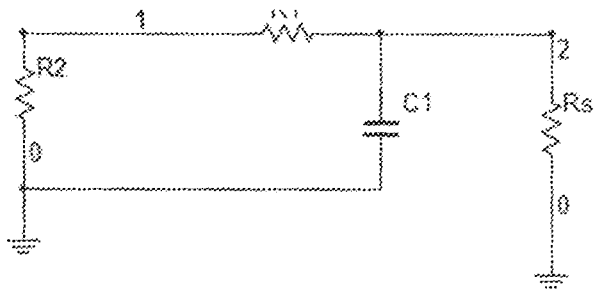

Figure 2.19 Direct current sensing

Current to voltage conversion is done externally with ground referenced resistors. Under normal operation the peak voltage across Rs is controlled by the E/A according to the following relation:

$$I_p = \frac{V_c - 1.4}{3R_s} \tag{2.37}$$

Where V_c =control voltage =error amplifier output voltage.

Rs can be connected to the power circuit directly or through a power transformer. While a direct connection is simpler, a transformer can reduce power dissipation in Rs, reduce errors caused by the base current and provide level shifting to eliminate the restraint of ground referenced sensing. The relation between Vc and peak current in the power stage is given by:

$$I_{pk} = N\frac{VR_{s(pk)}}{R_s} \quad = \frac{N}{3R_s \times (V_c - 1.4)} \tag{2.38}$$

Where N=current sense transformer turns ratio =1, when transformer is not used.

When sensing current in series with the power switch, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and /or inters winding capacitance in the power transformer. If un-attenuated, this transient can prematurely terminate the output pulse. A simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to theUC3842 current sense comparator is internally clamped to 1V.Current limiting occurs if the voltage at pin 3 reaches this threshold value i.e. the current limiting is defined by $\frac{N \times 1V}{R_s}$ (2.39)

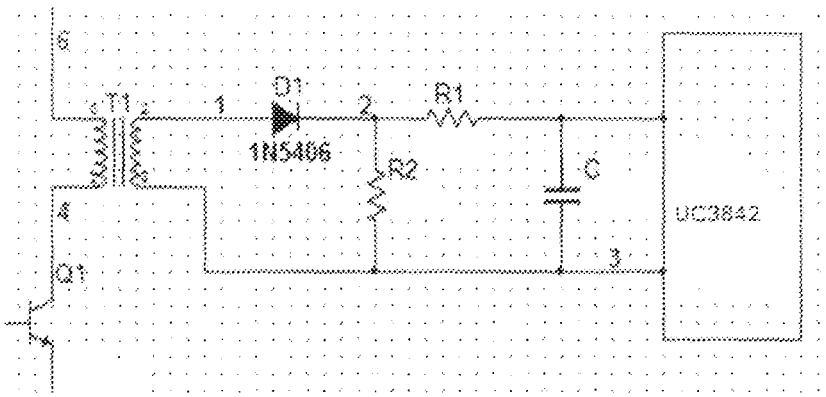

Figure 2.20 Transformer coupled current sensing.

2.5.12.4 Error Amplifier (E/A)

The non inverting input is not brought out to a pin, but is internally biased to 2.5V +/- 2%.The E/A output is available at pin 1 for external compensation allowing the user to control the converter's closed loop frequency response. The E/A output will source 0.5mA and sink 2mA.A lower limit for feedback resistor R_f is given by:

$$R_{f(min)} = \frac{V_{E/A out(max)} - 2.5}{0.5mA} = \frac{6 - 2.5}{0.5mA} = 7k\Omega.$$

2.5.12.5 Totem Pole Output

The UC3842 has a single totem pole output which can be operated to +1 amp peak for driving MOSFET gates and a 200mA average current for bipolar power transistors. Limiting current through the IC is accomplished by placing a resistor between the totem pole output and the gate of the MOSFET the value is determined by dividing the totem pole collector voltage Vc by the peak current rating of the IC's totem pole. Without this resistor the peak current is limited only by the dv/dt rate of the totem pole switching and

the MOSFET gate capacitance. A schottky diode is connected between the output of the PWM and ground to prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective the diode selected should have a forward drop of less than 0.3V at 200mA Placing the diode as physically close to the PWM as possible will enhance circuit performance.

2.5.12.6 Noise

Noise on the current sense or control signals can cause significant pulse width jitter, particularly with continuous inductor current designs. Ceramic monolithic by pass capacitors (0.1μf) from V_{cc} and V_{ref} to ground will provide low impedance paths for high frequency transients at the ground points. In order to minimize noise spike choose C_t (timing capacitor) as large as possible remembering that dead time increases with C_t. It is recommended that C_t never be less than 1000pNoise could result when the output pin 6 is pulled down below ground at turn off by external parasites, especially when driving MOSFET. A schottky diode clamp from ground to pin 6 will prevent such output noise from feeding back to the oscillator.

CHAPTER THREE

MATERIALS AND METHODS

3.0 Introduction

This chapter describes the design of a forward converter using the theories of the preceding chapter. The forward converter is composed of various sub circuits which interact with one another to ensure optimal and stable performance. Sub circuits of the converter were first designed and tested individually prior to interconnection with each other. The schematic diagram of the converter is shown in Figure 3.1 below:

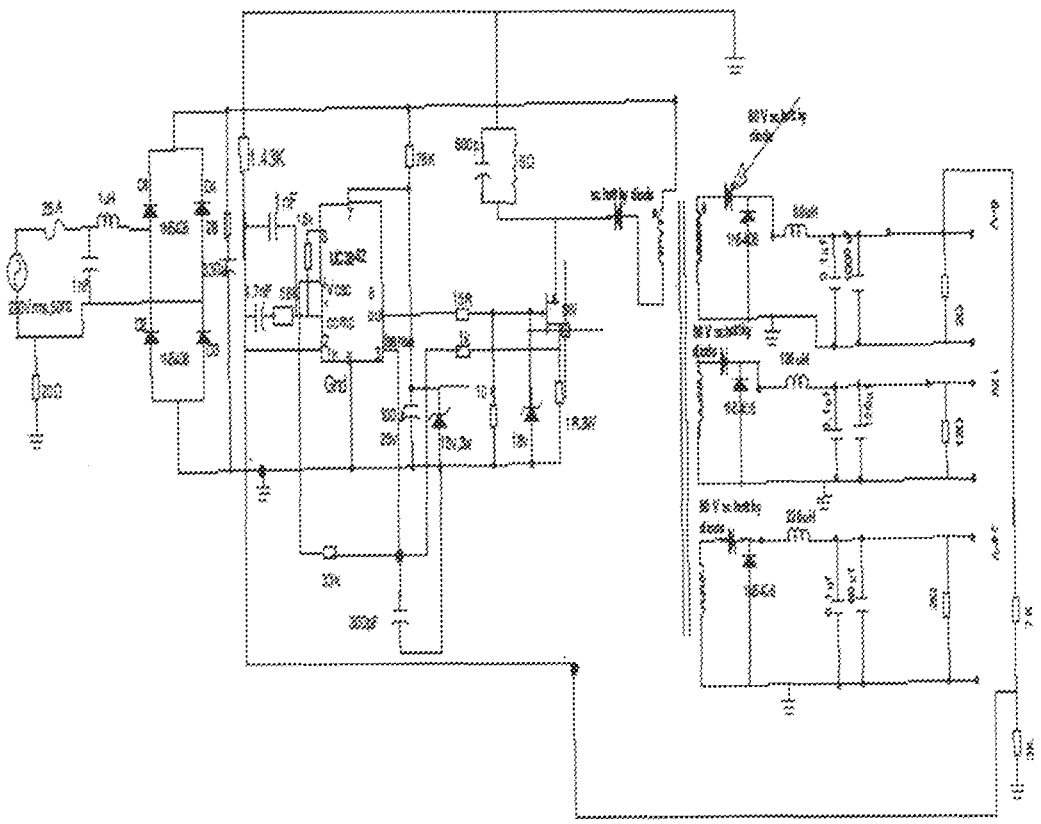

Figure 3.1 Circuit of a forward converter for construction

3.1 Specifications for the Forward Converter

Design of a converter commences with statement of the parameters of the converter .The following specifications apply to the designed forward converter:

Input rectifier configuration- full wave

Inrush limiting to be provided by a negative temperature coefficient thermistor – NTC

Converter topology -Single switch forward

Efficiency - 80%

Ripple voltage - 10 % of peak to peak of output voltage, V_{pp}

Frequency = 100 KHz.

A.C input voltage:

$V_{in\ a.c(low)}$ 220-10% V =198 V_{rms}

$V_{in\ a.c(hi)}$ 220+10% V =242 V_{rms}

Peak D.C. input Voltages:

$V_{in\ (low)}$ =1.414 x $V_{in\ a.c\ (low)}$ =1.414 x198 =280V

$V_{in\ (hi)}$ =1.414 x $V_{in\ a.c\ (hi)}$ = 1.414 x242 =342V

Output DC Voltages and currents: (6V/15A),(12V/5A), (24V/3A)

Total output power p_o = (6x15A +12x5A+24x3A) =222W

Maximum average input current $I_{in\ av}$ = p_o/efficiency x$V_{in\ (min)}$

=222/.8 x280 =0.99A

Nominal peak current, I_{pk} =2.8x p_o /$V_{in\ min}$ =2.8 x 222/242 =2.6A

3.2 Input Rectifier /Filter Circuit

The specifications for the rectifier are as follows:

Input ac power supply -220V +/- 10% rms

Diode type - IN5406; with the following data:

Average rectified forward current, $I_{F(AV)}$ = 3A at 75°C,

Maximum repetitive reverse voltage, V_{RRM} = 600V

Non repetitive peak forward surge current I_{FSM} = 200A

Power dissipation P_D = 6.25W

Forward voltage drop at 3A = 1.2V

The input rectifier circuit incorporates such features as :

Input switch/fuse rated at 25A

EMI filter

Inrush limiting negative temperature thermistor

Line cord

The complete rectifier circuit with the resulting simulation results is shown in Figure 4.1 below. The simulation result shows the following data:

i) Average DC current, I_{dc}=23.1A

ii) Peak DC voltage, $V_{dc(p-p)}$=313.7-V

iii) Peak current, $I_{(p-p)}$=13.4A

iv) I_{rms}=15.2A

v) V_{rms}=185-V

vi) I_{p-p}=43.1A

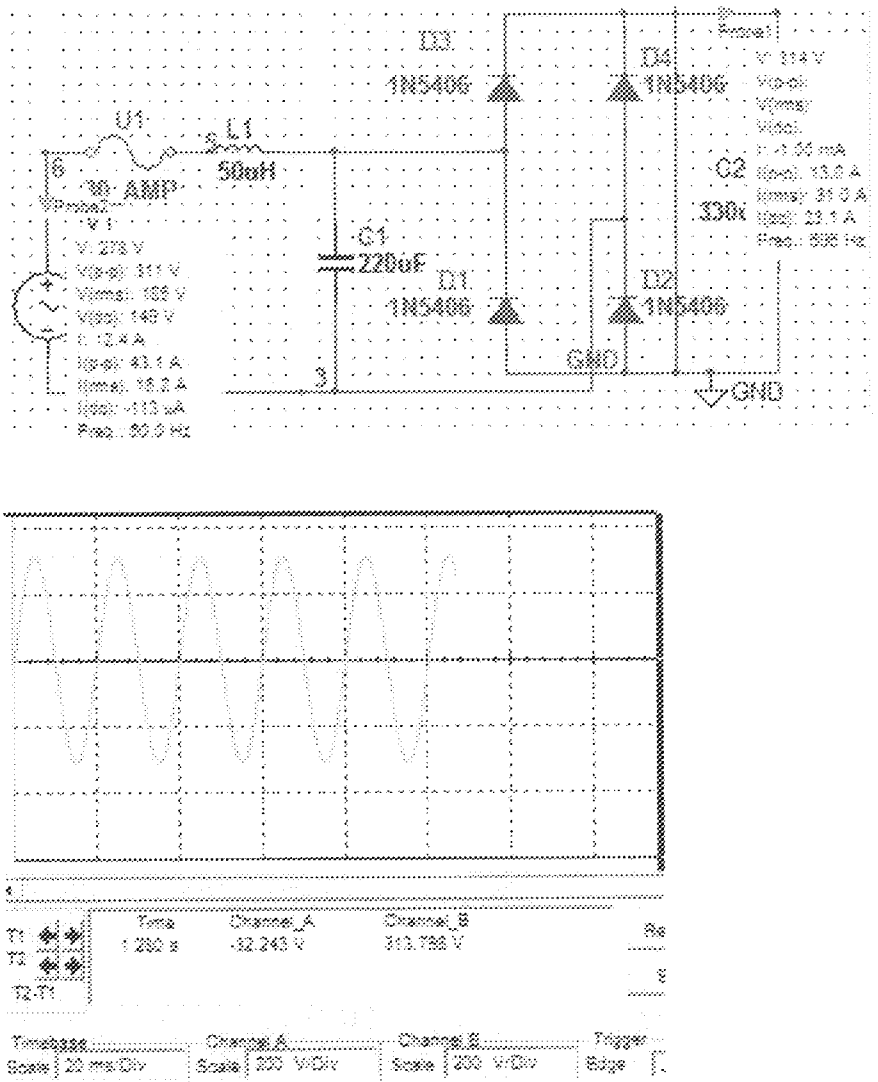

Figure 3.2: Full wave rectifier circuit and output voltage waveform

3.3 Bulk Capacitor

The key concern here is the DC voltage decay during the time the input rectifier is not conducting. The capacitor reduces the ripple voltage in the input to the dc converter in addition to providing a hold-up time during which the regulated supply keeps providing the regulated voltage output in the absence of the AC input voltage caused by a momentary power outage and can be calculated according to (Mohan *et al* 2003) by:

$$C_2 = \frac{2 \times ratedpoweroutput \times holduptime}{V^2_{d(min)} - V^2_{d(min)} \times \eta} \qquad (3.1)$$

where $V_{d\,(min)}$ is chosen to be in the range of (60-75)% of the nominal input voltage V_d and η is energy efficiency of the power supply, according to (Mohan, *et al* 2003) .

Putting the values we have $Co = \frac{2 \times 222 \times 0.02}{342^2 - 239.4^2} = 297.7\mu F$

Value selected is 400μF

3.4 The High Frequency Transformer

Construction of the transformer starts with core selection. Cores have different dimensions specified in terms of: A, B, C, D, E, and G values and power ratings. In this project EE core was locally sourced and the size was found to match core ER35 from core selection charts parameters of this core was found to be as follows:

Power rating - 443W, at 100 kHz

Ac value =0.0001m^2

Flux density =0.1wb/m^2

The measured dimensions of the core were found to be as stated below:

1. A =43mm
2. B =16mm
3. C=10 mm
4. øD =16mm
5. E = 16mm
6. G=2.080mm

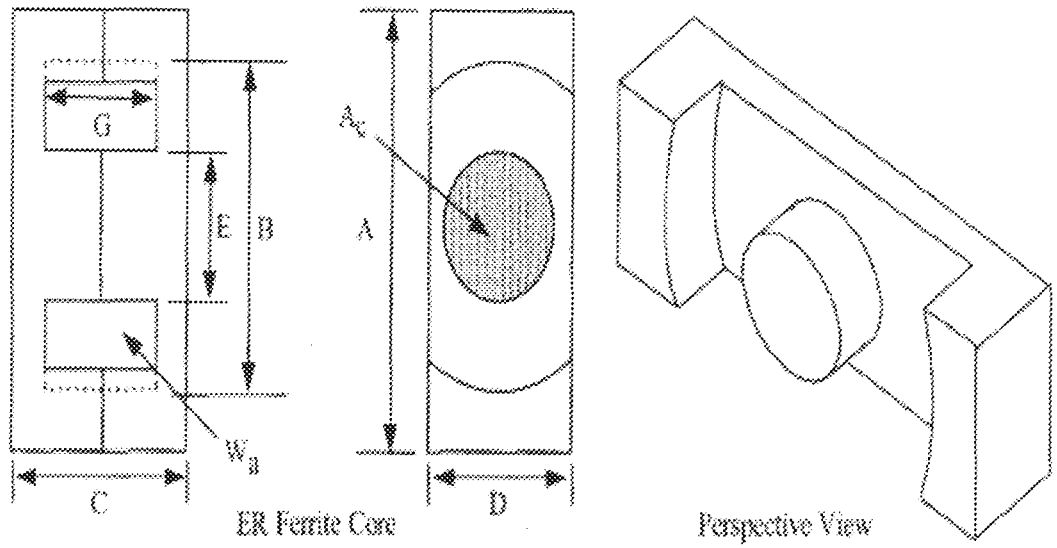

Figure 3.3 ER-Core Dimensions (Melyman,2004)

Table 3.1: Dimensional data for ER ferrite cores (Melyman , 2004)

ER. Ferrite Cores (Ferroxcube)													
Part No.	A (cm)	B (cm)	C (cm)	D (cm)	E (cm)	G (cm)	Part No.	A (cm)	B (cm)	C (cm)	D (cm)	E (cm)	G (cm)
ER 9.5	0.95	0.75	0.49	0.5	0.35	0.32	ER 42	4.2	3.005	4.48	1.56	1.55	3.09
ER 11	1.1	0.87	0.49	0.6	0.425	0.3	ER 48	4.8	3.8	4.22	2.1	1.8	2.94
ER 35	3.5	2.615	4.14	1.14	1.13	2.95	ER 54	5.35	4.065	3.66	1.795	1.79	2.22

Table 3.2: Design data for ER ferrite cores (Mclyman, 2004)

ER. Ferrite Cores (Ferroxcube)											
Part No.	W_{cu}	W_{fe}	MLT	MPL	W_a	A_c	W_c	A_p	K_g	A_t	AL
	grams	Grams	Cm	cm	A_g	cm^2	cm^2	cm^4	cm^5	cm^2	mh/1K
ER 9.5	0.6	0.7	2.7	1.42	0.842	0.076	0.064	0.00486	5.4E-05	3	435
ER 11	0.7	1	3.2	1.47	0.65	0.103	0.067	0.00688	0.00009	3.7	609
ER 35	56.7	46	7.3	9.08	2.19	1	2.19	2.19037	0.12034	62.4	1217
ER 42	72.9	96	9.1	9.88	1.189	1.89	2.248	4.24867	0.35244	81	2000
ER 48	120.7	128	11.5	10	1.185	2.48	2.94	7.2912	0.62625	100.1	2478
ER 54	101.9	122	11.4	9.18	1.052	2.4	2.525	6.0606	0.51254	96.2	2652

*This AL value has been normalized for a permeability of IK. For a close approximation of AL for other values of permeability, multiply this AL value by the new permeability in kilo-perm. If

The new permeability is 2500. Then use 2.5.

3.5 Calculation of Primary and Secondary Turns

The construction requires a minimum number of turns on the high current 6V winding and good cross regulation to the 12 V winding since these have the tightest tolerances. Output rectifiers selected are schottky diodes with 0.6 V forward voltage drops, which imply a transformer output requirement of 6.6v and 12.9v for the 6v and 12v terminals respectively. Calculation of the turns can be carried out using formulae or using iteration process. The method chosen involves the use of formula as shown below:

Primary turns are calculated using the formula

$$N_{pri} = V_{in}(nom)\frac{1}{4fB_{max} \times A_c} \qquad (3.2)$$

$$= \frac{342}{4\times10^5 \times 0.1 \times 0.0001} = 85.5 = 86 \text{ turns}$$

Calculating for the 6V secondary turns which being the highest current terminal serves as the reference to other secondary outputs we have

$$\text{Secondary turns, } N_s = 1.1 \times \frac{V_{out} + V_{fwd}}{V_{in(min)} \times D_{max}} \qquad (3.3)$$

$$= \frac{1.1 \times 86 \times 6.6}{280 \times 0.45} = 4.5 = 5$$

When determining any additional secondary winding one must account for each of the forward voltage drops of their respective rectifiers that is:

$$N_{sec(n)} = N_{sec(1)} \left[\left(V_{out(n)} + V_{fwd(n)} \right) \times \left(\frac{1}{V_{sec(1)} + V_{fwd(1)}} \right) \right] \qquad (3.4)$$

For 12V output we have:

$$N_{12} = \frac{5(12 + 0.9)}{6 + 0.6} = 9.8 \approx 10 \text{ turns}$$

$$N_{24} = 5\left(\frac{24 + 0.9}{6 + 0.6} \right) = 18.7 \approx 19 \text{ turns}$$

The auxiliary winding turns $N_{18} = 5\left(\frac{18 + 0.6}{6 + 0.6} \right) = 14$ turns

Final transformer parameters are:

1. Primary inductance = 957μH
2. Primary turns =86T,
3. 6V =5-T
4. 12V =14T
5. 24V= 2no 19-T
6. Auxiliary winding 14-T
7. Ferrite core ER-35.

3.5.1 Winding of Coils:

The primary and reset windings were wound first onto the bobbin. Next the auxiliary winding was wound on top of these windings. Three layers of Mylar tape were applied to provide some degree of dielectric isolation, then the secondary winding was applied last .A last layer of tape was added to provide some protection to the outer winding.

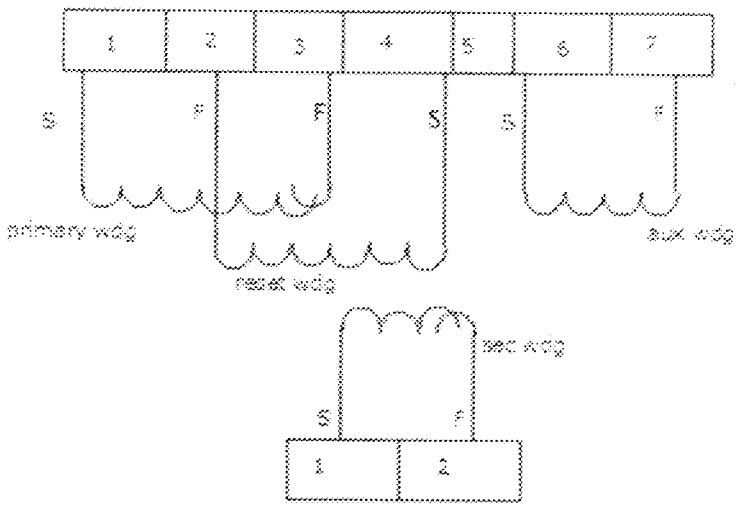

Figure 3.4: Terminal connection of the transformer windings

3.6 MOSFET switch

Minimum drain –source rating $V_{DSS(min)} = (V_{in(max)} + V_{clamp})$. For $V_{in(max)}$ = 342V $V_{DSS(min)}$ = 342 +376.2 = 718.2V. Minimum drain current rating of the selected switch is recommended to be greater than the maximum peak current. A reasonable value of $R_{DS(ON(max))}$ is recommended, also recommended is provision of heat sink for effective heat dissipation from the switch. MOSFET type selected is 11N80C3 with the following data: $V_{DSS(min)}$ =800V,I_D =11A , $R_{DS(ON)}$ =0.45Ω .

3.7 Output Components' Calculations

3.7.1 Output Inductor: The output inductance value is calculated thus:

Output filter inductance Lo, is given by:

$$\text{Lo} = 1.1\left[\left(\frac{V_{in(min)}N_s}{N_{pri}}\right) - V_{out}\right] \times \frac{T_{off(min)}}{1.4 \times I_{out(min)}} \qquad (3.5)$$

$$Dutycycld(\min) = \frac{V_{out} \times N_p}{V_{in(max),} \times N_s} \qquad (3.6)$$

At 100kz, for 6V output this becomes

$$= \frac{6 \times 86}{342 \times 5} = 0.3$$

At 100kz, T =10μs so that T_{on} =3μs and T_{off} =7μs

$$T_{off(min)} = \left(1 - D(\min) \times \frac{1}{f_{sw}}\right) = 1\text{-}0.3 \times 10 = 7\mu s$$

$V_{in(min)}$=280V

So that for 6V output, $L_6 = \left[1.1 \times 280 \times \frac{5}{86} - 6\right] \times 7. \times 10^{-6} \times \frac{1}{1.4 \times 2}$

$$= 45\mu H$$

For 12V output, $L_{12} = \left(\frac{308 \times 0.1162 - 12}{1.4}\right) \times 7 \times 10^{-6} = 118\mu H$

For 24V output, $L_{24} = \left(\frac{308 \times 0.22 - 24}{1.4}\right) \times 7 \times 10^{-6} = 218\mu H$

3.7.2 Output Rectifiers

The rectifier current is the peak inductor ripple current (minimum load current) added to the maximum load current that is:

$$I_{diode} = I_{out(max)} + I_{ripple(peak)} \quad (3.7)$$

For 6V/15A output, I =15+1.5 =16.5A

For 12V/5A „ I =5+0.5 =5.5A

For 24V/3A „ I =3+0.3 =3.3A

The reverse voltage rating for the rectifiers is determined using the maximum input voltage and transformation ratio, that is: $V_r = V_{in(max)} \times \left(\frac{N_s}{N_{pri}} \right)$ (3.8)

For the 6V output we have: $\frac{342 \times 5}{86}$ = 19.9V selected value is 25V

„ 12V „ „ „ : $\frac{342 \times 10}{86}$ =39.8V selected value is 40V

„ 24V „ „ „ : $\frac{342 \times 19}{86}$ =75.6-V, selected value is 80V

The output rectifier will be a surface mounted D2PAK schottky diodes .This efficiently couples the heat to the copper pad on the Vero board.

3.7.3 Start up Components

When the auxiliary power supply from the transformer is less than 10 -V, the start-up circuit is operational. When the auxiliary supply exceeds 10-V it cuts off its collector current, which is about 1mA. A 10μF or greater capacitor is normally placed on the auxiliary bus to store enough energy to actually start the supply, since the IC will draw about 10mA in the operate mode. A passive start up circuit is used to limit the input current to the control IC such that the current flowing in the start up circuit must be less

than current needed to run the control IC. The UC3842 use about 10mA during normal operation and draws between 0.3 and 0.5mA in standby mode. Therefore:

$$R_{start} = R_{st} = \frac{V_{min}}{I_{st(max)}} \quad (3.9)$$

$= 280/1mA = 280k.$

3.7.4 Primary Current Sensing Circuit Components

To keep the current mode operation linear and to reduce losses associated with current sensing the peak sense voltage must be kept less than 1V in normal operation.UC3842 used in this project has a maximum trip voltage of 1.0 V. Trip voltage chosen is therefore 0.6 V, giving a current sense resistor

$$Rs = \frac{V_{trip}}{I_{peak(max)}} \quad (3.10)$$

$=1/2.6 = 0.38\Omega.$

Power dissipated in the resistor, $P_d = \frac{V^2_{st(max)}}{R_{st}}$ (3.11)

$=342^2/280 = 0.42\text{-W}$

3.7.5 Current Ramp Time Delay Circuit Components

This circuit is very important to the over- all operation of the circuit. It provides the following:

i. Spike elimination to the current comparator

ii. Time delay function from the current sense resistor to the input to the current comparator. Although a wide range of resistor and capacitor values will work, some minimum time delay is required to avoid instabilities due to too short ON TIME at the

high range of input voltages. One starts by selecting the capacitor value which is in the range 470pf to 1000pf. Value selected is 1000pf and time delay chosen is 0.7μs because this is the approximate minimum OFF TIME at the high input voltage. The value of the resistor becomes. R_t =700nS/1000pf=700Ω.Standard value chosen is 680Ω.

3.7.6 Maximum Duty Cycle

The UC3842 has a maximum duty cycle of approximately 100%.However for optimum IC controller performance the dead time should not exceed 15% of the oscillator clock frequency. During the discharge or dead time the internal clock signal blanks the output to a low state, and this limits the maximum duty cycle to:

$$D_{max}=1-\frac{t_{dead}}{t_{period}} \qquad (3.12)$$

with a switching frequency of 100 KHz.

Dead time =15% of 1/100 KHz =1.5μs

D_{max} =1-1.5/10 = 0.85

Using the graph of dead time versus timing capacitor shown in Figure3.4a below, we estimate the value of the timing capacitor and finally use the graph of timing resistance versus frequency in Figure 3.5.6b below to estimate the value of the timing resistor. From the graphs, C_t= 4.7nF and R_t =7KΩ.

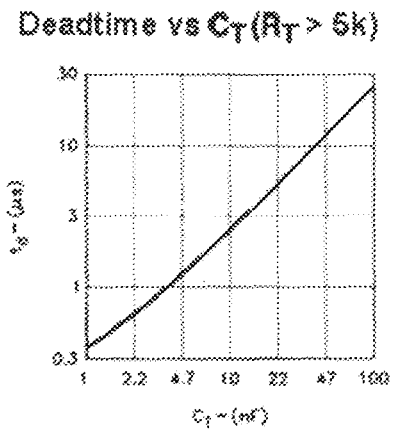

Figure 3.5a Dead time Vs C_T - (Unitrode application note U- 100A, 2004)

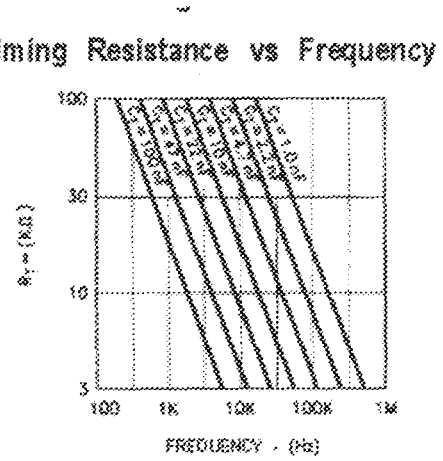

Figure 3.5b Timing resistance Vs frequency (Unitrode application note U-100A, 2004)

3.7.7 Voltage Feed –Back Circuit

According to Unitrode application note U-100A (2004), the lower resistor of the voltage sensing net work is set by assuming a sense current of 1mA so that the lower resistor,

$$R_{lower} = \frac{V_{ref}}{I_{sense}} \qquad (3.13)$$

$$= \frac{5}{0.001} = 5k\Omega$$

Splitting the output sensing among the outputs will improve the cross regulation of all the outputs. The output with the lower voltage, 6-V is connected to the feed-back loop

which is voltage sensitive. The loads on the higher output voltage are less susceptible to voltage variations. Therefore proportion of sense current selected is 70% for the 6V output and 30% for the 12V output. Therefore value of 6V sense resistor is:

$$R_6 = \frac{6-5}{0.7 \times 1mA} = 1.43K$$

$$R_{12} = \frac{12-5}{0.3 \times 1mA} = 23.3K$$

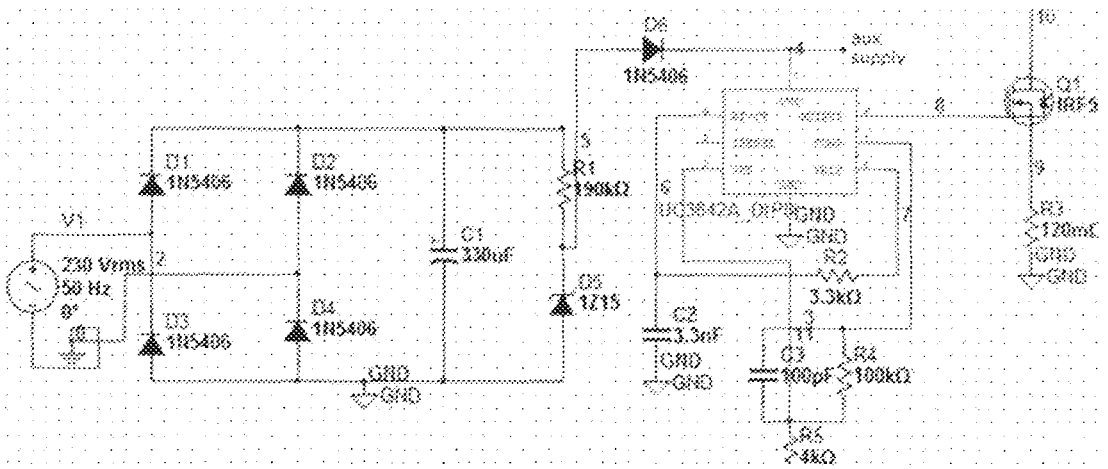

Figure 3.6: Rectifier, start up and bias circuit.

3.7.8 Output Capacitors

The aim of the output capacitor is to absorb the A.C current ripple in order to prevent it flowing through the load. Thus the current that flows through the output load is only a DC current. The calculations for the values of the output filter capacitors will be done at the lowest frequency since the ripple voltage will be greatest at this frequency. More-so capacitor values are determined by output current and are calculated by the relationship:

$$Co = \frac{I_{o(max)} \times V_{ripple}}{f_{co(min)}} \qquad (3.15)$$

Where f_{co} is the expected lowest frequency of operation determined by Shannon's theorem that cut of frequency, $f_c = f/10 \leq f/2$, so $f_c = 100/5 = 20kHz$

For 6V/15A output, Co =15/20 kHz x0.6 =1250μf

With I_{min}=3A and ripple voltage of 10%, the equivalent series resistance of the 6V output capacitor becomes, ESR6 = $\frac{\%ripple}{I(\min)} \times V_{out}$ (3.16)

$$= \frac{0.1 \times 6}{3} = 200m\Omega$$

For (12V/5A) and 1A minimum current, output $C_o = \frac{5}{10 \times 1.2} = 417\mu f$

$$ESR_{12} = \frac{0.01 \times 12}{1} = 120m\Omega$$

For (24V/3A) and 1A minimum current, output $C_o = \frac{3}{2.4 \times 10} = 125\mu f$

$$ESR_{24} = \frac{0.01 \times 24}{1} = 240m\Omega$$

Adding a ceramic capacitor with a value between 0.1μf to 1μf, in parallel to each of the output capacitors is a standard practice to provide high frequency decoupling for the Vcc (Input terminal of the MOSFET switch) and to provide a reservoir for the peak currents required to turn on the power switch.

CHAPTER FOUR

4.0 RESULTS AND DISCUSSION

The design and computations of chapter four were followed up by simulations and the construction works respectively.

4.1 Simulations and Results

Simulation of the circuits entailed use of:

i. MULTISIM

ii. Pulse width modulation controller PWMCM (U5) and

ii. High frequency transformer (U1) with transformation ratio 2:1, from samples of SMPS in the MULTISIM library (with the advice of Patrick Noonan of National instruments discussion forum, as per appendix A).

iii. AC power supply

RMS voltage =220V

Frequency =50Hz

Voltage offset =0V

The stage by stage simulations involved the following:

a. Input A.C. / input rectifier circuit DC out-put
b. PWM controller and MOSFET gate
c. MOSFET switch output
d. High frequency transformer output

4.1.1: Input Rectifier Circuit /Waveform

The input AC / rectifier output waveforms are shown in Figure 4.1 below. The circuit performed satisfactorily with output current $I_{dc=}$ 23.1A and peak DC output voltage at 312V.

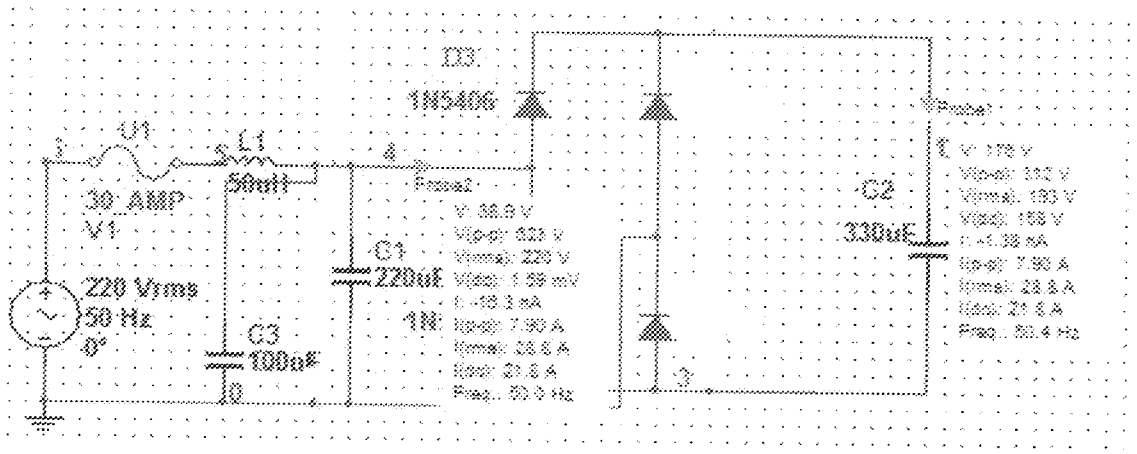

Figure 4.1a: Rectifier Circuit.

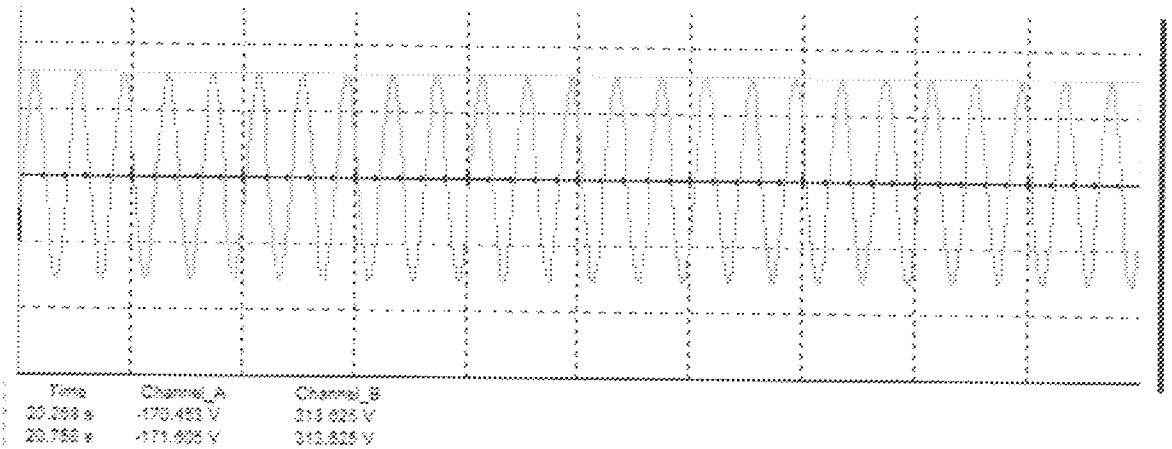

Figure 4.1b: Input AC Voltage/Output DC Voltage Waveforms.

Table 4.1 shows the simulation result of input rectifier circuit.

Table 4.1: Simulation Result of Input Rectifier Circuit.

	Channel A	Channel B
x1	0.0000	0.0000
y1	0.0000	1.2326e-032
x2	0.0000	0.0000
y2	0.0000	1.2326e-032
dx	0.0000	0.0000
dy	0.0000	0.0000
1/dx		
1/dy		
min x	0.0000	0.0000
max x	13.2753	13.2753
min y	-311.1270	0.0000
max y	311.1270	313.6254
offset x	0.0000	0.0000
offset y	0.0000	0.0000

4.1.2 PWM Controller UC3842

This IC that provides the duty cycle was tested next using oscilloscope to observe the waveform. The controller IC UC3842 was found not to be working. Search was conducted to find out reason for this. It was found out from national instrument discussion forum that that the student version of MULTISIM 10.0 does not have simulation model of UC3842.National instrument Engineers however recommended use of equivalent IC PWM CM found in their demonstration sample. This IC was consequently used to obtain the result shown in Figure 4.2 below. Output voltage measured using oscilloscope was found to be 10.848V sufficient to trigger the MOSFET switch into conduction.

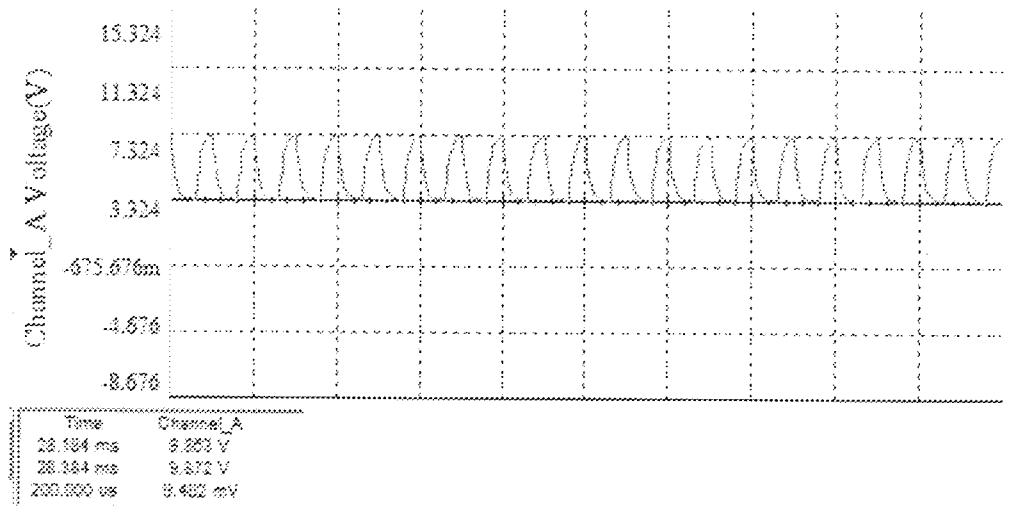

Figure 4.2: Simulation Output of IC Controller PWM CM.

4.1.3 MOSFET Switch

Simulation result of the voltage across the MOSFET switch is shown in Figure 4.3 below. Voltage across the MOSFET was observed to be 340V.This indicates a very big safety margin (42.5%) on the selected 800V MOSFET.

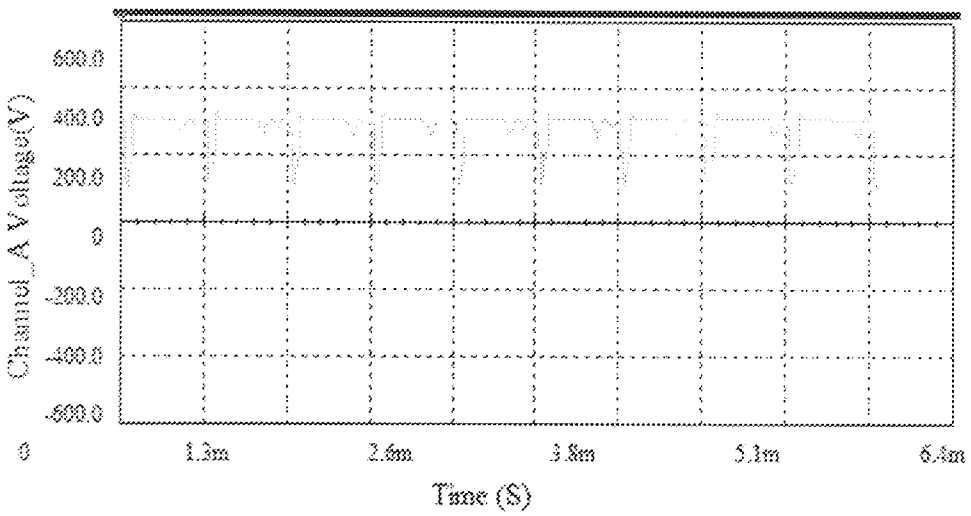

Figure 4.3: MOSFET Switch Voltage Waveform.

4.1.4 High Frequency Transformer Output

MULTISIM recommends use of single output linear transformers found in its library for simulation. The only adjustable parameter in this model is the primary to secondary turns ratio. The simulation was done by changing the transformation ratio of 0.5 to 0.2 to obtain 69.63V.The wave form is shown in Figure 4.4 below

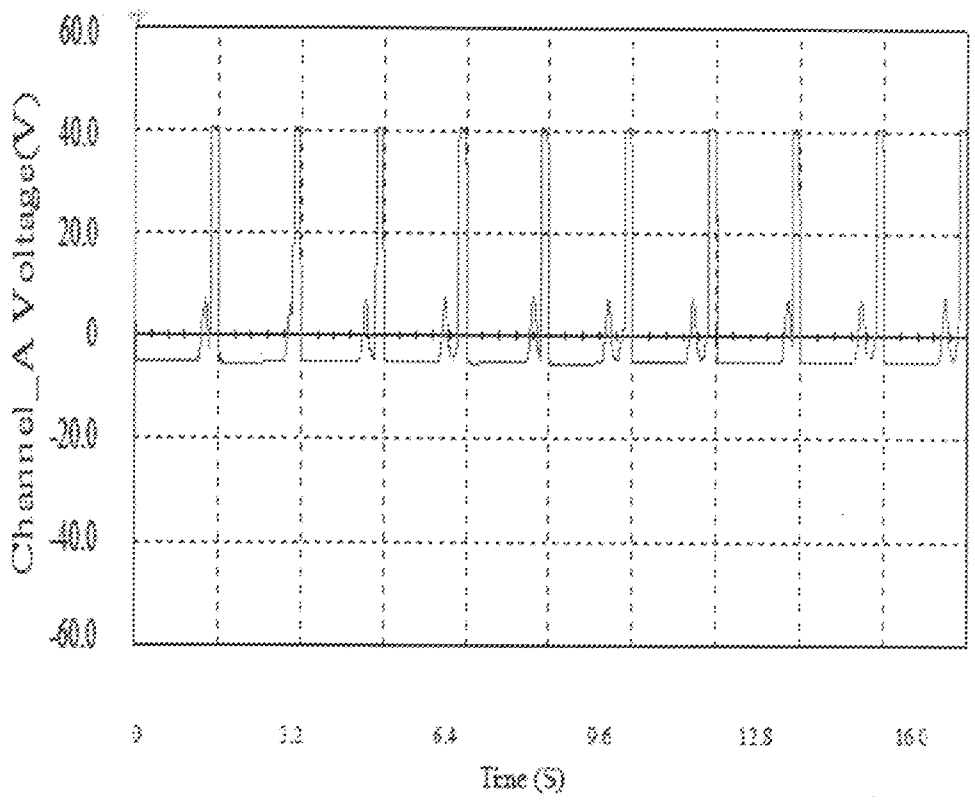

Figure 4.4: Transformer Output Voltage Waveform

Figure 4.5 represents Output Voltage waveform of high frequency diode.

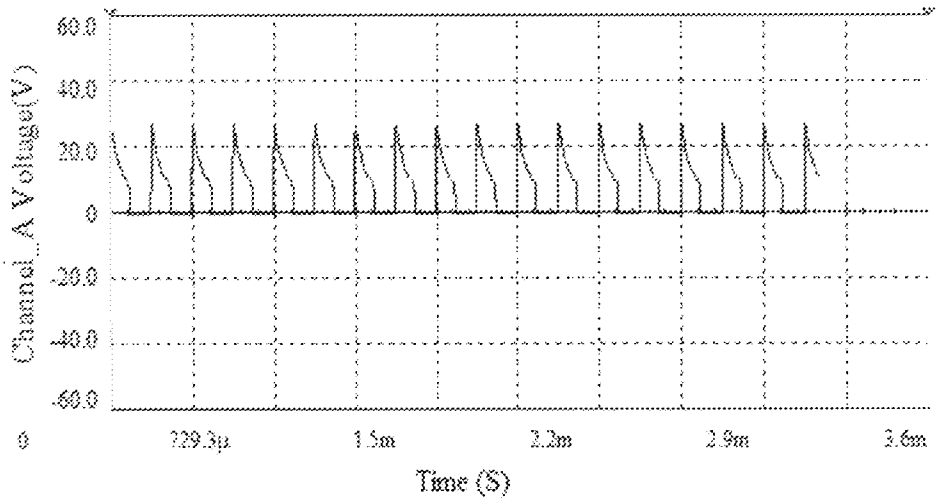

Figure 4.5: Output Voltage Waveform of High Frequency Diode

Table 4.2 gives the simulation result of high frequency diode as simulated.

Table 4.2: Simulation Result of High Frequency Diode

	Channel A
x1	9.8306m
y1	21.9103
x2	9.8306m
y2	21.9103
dx	0.0000
dy	0.0000
1/dx	
1/dy	
min x	9.8306m
max x	12.5240m
min y	-406.7175m
max y	27.0054
offset x	0.0000
offset y	0.0000

4.1.6 Output Voltage Simulations results

Figure 4.6 represents the simulation output voltage of 6v, 12v and 24v terminals

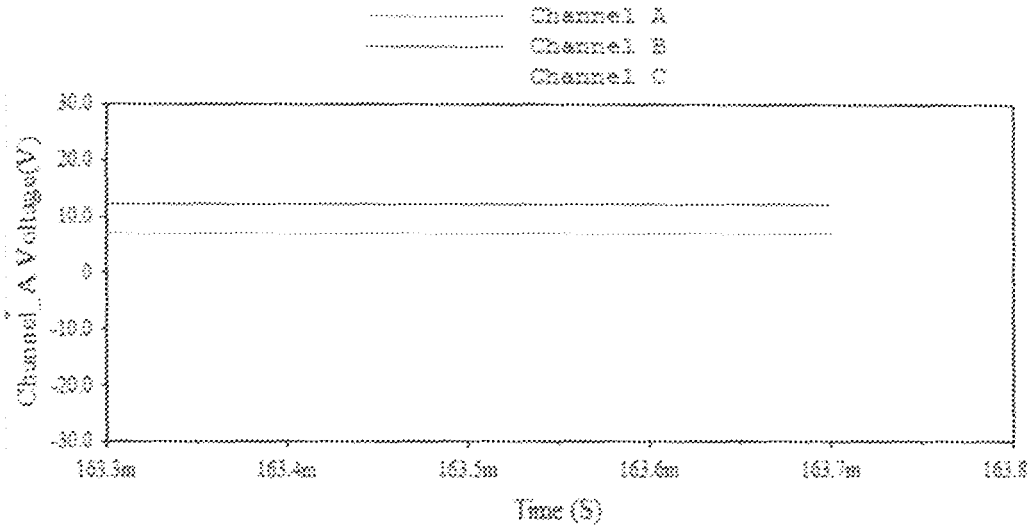

Figure 4.6: Simulation Output voltage simulation results of 6V, 12V and 24V terminals

Table 4.2 shows the result of output terminals as simulated.

Table 4.3: Simulation Result of Output Terminals

	Channel A	Channel B	Channel C
x1	163.2804m	163.2804m	163.2804m
y1	6.8723	12.1726	22.0483
x2	163.2804m	163.2804m	163.2804m
y2	6.8723	12.1726	22.0483
dx	0.0000	0.0000	0.0000
dy	0.0000	0.0000	0.0000
1/dx			
1/dy			
min x	163.2804m	163.2804m	163.2804m
max x	163.6810m	163.6810m	163.6810m
min y	6.8490	12.1644	22.0483
max y	6.8731	12.1736	22.0800
offset x	0.0000	0.0000	0.0000
offset y	0.0000	0.0000	0.0000

4.2 Construction:

Following the satisfactory result of the simulations obtained by slight adjustment in component values, construction of the regulated DC power supply was carried out using the amended drawing shown in Figure 4.7 below. The following processes were involved:

1. Selection of component values from component data sheets.
2. Interconnection of components on Vero board to build the sub-circuits. Each sub-circuit was tested separately.
3. Interconnection of sub-circuits to build the complete circuit. After every interconnection a test was carried out

Furthermore heat generating devices like transformers were mounted some distances away from semi-conductor devices like the power MOSFET switch. The MOSFET was thereafter mounted on heat sink for effective heat dissipation.

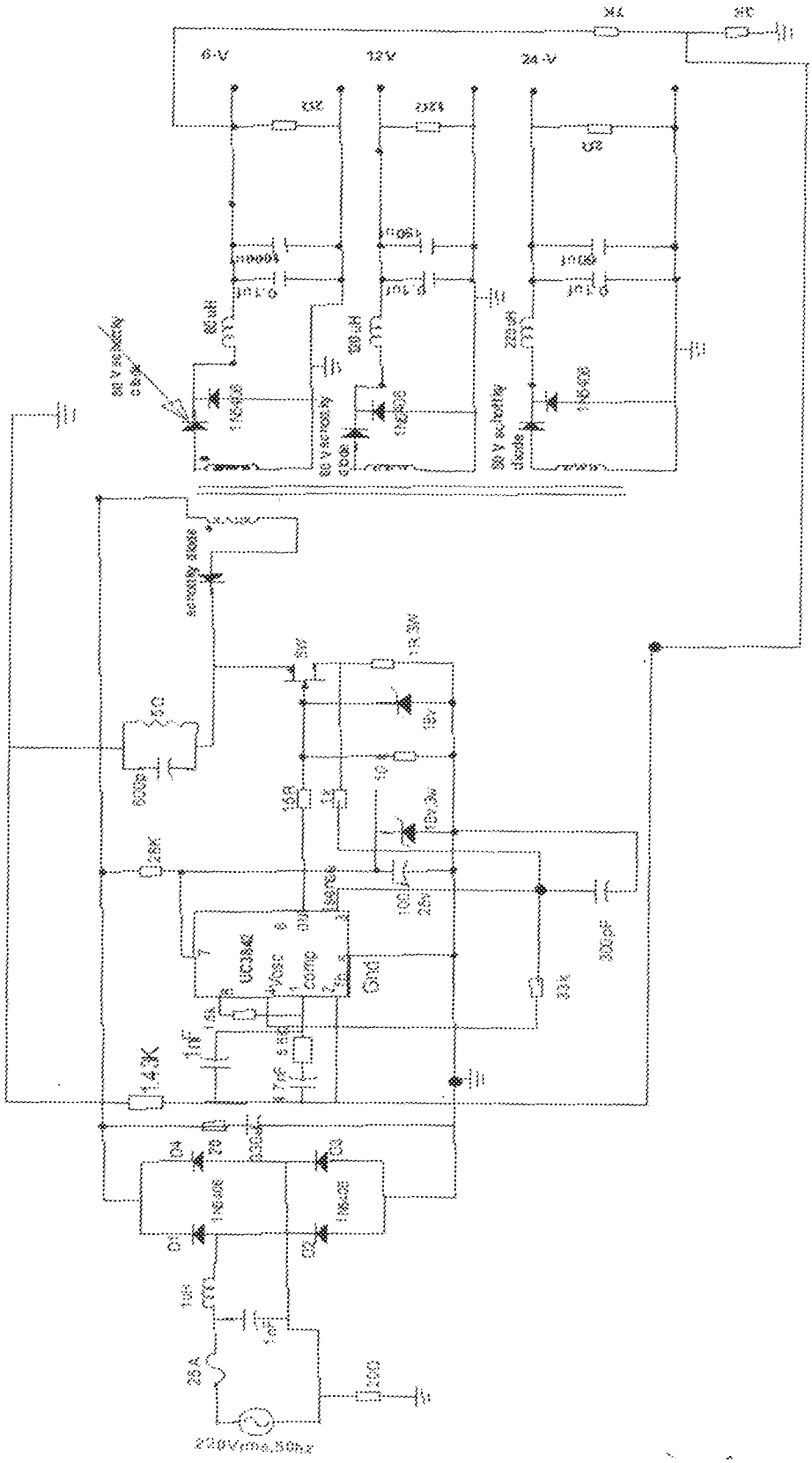

Figure 4.7: Circuit for Construction

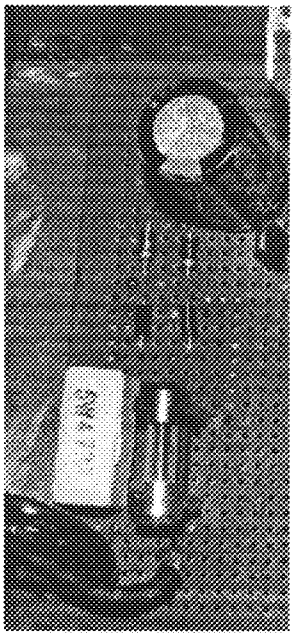

Plate I: Input section of converter

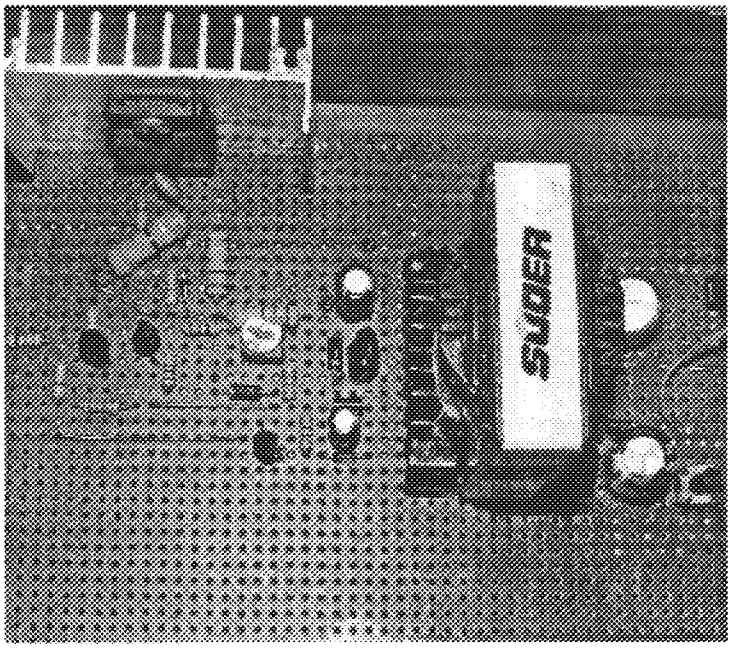

Plate II: Converter control section

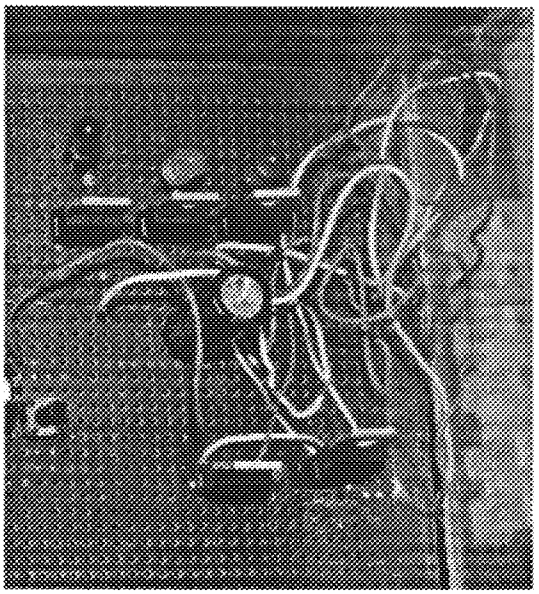

Plate III: Output section of converter

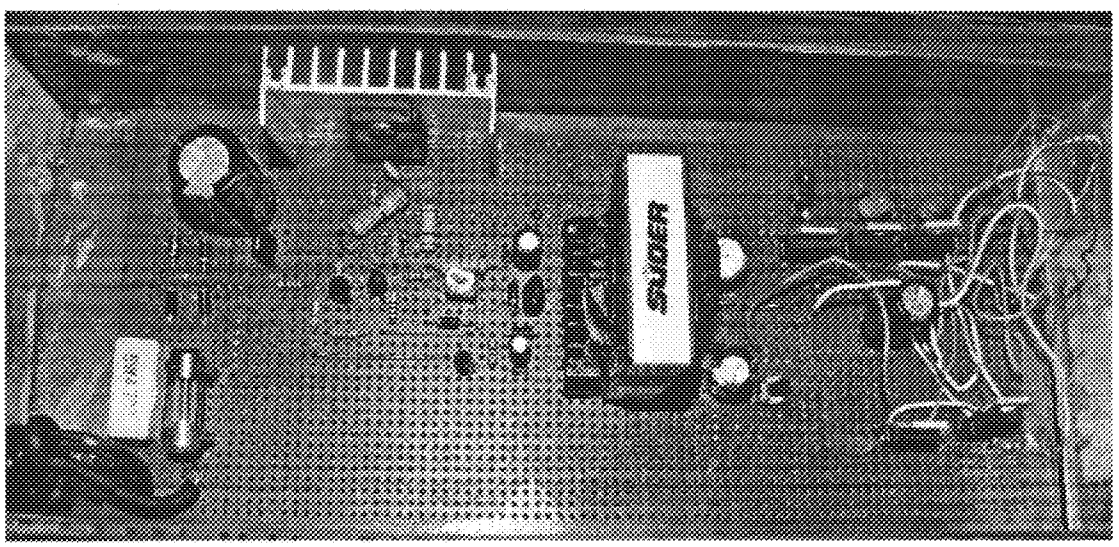

Plate IV: Complete circuit

4.3 Testing and results: Testing was carried using a multi-tester.

4.3.1 Input Rectifier: The AC input rectifier voltage was measured as 235V while the average output DC voltage was measured as 210V.

4.3.2 Output Voltages: The measured output voltages on open circuit were found to be as follows:

i. 5.8V for 6V

ii. 12V for 12V

iii. 23.5V for 24V

These were very satisfactory.

4.4 Stability Analysis

To investigate stable operation of the forward converter a stability analysis was carried out using Bode plot .Figure 4.12a shows the equivalent model of the forward converter. The transfer function is first derived as shown below and thereafter the Bode plot was obtained using *MATLAB*.

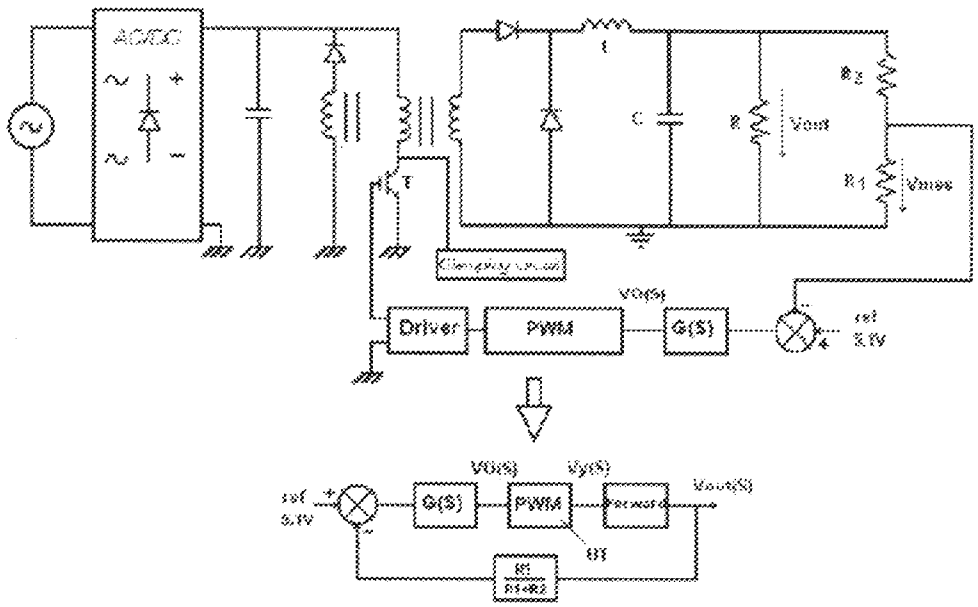

Figure 4.12a: Approximate representation of the forward converter (Mohan *et al* 2003)

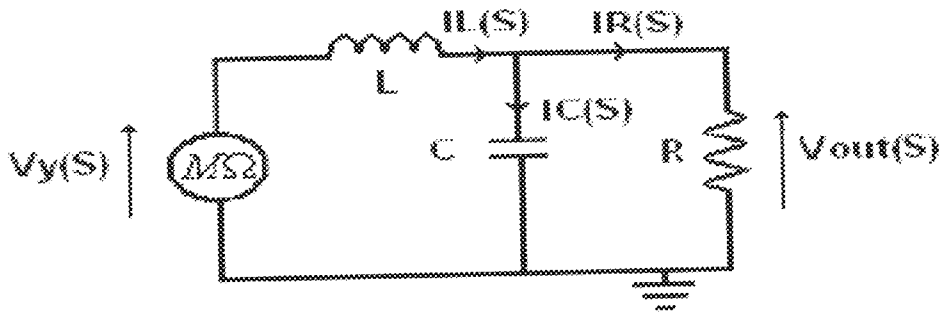

Figure 4.12b: Equivalent scheme of a conducting forward converter transformer and output filter.

The Bode representation of the open loop control system of the converter is shown in Figure 4.12c below.

the bode plot shows the following data:

Phase margin =6.15degrees

Delay margin =2.52sec

Frequency=4.26 E^{-4} rad/sec

The closed loop was confirmed to be stable.

Peak gain= 28.3db

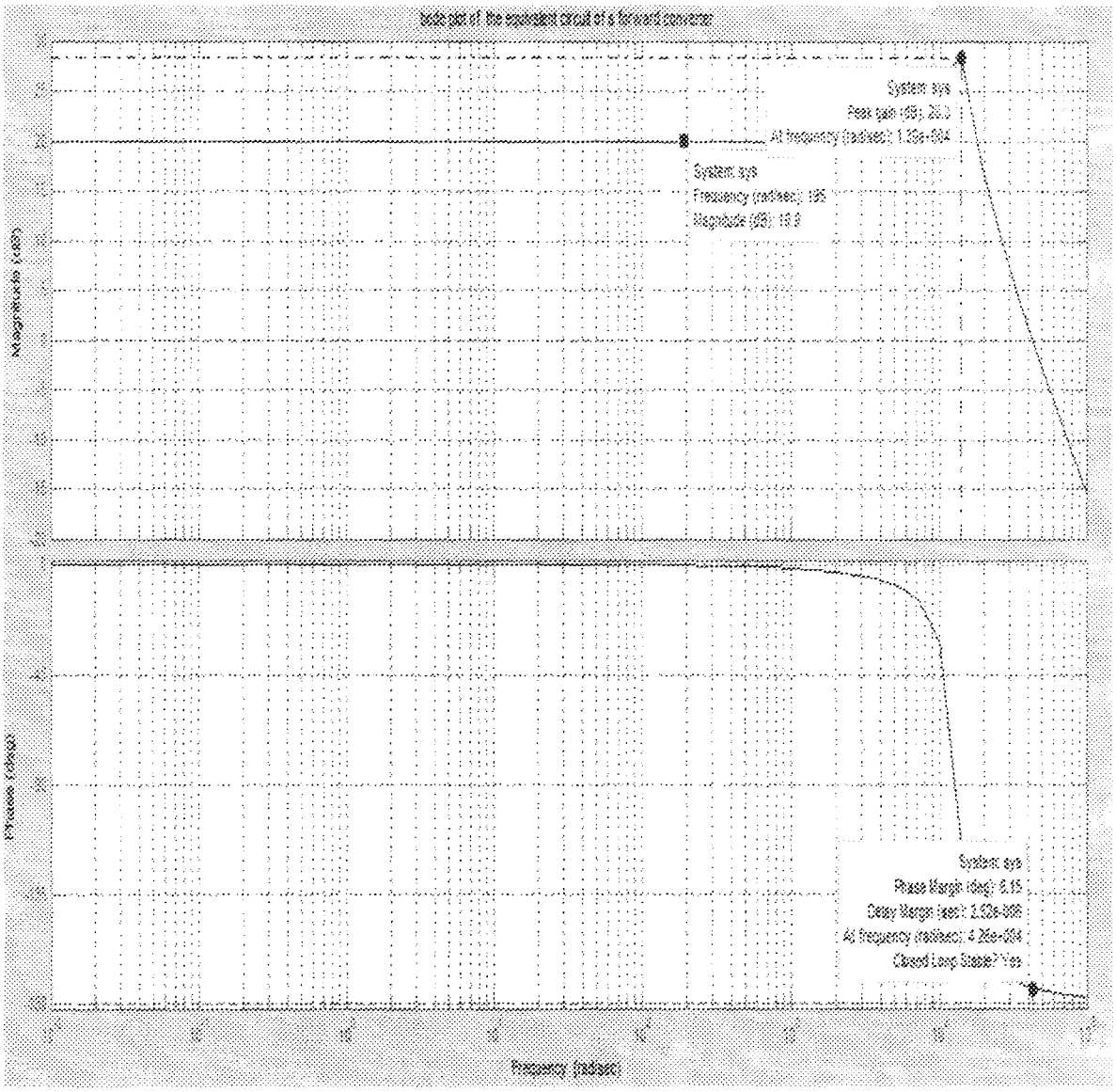

Figure 4.12c: Bode plot of equivalent converter circuit

CHAPTER FIVE

5.0 CONCLUSIONS AND RECOMMENDATIONS

5.1 CONCLUSIONS

5.1.1 Observations:

A model of the transformer was initially wound for the 6V terminal. The transformer was thereafter connected to the designed circuit. Voltage output measured was 20V. The number of turns for the transformer and the 12V and 24V were consequently adjusted before winding the transformer again.

The transformer was reconnected into the circuit and further tests carried out. In the course of the tests, the circuit was observed to foul, leading to further investigation of the circuit, using N1 Multism. A resistor was therefore introduced in the earth path of the practical converter to the work.

5.1.2 Controller IC: The controller output voltage was measured 9.5Vdc and the value agrees with recommended manufacturer value of 10V for triggering the MOSFET switch into conduction (Figure 4.26 above)

5.1.3 Input Voltage:

The peak currents are normally high when using a rectifier /capacitor input from an AC line. This peak current became very high at high input voltage of 220V and led to repeated blowing of the input fuse. The converter operation was however stable between 160Vrms and 200Vrms.

5.1.4 MOSFET drain to source voltage: At high input the voltage measured across the MOSFET switch was 340V. This indicates sufficient margin (42.5%) on the selected 800V MOSFET.

5.1.5 Output Voltages: The outputs were evaluated by varying the load on the regulated output of 6V and observation made on the other two terminals of 12V, and 24V that were not regulated

In carrying out the validation of the input rectifier the following equations were regulated. The results obtained are as stated below:

Full Load: Maximum load on the 6V terminal were as follows:

$I = 13.7A$, $I_{dc} = 10.83A$, $V_{dc} = 5.8V$, $I_{ripple} = 27\%(2.87A)$

For 12V terminal: I=6.27A, $I_{dc} = 5.39A$, $V_{dc} = 12.6V$, $I_{ripple} = 0.88A(14\%)$

For 24V terminal: $I = 3.81A$, $I_{dc} = 3.81A$, $I_{dc} = 2.86A$, $I_{ripple} = 0.95A(25\%)$

Light Load: Results obtained when the 6V terminal was lightly loaded, that are: $I = 7.44A$, $I_{dc} = 6.7A$, $I_{ripple} = 0.74A(9\%)$ are as stated below :

For 12V: $I = 6.31A$, $I_{dc} = 5.38A$, $I_{ripple} = 0.93A(15\%)$

For 24V: $I = 3.81A$, $I_{dc} = 2.91A$, $I_{ripple} = 0.9A(24\%)$

The unregulated outputs at maximum load on the 6V terminal showed lower output values. Both unregulated outputs were high when they were lightly loaded and the 6V was at its maximum. This is due to the resistive losses in the 12V and 24v output paths.

With the above results it is reasonable to conclude that the converter constructed has met most of the design requirements.

5.2 Recommendations

Some problems were encountered in the course of this project .They include the following:

i. In the course of simulation it was discovered that some of the MULTISIM components do not have simulation models in its library, an example being the controller IC, UC3842. A lot of time was therefore spent searching for solution, which was to copy the models in the *switch mode sample circuits.*

ii. Non availability of multiple output winding transformers for simulation in the MULTISIM library hence the three outputs were simulated by looping the outputs.

iii. Non availability of an off-the shelve transformer led to the winding of the high frequency transformer locally, with provision for reset winding. When this was connected to the circuit, burning of the IC regulator and the MOSFET switch occurred several times implying that the transformer core was not being reset properly. This led to the introduction of the RCD clamp circuit to obtain a stable operation.

iv. Some components were found to have ratings which differed greatly from their actual values and therefore failed when subjected to the voltage ratings on their bodies.

In view of the observations made above, it may therefore be recommended as follows:

i. To ensure that there is good cross regulation between the regulated output and the unregulated outputs, it is recommended that the project be carried out using coupled inductors instead of individual inductors. In this way any change in load in anyone output will affect the other outputs equally thereby ensuring stability of operation.

ii. A professional simulation package will give better simulation results as it has all the simulation models in its library and hence a better designed power supply. It is therefore recommended that students be made to have access to professional simulation packages instead of student version that has so many limitations.

iii. The converter safety against radio and electromagnetic interference was implemented by using a metallic enclosure provided with ventilating ducts. Terminal for earthing of the converter was also provided. Other safety methods could however be explored in future project work.

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APPENDICES

Appendix A: NI simulation forum (UC 3842 not working)

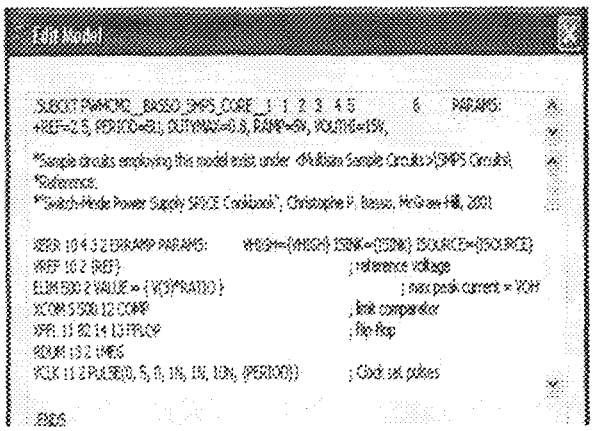
Re: UC3842 model is not working at all Option

Hi[illegible]

Hello - attached is the UC3842 model you are looking for in v10.1 in a flyback topology (modified from existing SMPS samples). I suggest that for Switch Mode Power Controllers that you also reference the SMPS samples (File -> Open Samples -> SMPS). Many of sample circuits in the topologies shown have corresponding SMPS controller ICs models with parametric values that allow you to match the specifications closely with the manufacturer's IC specifications. The sample I included swaps out the BASSO model for the UC3842 model.

Recently a customer looking for a Linear Technologies SMPS controller (not in the DB) was successfully able to use a corresponding PWM/CM BASSO model in lieu of actual orig SPICE model as many of these are proprietary or encrypted.

These BASSO models are relatively easy to use. For a given topology (CM or VM: buck, boost, flyback), open up the sample circuit. Adjust the model by opening up it SPICE model of the controller within the circuit (Double-click on part -> Edit Model button). Adjust the 'Current Instance Parameters' to match those found on the datasheet as shown below:



Re: UC3842 model is not working at all!

Options ▾

[redacted]

Could it be possible that are using a component that does not have a simulation model attached to it?

I quickly tested the UC3842 component, and correctly saw 5V on the reference pin. But the variants of this component (ie. the UC3842A_DIP8, UC3842_SO8 etc.), are for schematic capture/layout only and have no simulation models linked to them. If this is the case, try swapping the component for the UC3842.

If you're still having trouble, post your circuit. It's always easier to pinpoint the issue that way!

Natasha Baker
R&D Engineer
National Instruments

Join the NI Circuit Design Community
Follow Multisim on Twitter!

Re: UC3842 model is not working at all!

Options ▾

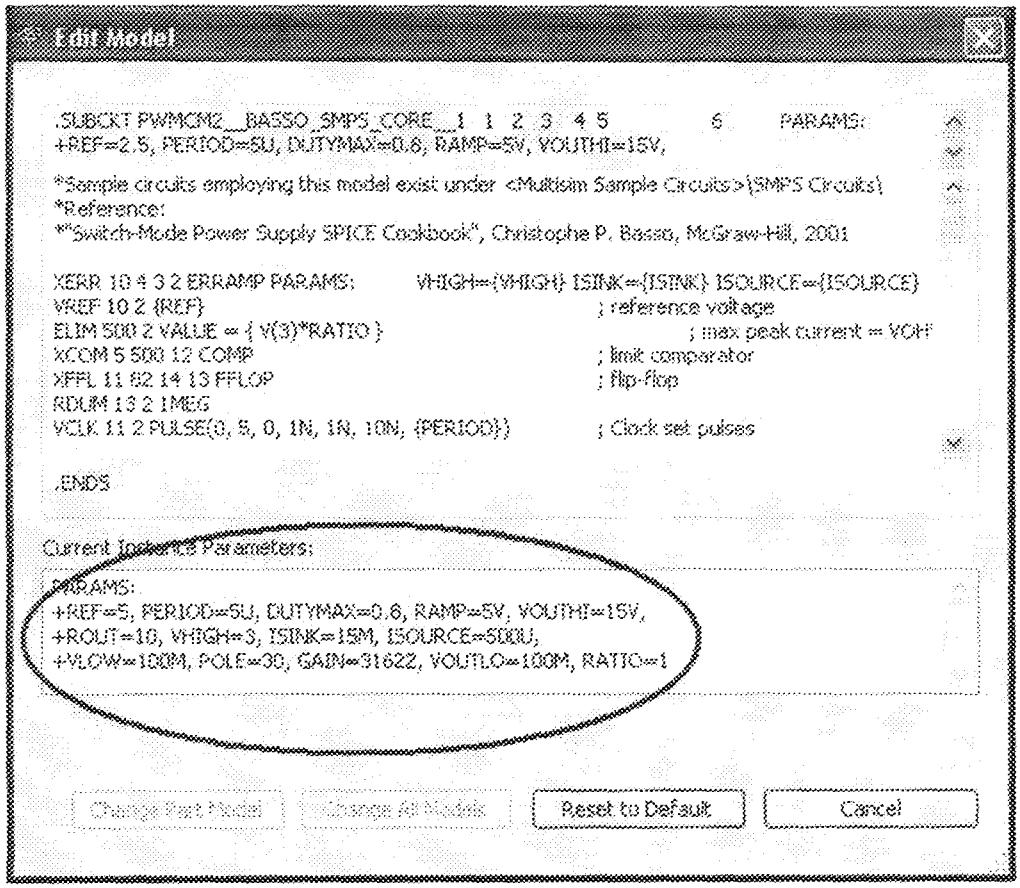
[redacted]

Nick_Barnes,

Hello - attached is the UC3842 model you are looking for in v10.1 in a flyback topology (modified from existing SMPS samples). I suggest that for Switch Mode Power Controllers that you also reference the SMPS samples (File -> Open Samples -> SMPS). Many of sample circuits in the topologies shown have corresponding SMPS controller ICs models with parametric values that allow you to match the specifications closely with the manufacturer's IC specifications. The sample I included swapped out the BASIC model for the UC3842 model.

Recently a customer looking for a Linear Technologies SMPS controller (not in the DB) was successfully able to use a corresponding PWMCM BASIC model in lieu of the actual orig SPICE model as many of these are proprietary or encrypted.

These BASIC models are relatively easy to use. For a given topology (CM or VM, buck, boost, flyback) open up the sample circuit. Adjust the model by opening up the SPICE model of the controller within the circuit (Double-click on part -> Edit Model button). Adjust the 'Current Instance Parameters' to match those found on the datasheet as shown below.



Appendix B: MATLAB Code for plot of forward converter transfer function.

```
>> %script file:forward converter crtransfer function
% Purpose :To plot the transfer function
%  Date        programmer   Description of change
 %  ====        ==========   =====================
 % 30/9/2011     OC Emelogu    Nil
  %num =coefficients of numerator variables
  %den =coefficients of denominator variables
  %w log of the frequency range
  num=[0 0 9.94];
  den=[0.00000006 0.000025 1];
  w=logspace(-3, 5);
  bode(num,den,w);
  title('Bode plot of a forward converter')
``
```

Appendix C: Derivation of forward converter transfer function

We apply *Kirchhof's* current law to the forward converter's equivalent circuit to obtain the governing equations and use Laplace transform to solve the equations.

$$iR_{(s)} = \frac{V_{out(s)}}{R}$$

$$i_{c(s)} = sCV_{out(s)}$$

$$i_{L(s)} = i_{c(s)} + i_{R(s)} = sCVout(s) + \frac{V_{out(s)}}{R}$$

$V_{L(s)} = sLi_L(s)$ and $V_L(s) = V_s(s) - V_{out}(s)$ so that.

$$\frac{V_{out(s)}}{V_i(s)} = \frac{1}{1 + s^2LC + s\frac{L}{R}} \qquad (1)$$

$$\text{Now, } V_s(s) = \mathrm{D}(s)\, V_{in} \frac{N_s}{N_p} \qquad (2)$$

$$D_{(s)} = \frac{V_c(s)}{U_T} \qquad (3)$$

Combining equations 1,2 and 3 above we have :

$$\frac{V_{out}(s)}{V_{c(s)}} = \frac{V_{in} N_s}{U_T N_p} \Big/ 1 + s^2LC + s\frac{L}{R} \qquad (4)$$

Designing the controller for the worst situation, which occurs when, R =∞, then P_{out} =0 and equation 5.6 reduces to:

$$H(s) = \frac{V_{out}(s)}{V_o(s)} = \frac{V_m N_s}{U_T N_p} \Big/ 1 + s^2 LC \qquad (5)$$

The cut off frequency is $f_o = \frac{1}{2\pi\sqrt{LC}}$ and the static gain $K = \frac{V_m N_s}{U_T N_p}$

Where: U_T =2.4V is the value of the triangular voltage provided by the IC manufacturer.

L =output inductance

C=output capacitance

N_p=high frequency transformer primary winding

R= load resistance

V_{out} =output voltage across load resistor

V_o =input voltage to the output filter network

N_s = high frequency transformer secondary winding

V_c =output voltage of error amplifier or control voltage, $V_{control}$

From the above it can be seen that when R =∞, Pout will be zero and the transfer function reduces to:

$$H(s) = \frac{V_{out(s)}}{V_o(s)} = \frac{V_m N_s \times 1/U_T N_p}{1 + s^2 LC}$$

The cut off frequency is given by =$f_o = \frac{1}{2\pi\sqrt{LC}}$

And the static gain $K = \frac{V_m N_s}{U_r N_p}$

The controller design is based on the controlled output of (6V/15A),with output parameters as C=1000μf and L=60μH. Substituting the above parameters into equation 5.6 the transfer function becomes

$$H(s) = \frac{9.94}{0.00000006s^2 + 0.000025s + 1}$$

Appendix D: Cost Analysis of Converter

Component	No.	Rate	Amount
30 A Switch	1	200	200
25A Fuse	1	50	50
Thermistor	1	200	200
50μH Inductor	2	40	80
218 μH „	1	40	40
220μH „	1	40	40
400μF/400V Capacitor	1	450	450
100μF „	2	100	200
1mF „	1	100	100
417μF „	1	100	100
125μF „	1	100	100
1nF. Ceramic Capacitor	2	30	60
4.7nF „ „	1	30	30
1nF „ „	3	30	90
300pF „ „	1	50	50
600pF „ „	1	50	50
Diodes IN5406	4	20	80
18V zener diodes	2	10	20
6V „ „	1	10	10
12V „ „	1	10	10
24 „ „	1	10	10
80V shottky diodes	2	20	40
40V „ „	4	20	80
400W pulse transformer	1	500	500
800V MOSFET	1	250	250
UC3842 IC controller	1	200	200
Vero board	1	200	200
Casing	1	400	400
Resistors	5	20	100
Nuts, bolts, screws	lots	-	200
Total	-	-	4640.00

Appendix E: Reliability analysis of forward converter

Component	No Used- n_i	Basic failure rate, λ (% /10^3 hr)	Weighting factors due to : Env. W_e	Temp. W_t	ratin W_r	Over all failure rate λ_{ai} = $n_i w_e \lambda_i w_t w_r \left(\%/10^3\ hr \right)$
Switch	1	0.02	3	1.5	3	2.7
Thermistor	1	0.06	3	1.5	3	0.81
Fuse	1	0.02	1.5	1.5	2	0.09
Inductor	4	0.05	3	1.5	3	2.7
Electrolytic capacitor	7	0.02	3	1.5	3	1.89
ceramic Capacitor	8	0.03	1.5	1.5	3	1.62
Diodes	4	0.05	1.5	1.5	1.5	0.675
Pulse transformer	1	0.08	3	1.5	3	1.08
Power MOSFET	1	0.05	1.5	1.5	2	0.225
Schottky diodes	7	0.05	1.5	1.5	1.5	1.18
Resistors	15	0.05	1.5	1.5	2	3.375
Zener diodes	5	0.03	1.5	1.5	2	0.675
Connectors	100	0.001	1.5	1.5	2	0.45
IC controller	1	0.05	1.5	1.5	2	0.225
						17.695%

From the result above, the converter failure rate = 17.695% =0.17695

System reliability, $R = e^{-\lambda_{ai} t}$ (Oroge, 1991)

Where λ_a = total system failure rate, t = period of operation in hours

Therefore for a continuous operation for 264 days and 8 hours daily, the reliability will be:

$$= e^{-0.17695 \times 0.001 \times 2112} = e^{-0.3738368}$$

$$=0.685$$