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A COMPARATIVE STUDY ON SVC AND CAPACITOR PLACEMENT FOR POWER LOSS REDUCTION IN THE 132kV SHIRORO POWER TRANSMISSION NETWORK

Tsado, J.; Alimi, A.T.; *Sadiq, A. A.; and Habibu, H.

Department of Electrical and Electronics Engineering, Federal University of Technology, Minna, P.M.B 65, Nigeria

*Corresponding Author: ahmad.abubakar@futminna.edu.ng

ABSTRACT

Evacuation of bulk electrical power generated at remote locations over high voltage transmission networks is preferred, due to economical and reliable supply. However, the inherent characteristics of the transmission facilities results into unacceptable levels of power quality; often measured in terms of voltage deviation and active power losses. These power quality issues increase with the length of the transmission network. Conventionally, Capacitor banks were placed appropriately to mitigate these problems, while recently, FACTS technology is receiving much attention to improve power quality indexes. This paper compares the Effect of Static VAR Compensator (SVC) and Capacitor placement on power loss reduction of the 132kV Shiroro transmission network. The 132kV Shiroro transmission network was modelled as a 10 buses network. Ant colony optimization (ACO) technique was employed for optimal placement of SVC in the modelled network using Power System Computer Aided Design/Electromagnetic Transient and DC (PSCAD/EMTDC) software. The result obtained shows that the total real power losses of the network were 8.43MW and 3.59MW with capacitor and SVC placement respectively. In addition, voltage profile of the system improved and sums of voltage deviation were 28.86volts and 18.55volts with capacitor and SVC optimal placement respectively. It was further observed that SVC reduced the transient effects experienced on the network especially during single line to ground fault condition.

Keywords: SVC, Capacitor, PSCAD, Power Loss & Transmission Network.

1.0 INTRODUCTION

In the past few years the demand for electrical energy has increased significantly and as some result transmission systems operators are facing power transmission capability limitation crisis. The limitations occur while maintaining a balance between stability and capability of transmission line. As a result, the power transmission capability of the network is often under-utilized. This results in non-optimal operation of the energy transmission systems. One among the solutions to this problem of increasing power transmission capability is construction of new transmission lines, which is associated with the difficulties of acquiring new right of ways and huge capital investment (Ramachandra and Ramalinga, 2009).

In interconnected power systems, such as the Nigerian power system network, like all other power system, no matter how carefully the system is designed, losses are present. Electric power losses are a form of wasteful energy caused by external factors or internal factors, and energy dissipated in the system. They include losses due to resistance, atmospheric conditions, theft, miscalculations and losses incurred between sources of supply to load centre (or consumers) (PHCN, 2014). Loss minimization and quantification is very vital in optimal operations of power system; knowing how losses occur, steps can be taken to limit and minimize them. These will lead to effective and efficient operation of the system. Therefore, with optimal placement and sizing of FACTS, the existing power generation and transmission networks can be efficiently used without having the need to build new transmission lines and at the same time save cost. Basically, losses in electrical power system can be either losses caused by internal factors known as technical losses or those cause by external factors known as non-technical losses (Anumaka, 2012).

In view of the forgone, Flexible Alternating Current Transmission Systems (FACTS) are devices emanating from recent innovative technologies that are capable of altering voltage, phase angle and/or impedance at particular points in power systems (Hingorani & Gyugyi, 2000). Their fast response offers high potentials for power system stability enhancement in the form of steady state flow control (Darabian & Jalilvand, 2017). In addition, FACTS devices are also used to control the power flow in the transmission lines as well as the bus voltages (Nwohu, Isah, Usman, & Sadiq, 2016). Several efforts were made to find ways to ensure power quality of the system in terms of voltage stability (Udgir, Srivastava, & Pandit, 2014). It is found that FACTS devices are good choice to improve the voltage stability in power systems (Balachennaiah, Suryakalavathi, & Nagendra, 2015). Moreover, reduction of system losses is of paramount importance because of its financial, economic and socio-economic values to the utility company, customers and the host country.

FACTS devices have been deployed to reduce real power losses as reported by various literatures, such as: (Benabid & Boudour, 2008), Static VAR Compensators (SVC) and Thyristor Controlled Series Compensators (TCSC) were used to enhance voltage stability, reduce power loss and voltage deviations in IEEE 14 bus test system; while the use of Differential Evolution to placed SVC aimed at voltage security enhancement and loss reduction in IEEE 30 bus test system was reported in (Udgir *et al.,* 2014). Again, (Balachennaiah *et al.,* 2015) optimized real power loss and voltage stability limit using UPFC. Similarly, (Sahu & Dubey, 2015) use Particle Swarm Optimization (PSO) to determine the location of STATCOM in IEEE 14 bus network aimed at voltage profile improvement, power losses and THD reduction. Recently, (Nwohu *et al.*, 2016) deployed TCSC for real power loss reduction.

Among the FACTS controllers, Static Var Compensator (SVC) provides fast acting dynamic reactive compensation for voltage support during contingency events (Darabian & Jalilvand, 2017) which would otherwise depress the voltage for significant time duration. SVC also dampens power swings and reduces system losses by optimized reactive power control (Nwohu, 2009).

Owing to these facts, the potential benefits of SVC for power loss reduction on the 132kV Shiroro transmission is investigated. This article therefore, adopts the use of SVC among other shunt devices (such as Static synchronous compensation STATCOM) for providing power loss reduction in addition to damping of transient disturbances to restore bus voltages back to pre-faults profile.

2.0 NETWORK AND SVC MODELLING

A Static VAR Compensator (SVC), whose structure is depicted in Figure 1, is a power quality device, which employs power electronics to control the reactive power flow of the system where it is connected (Kishor, Thakre and Bodhe, 2009). As a result, it is able to provide fast-acting reactive power compensation on electrical systems. The SVC is an automated impedance matching device, designed to bring the system closer to unity power factor. When SVC is connected to power system to regulate transmission voltage, it is then called transmission SVC and when it is connected near large industrial loads to improve power quality, then it is called industrial SVC. Static VAR compensators have their output adjusted to exchange inductive or capacitive current in order to control a power system variable such as the bus voltage. SVC is based on thyristors without the gate turn-off capability. It includes separate equipment for leading and lagging vars; the thyristor-controlled reactor (TCR) or thyristor-switched reactor (TSR) for absorbing reactive power and thyristor-switched capacitor (TSC) for supplying the reactive power. It is low cost substitute for STATCOM. Proper placement of static VAR compensator (SVC) and thyristor controlled series compensator (TCSC) reduces transmission losses, increases the available capacity, and improves the voltage profile (Guneet, 2012). The corresponding V–I characteristics diagram of an SVC as shown in Figure 2 has two different operating regions. Inside the control range, voltage is controllable with an accuracy set by the slope. Outside the control range the characteristic is that of a capacitive reactance for low voltages, and that of a constant current for high voltages. The low-voltage performance can easily be improved by adding an extra TSC bank (for use under low-voltage conditions only).

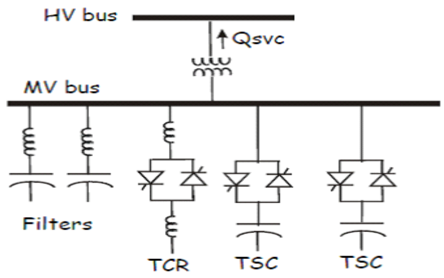

Figure 1: Structure of SVC

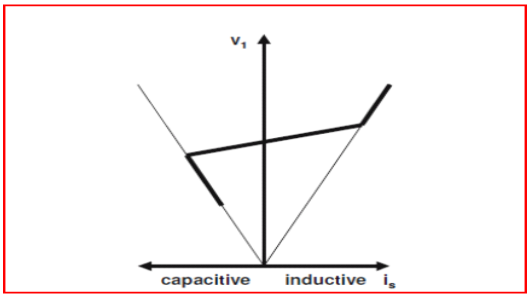

Figure 2: Voltage/Current Characteristics of SVC

The TSR is a TCR without phase control of the current, being switched in or out like a TSC. The advantage of this device over the TCR is that no harmonic currents are generated (Bindeshwar, *et al.*, 2011).

Figure 3 shows the simplified model of a power transmission system, similar to the single machine infinite bus system. Two power system buses are interconnected by a transmission line which is assumed lossless and represented by the reactance XL. $V_1\angle\delta_1$ and $V_2\angle\delta_2$ represent the voltage phasor of the two power system buses with angle $\delta = \delta_1 - \delta_2$ between the two.

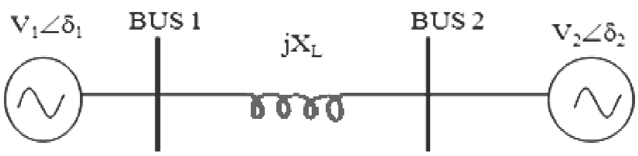

Figure 3: Simplified Model of Power Transmission System

The active P_{12} and reactive power Q_{12} flow between buses 1 and 2 of a lossless transmission line are given by equations 1 and 2.

$$P_{12} = \frac{V_1 V_2}{X_L} \sin(\delta_1 - \delta_2) \quad ... \quad (1)$$

$$Q_{12} = \frac{V_1^2}{X_L} - \frac{V_1 V_2}{X_L} cos(\delta_1 - \delta_2) \quad ... \quad (2)$$

2.1 Objective Function

The objective function is to maximize the reactive power thereby reducing the power losses in the Transmission network considered**.** Complex Current in Power System is define by equation (3).

$$I^* = \frac{S}{V} \quad ... \quad (3)$$

But active power loss is expressed as $P_{loss} = I^2 Z$, while complex power flow into/out of a bus numbered k is $S_k = P_k + jQ_k$. Hence, equation (3) becomes (4).

$$I^* = \frac{P_k + jQ_k}{V_k} \quad ... \quad (4)$$

In general, active power loss is expressed as in equation (5).

$$P_{loss} = \left(\frac{P_k i + jQ_k}{V_k} \right)^2 Z \quad ... \quad (5)$$

Where: S_k is the apparent power, P_k the real power, Q_k the reactive power, V_k the k[th] bus voltage, I^* is Current (Complex), and Z is equivalent impedance all at the k[th] bus for a g buses network. K = 1, 2, 3…g.

The total active power loss for an n lines network is expressed as given in equation (6).

$$P_{loss} = \sum_{i=1}^{n} R_l I_l^2 = \sum_{i=1}^{n} \sum_{j \neq 1}^{n} [V_i^2 + V_j^2 - 2V_i V_j Cos(\delta_i - \delta_j)] Y_{ii} Cos\theta_{ij} \quad \ldots \quad (6)$$

Where: n is the number of lines, R_L is the resistance of line L, I_L is the current through line L, V_i and δ_i are the voltage magnitude and angle at the i[th] node. Y_{ii} and θ_{ii} are the magnitude and angle of the line admittance (Reza, Azah, and Hussain, 2011).

2.2 Modelling of a Static Var Compensator

Static VAR Compensator is a shunt connected FACTS device, which play a major role to regulate voltage profile at the given bus and to reduce the real power loss by adjusting the reactance value of. SVC composed of fixed capacitor (FC) and thyristor controlled reactor (TCR). Figure 4, depicts a typical modelling of an equivalent circuit of a simple SVC. In the equivalent circuit of SVC, it is seen that it has parallel connection of capacitor and inductor. Herein it has the capability to act in capacitor mode or inductor mode to ensure the objective function. The reactance X_{SVC} is assumed as a function of tuning the firing angle of TCR, since it is in parallel connection to the fixed capacitor. Evaluation of SVC parameter becomes major task for enhancement of Voltage profile and real power loss minimization in transmission line. The value of capacitor and the TCR inductive value are formulated as follows;

$$X_C = \frac{V_{bus}^2}{Q_{SVC}} \quad ... \quad (7)$$

$$X_L = \frac{X_C}{2} \quad ... \quad (8)$$

Figure 1 can be appropriately represented by figure 4 where the equivalent reactance of all TSC is X_C.

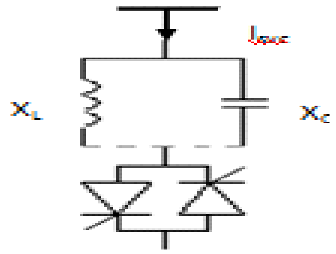

Figure 4: Equivalent circuit of SVC (Prabaakaran, *et al.,* 2013).

Hence, Equivalent SVC reactance is calculated by equation (9)

$$X_{SVC} = \frac{X_c X_{TCR}}{X_C + X_{TCR}} \quad ... \quad (9)$$

Where: V_{bus} is bus voltage in p.u. at which SVC is placed, X_L is Inductive reactance in p.u, X_C is Capacitive reactance in p.u., X_{TCR} Reactance of the thyristor controlled reactor in p.u. Q_{SVC} is reactive power injection by SVC p.u. and X_{SVC} reactance of the SVC p.u.

As the reactive power demand at the bus varies, the susceptance is varied subject to the limits. However, the reactive power is a function of the square of the bus voltage. Hence the reactive power generated decreases as the voltage decreases.

The SVC can both absorb as well as supply reactive power at the bus it is connected to by control of the firing angle of the thyristor elements. By controlling the firing angle α of the thyristors (the angle with respect to the zero crossing of the phase voltage), the device is able to control the bus voltage magnitude. Changes in α results in changes in the current and hence, the amount of reactive power consumed by the inductor. When α = 90°, the inductor is fully activated but is deactivated when α = 180°. Actually, the basic control strategy is to keep the transmission bus voltage within certain narrow limits defined by a controller droop and the firing angle α limits (90° < α > 180°).

2.3 Shiroro Network Modeling in PSCAD

The 10 - bus system network considered was modelled on the PSCAD/EMTDC environment to determine the power loss reduction on the network using SVC. The simulation of the 132kV Shiroro transmission network was carried out to determine the power losses of the system as well as the transient analysis with and without SVC. Figure 5 shows the one-line diagram of the 132kV Shiroro transmission network when connected to the static Var compensator to determine the power losses for both active and reactive power as well as the transient analysis.

2.4 Ant Colony Optimization (ACO) Technique

Research has shown that the behaviour of ants (termites) can be seen as natural model of collective problem solving. The analogy between the way ants look for food and combinational paradigm, which is called ant colony meta-heuristic. The ant colony technique which is meta-heuristic in nature is a simulation of a set of ants which team together to find a solution of an optimization problem by means of a communication route called pheromone.

It was observed that ants are social insects living in colonies. In an attempt to find food, ant move and deposits some pheromone on the ground, which defines the path it follows. By this, other ants moving towards the feeding area can identify the pheromone left by the previous ant and with high probability, decide to follow it.

The pheromone assists in finding the shortest path between two points connected to two or more branches. As a result, the path with more pheromones determines the numbers of new ants that will choose this path at will (Dorigo and Theraulaz, 2004). The ACO was adopted in this research owing to its ease of computation and rapid speed of convergence. Figure 6 shows the ACO algorithms using probabilistic model to generate solutions to the problem under consideration.

Figure 6 shows a flow chart developed for the ACO technique. The following definitions of the algorithm input and output stages parameters are stated.

The initial stage: This is the stage where input parameters are set.

Generation of first node: generating the first node is by calculating the distance between parameters.

Ant tour transition stage: The ant located at the current node chooses the next node and if not satisfactory, the ant moves to the next location based probabilistic transition function and pheromone is converged.

Local Updating State: The optimal location of SVC is achieved as ants visit nodes and change their pheromone level.

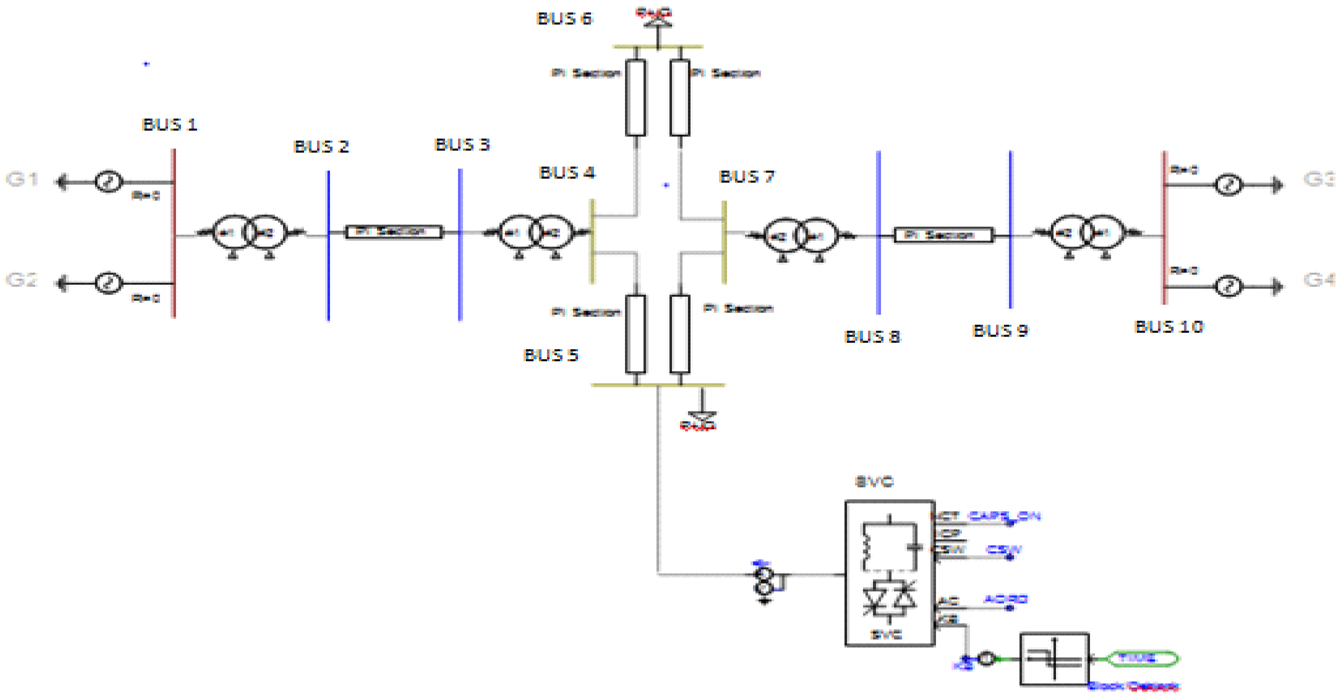

Figure 5: 132 kV Shiroro Transmission Network with SVC

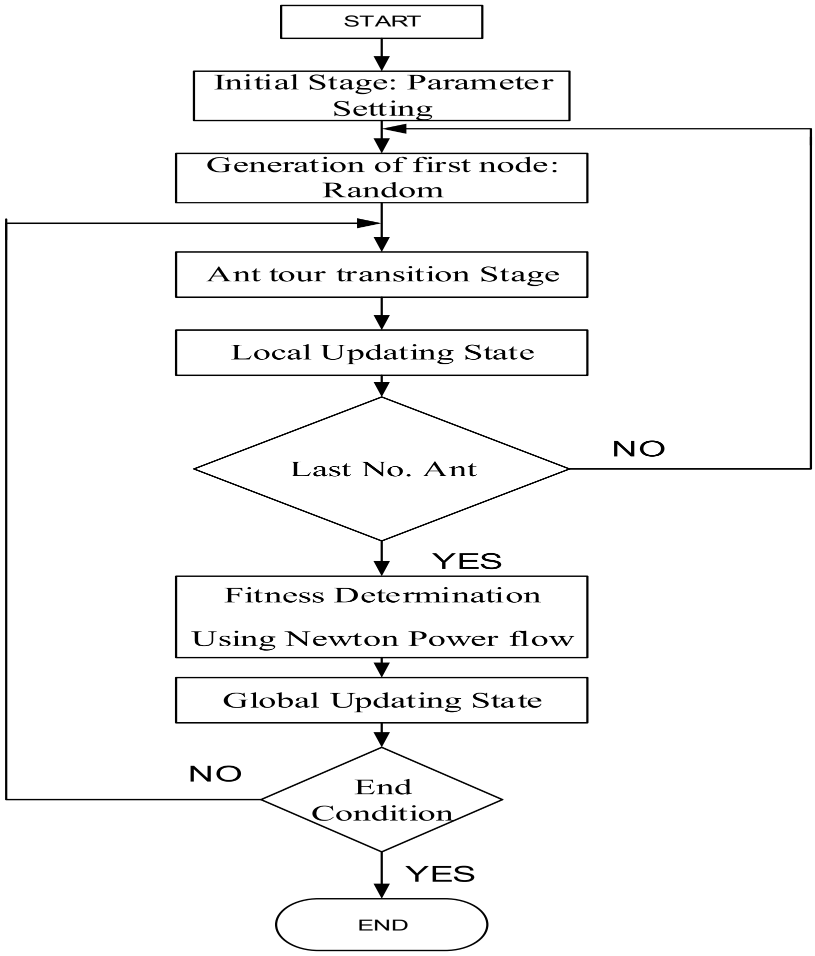

Figure 6: ACO Flowchart

Fitness Determination: This is achieved by running Newton Raphson power flow (NR) for all ants and objective function calculation is carried out. Global Updating State: The best ant tour is figured out from this which gives the best fitness among all the ants.

End Condition: The algorithm terminates when the conditions are satisfied and the process achieves convergence.

3.0 RESULTS AND DISCUSSIONS

3.1 Results

Table 1 shows the Voltage profile, active and reactive bus power loss analysis with capacitor and SVC placement. While figures 7 and 8 depict the results presented in Table 1 graphically.

When the SVC is placed, the amount of active and reactive power flows at bus 6 and bus 7 are as depicted

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in Figures 9, 10, 11 and 12 respectively. With reference to bus 6 in Table 1, active power loss with SVC is seen to be 0.03MW which is less than the value obtained when capacitors are placed which was found to be 0.06MW.

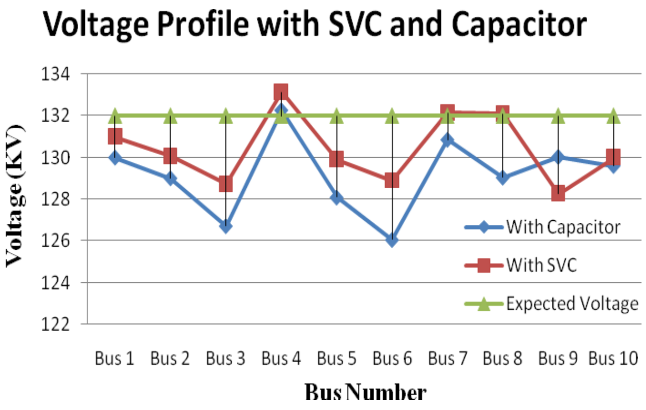

Figure 7: Voltage profile of the 132kV shiroro network modelled as 10 buses network

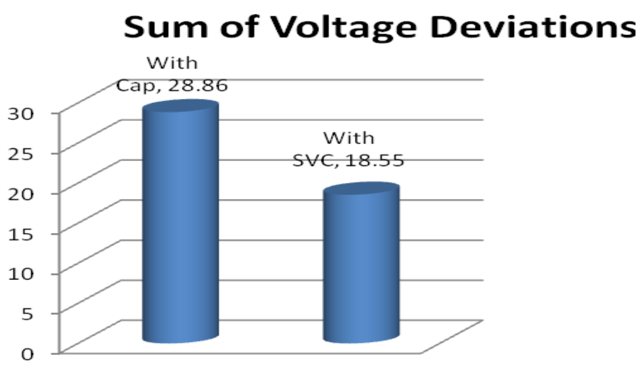

Figure 8: Sums of Voltage Deviations of the 132kV shiroro network modelled as 10 buses

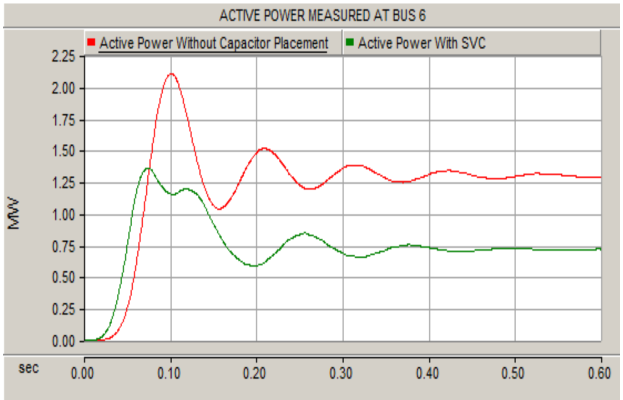

Figure 9: Active Power at bus 6

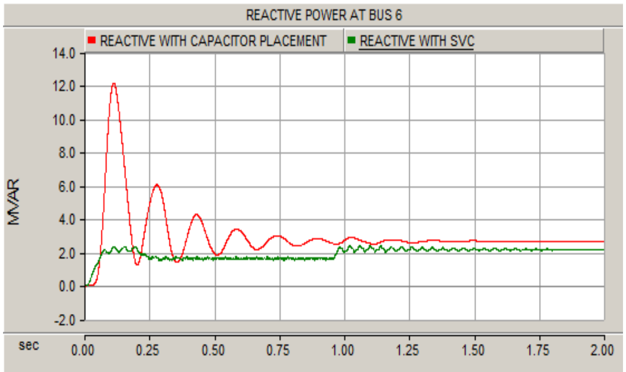

Figure 10: Reactive Power at bus 6

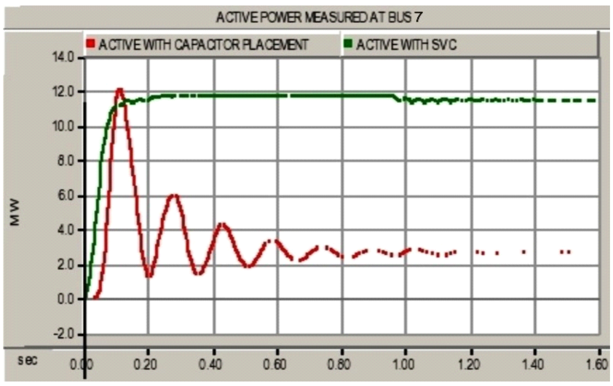

Figure 11: Active Power at bus 7

Likewise the reactive power loss with SVC is found to be -3.54MVAR as compared to the -2.89MVAR recorded when capacitors are placed on the network. Now, initiating a single line-ground fault at a start time of 0.2s and cleared at 0.95s,. The acitive power, reactive power and voltages were pbtained for buses 6, 7 and 9 as shown in Figures 13, 14, 15, 16 and 17.

Table 1: Voltage Profile, Active and Reactive power loss analysis

Bus No	Bus Voltage With Cap. Placement (kV)	Bus Voltage With SVC (kV)	Expected Bus Voltage (kV)	Active Power Loss with Cap. Placement (MW)	Active Power Loss with SVC (MW)	Reactive Power Loss with Cap. Placement(MVAR)	Reactive Power Loss with SVC (MVAR)
Bus 1	130.00	130.99	132.00	1.51	0.20	-2.53	-7.21
Bus 2	129.01	130.06	132.00	1.16	0.31	-1.76	-5.74
Bus 3	126.72	128.72	132.00	0.45	0.25	-4.14	-4.67
Bus 4	132.26	133.14	132.00	0.54	0.31	-3.67	-4.75
Bus 5	128.09	129.90	132.00	1.23	0.10	0.14	0.02
Bus 6	126.06	128.89	132.00	0.06	0.03	-2.89	-3.54
Bus 7	130.85	132.13	132.00	0.04	0.02	-5.19	-5.36
Bus 8	129.04	132.09	132.00	0.12	0.90	-7.12	-6.88
Bus 9	130.03	128.25	132.00	1.82	1.22	-3.53	-7.68
Bus 10	129.60	130.00	132.00	1.50	0.25	-1.75	-5.02
Total				**8.43**	**3.59**	**-32.44**	**-46.08**

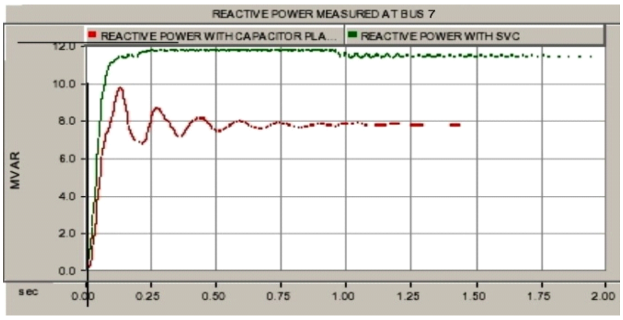

Figure 12: Reactive Power at bus 7

Figure 13: Active Power at bus 9

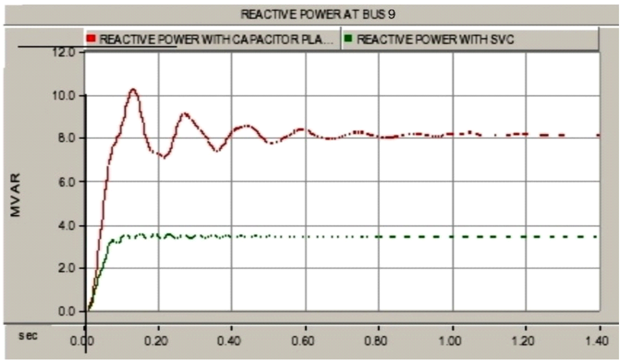

Figure 14: Reactive Power at bus 9

3.2 Discussions of Results

As depicted in figures 7 and 8, it is clear that the use of SVC greatly improves the voltage profile of the transmission grid system with an average of 131kV as against the 129 kV when compared to the use of Capacitor placement.

As depicted in Figure 9, 10, 11 and 12 respectively, the amount of active and reactive power flows at bus 6 and bus 7 experience a smoothening in wave form when compared with capacitor placement, with referenced to bus 6, the system experiences a not quite damped wave form within the interval where the fault occur indicating an active effect when SVC is optimally placed. The bus voltages are confirmed to be quite low as compared with the expected voltage magnitude (Figure 15). Initiating a single line-ground fault at a start time of 0.2s and cleared at 0.95s, with referenced to Bus 6, the system experiences a heavy distorted wave form within the interval where the fault occurs indicating a less active effect when capacitor is placed at various buses. These were repeated for Buses 7 and 9 as shown in Figure 16 and Figure 17 respectively.

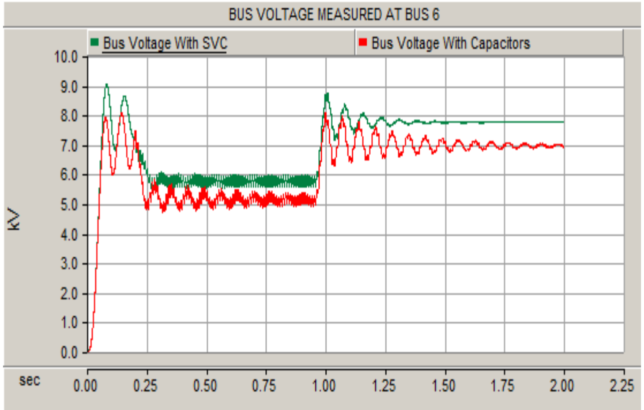

Figure 15: Bus Voltage at bus 6 during faults

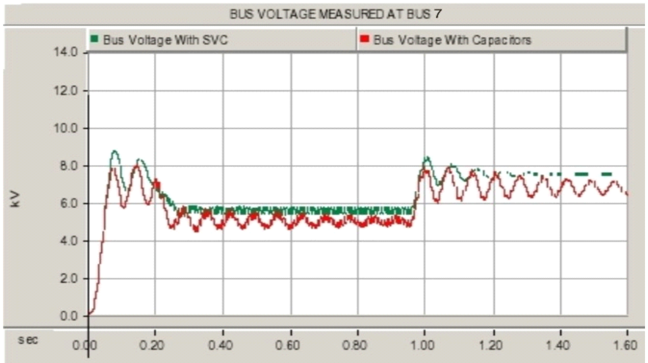

Figure 16: Bus Voltage at bus 7 during faults

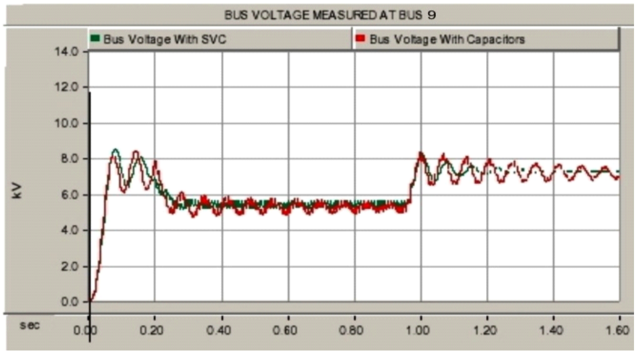

Figure 17: Bus Voltage at bus 9 during faults

The effects of SVC on the Shiroro 132kV Transmission network considered with the system subjected to fault condition. It can be seen that SVC is able to minimize losses in addition to mitigation of voltage collapse.

Initiating a phase-ground fault on the network at start time of 0.2 sec and cleared of 0.95 sec, with reference to Bus 6, when SVC is not connected on the network, the system experiences a swing in the magnitude of the current flow on the line which puts the system into an unbalanced state as depicted in Figure 18.

However, a single phase-ground fault initiated with SVC connected, the magnitude of the fault current flow is greatly minimized as shown in Figure 18. This demonstrates clearly the effects of SVC on the network especially during contingencies in the network at the same intervals. This process is repeated for buses 7 and 9 as shown in Figures 19 and 20.

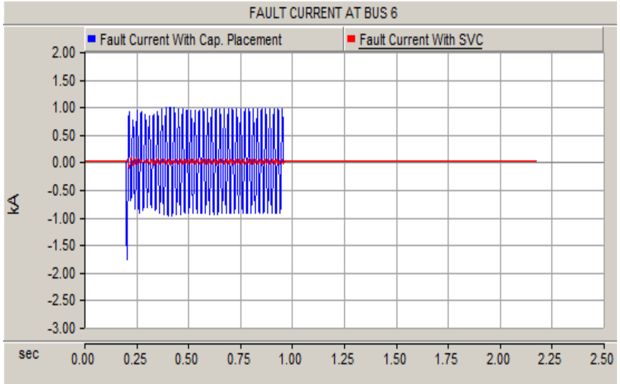

Figure 18: Fault Current at Bus 6

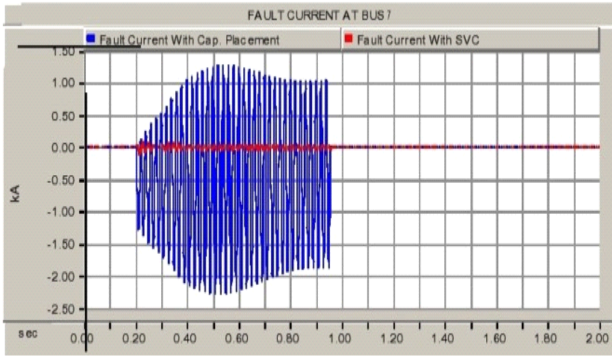

Figure 19: Fault Current at Bus 7

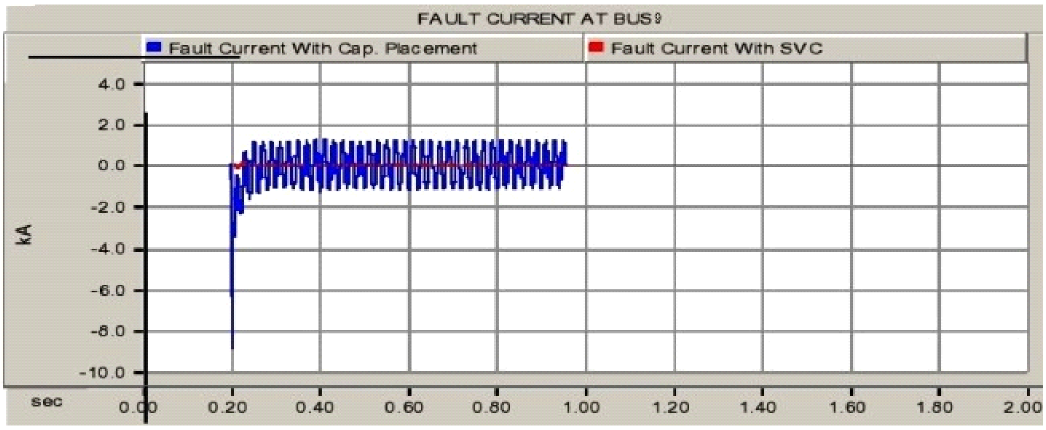

Figure 20: Fault Current at Bus 9

4. CONCLUSION

The basic structures of SVC operating under different voltage control and its bus model have been successfully applied on the case study. Simulations carried out confirmed that the SVC is capable of minimizing power loss, improve the voltage profile of the network as well as ensure system stability during fault condition on the 132 kV Shiroro transmission network when compared with capacitor placement. The use of the Ant Colony Optimization techniques for optimal placement of the SVC was successfully implemented. The PSCAD/EMTDC simulator for loss reduction analysis confirmed the results with the earlier works and presents the following achievements:

a) With the introduction of SVC, the magnitude of the voltage at various load buses sufficiently meet the permissible limit of 0.9 p.u. $\leq$ V $\leq$ 1 p.u. as stated in the objective function; and

b) The voltage profile of the system considered was observed to have averagely improved from 129 kV to 131 kV.

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