CHEAPER MEANS OF CONSTRUCTING TRAFFIC LIGHT: THE COUNTER-GATE ALTERNATIVE

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Abstract
There is a growing desire for electronic gadgets to be more affordable. However, this cannot be, except the cost of production is cut down considerably. This paper looks particularly, at one cost-effective method of producing traffic light compared to the microcontroller-dependent method which is rather relatively capital intensive. The intention is to cut down the cost of producing traffic light. The design procedure employed here makes use of the 555 timer IC configured to generate pulse signal; flip flop ICs arranged to realize a hexadecimal counter to count the pulses; and some logic gate ICs used to determine which binary pattern that would be allowed to get to the output. The result is a low-cost traffic light with satisfactory efficiency, stability and durability. The paper finally encourages engineers to be economical in their design and construction of gadgets as economics is a vital aspect of industrial activities.

Keywords: 555 timer; Counter; Decoder; Traffic; Light

INTRODUCTION

The counter-gate option of realizing traffic light has proven to be effective both technically and cost-wise. It is cheaper as a result of the components it employs. These components are just commonly available in the local markets around and they include resistors, capacitors, 555 timer IC, 7476 flip-flop IC, simple gates ICs (such as 7408 and 7432), relays, transistors and other simple components of that order. It is solid state throughout, as it does not employ any programmable or software-dependent device such as the microcontroller.

The traffic light can equally be realized using the microcontroller and other auxiliary components. However, the microcontroller for one is a very expensive device. Apart from the cost of purchasing it, more expensive is its programming. The cost of programming one microcontroller can take care of building the counter-gate traffic light completely.

According to Ihemadu (2008), this particular counter-gate traffic light comprises five stages namely,

- Power supply stage
- Pulse generator stage
- Counter stage
- Decoder stage
- Lighting stage

The power supply stage employs d.c. voltage regulators to stabilize the voltage at certain values that are necessary for different parts of the circuit. The pulse generator stage uses the 555 timer IC in the astablemulti vibrator mode to generator a clock signal. The counter circuit uses 7476 J-K flip-flop IC arranged as modulo-16 counter. This circuit counts the

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pulses generated by the pulse generator circuit. The decoder stage employs OR gates, and AND gates to decide which of the three lights (green, yellow or red) would come on. The lighting stage uses relays and power transistors to switch ON or OFF any of the lights in turn. This is the final output of the entire circuit.

DESIGN PROCEDURE

The circuit was actually designed in parts. However, basic design issues were put into serious consideration so as to ensure consistency. Such issues include voltage requirement, current requirement, signal frequency, etc. The subsequent subsections show the design procedures of the various parts of the traffic light circuit.

The Power Supply Stage

The power supply stage of this gadget is a stabilized d.c. power supply circuit employing voltage regulator ICs and supplying two different output voltages: +12V and +5V. The 12V powers the pulse generator and the lighting circuits while the 5V powers the counter and decoder circuits. Singh (2011) has it that the 555 chip can be powered by 4.5V to 18V. Again, the lighting circuit employs 12-V relays and TIP 41 power transistors which require 12V. This informed the choice of 12V d.c. for the pulse generator and lighting circuits. The flip-flop and gate ICs are TTL devices and so use nominal voltage of 5V (NTE Data Book, 2014). This is why the counter and decoder circuits are powered by 5V. The various units of the power supply stage are shown below.

Transformer Unit: The transformer chosen was a 220V/12V, 1000mA, 50Hz transformer.

Rectifier Unit: Four 1N4001 diodes were used to arrange a bridge rectifier. The 1N4001 diode is a silicon diode and so each of them has an inherent voltage drop of 0.7V (Tooley, 2006). During each half cycle of the a.c. voltage, two alternate diodes conduct and this leads to a total voltage drop of 0.7V + 0.7V = 1.4V.The output d.c. voltage from the rectifier unit is $V_{dc} = 12V - 1 \cdot 4V = 10 \cdot 6V$

Filter unit: The type of filter used is the shunt input capacitor (electrolytic capacitor); and the preferred chosen value is 35V (that is, 1000μF, 35V electrolytic capacitor).

Regulator Unit: This unit uses two voltage regulators to step down the d.c. voltage to 12V and 5V. In deciding which regulator to use, it should be recalled that part numbers of the 7800 series are for positive voltage while those of 7900 series are for negative voltage. The fact that positive voltage was needed, informed the choice of 7800 series. Furthermore, the last two digits are the value of the voltage it stabilizes to; hence 7812 stabilizes to $+12V_{dc}$ while 7805 stabilizes to $+5V_{dc}$. The figure below is the circuit diagram of the power supply stage.

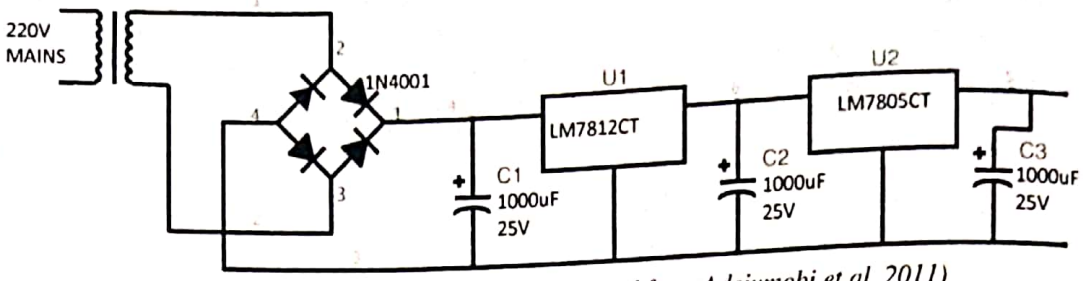


Fig.1. Power supply stage(adapted from Adejumobi et al, 2011)

The Pulse Generator Stage

The pulse generator circuit was realized using the 555 timer IC configured in the astablemultivibrator mode. According to Katz and Borriello(2004), the 555 chip can be tuned to generate clocks of alternate periods and duty cycles. By virtue of this it is possible to vary the frequency and duty cycle of the pulse. Kleitz (2005) explained that the 555 chip got its name from the three 5KΩ resistors setup as a voltage divider from V_{cc} to ground. He added that it comprises two comparators, an S-R flip-flop, a discharge transistor and a buffer. The figure below is a block diagram of the 555 chip in an astablemultivibrator mode.

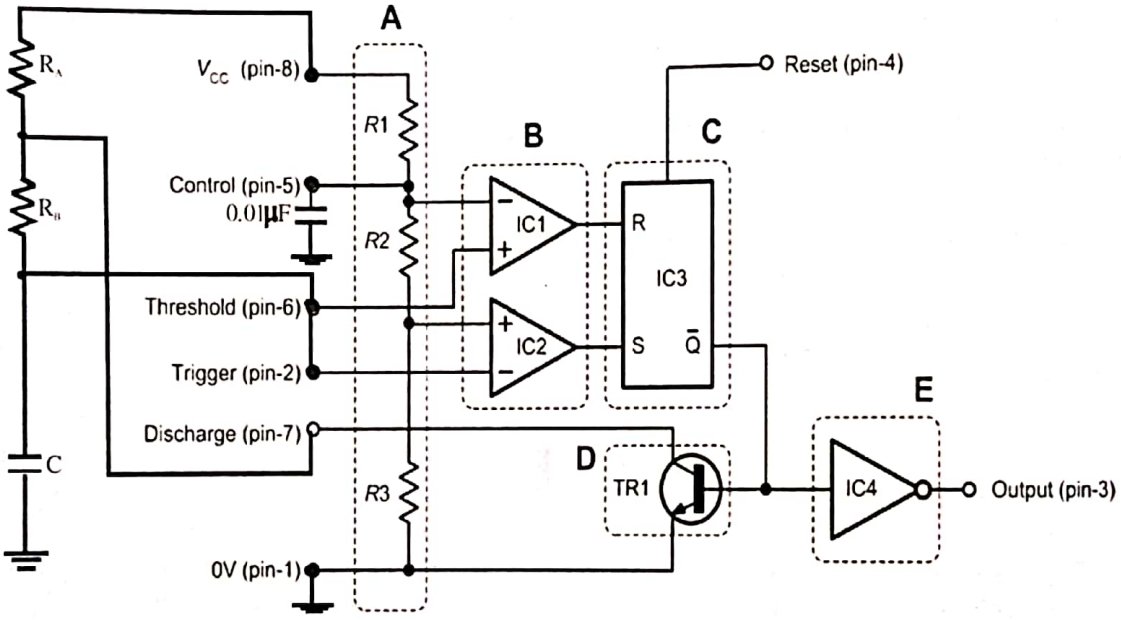


Fig. 2. Block diagram of 555 timer in astablemultivibrator mode (adapted from Kleitz,2005)

The operation of the above circuit is explained as follows:

- When power is first turned ON, the capacitor C is discharged, which places 0V at pin 2, forcing the lower comparator HIGH. This sets the flip-flop ($\bar{Q} = LOW, output = HIGH$).
- With the output HIGH ($\bar{Q}$ LOW), the discharge transistor is open, which allows the capacitor C to charge toward V_{cc} via R_A + R_B.When the capacitor voltage exceeds $\frac{1}{3}V_{cc}$, the lower comparator goes LOW, which has no effect on the S-R flip-flop; but when the capacitor voltage exceeds $\frac{2}{3}V_{cc}$, the upper comparator goes HIGH, resetting the flip-flop, forcing $\bar{Q}$ HIGH and the output LOW.

- With $\bar{Q}$ HIGH, the transistor shorts pin 7 to ground, which discharges the capacitor via R_B.
- When the capacitor voltage drops below $\frac{1}{3}V_{cc}$, the lower comparator goes back HIGH again, setting the flip-flop and making $\bar{Q}$ LOW, output HIGH.
- Now, with $\bar{Q}$ LOW, the transistor opens again, allowing the capacitor to start charging up again.
- The cycle repeats, with the capacitor charging up to $\frac{2}{3}V_{cc}$ and then discharging down to $\frac{1}{3}V_{cc}$ continuously. While the capacitor is discharging, the output is LOW.

Figure 3 below is the actual schematic diagram of the astablemultivibrator while figure 4 is its output signal.

Fig.3. Schematic diagram of the astablemultivibrator (adapted from Ihemadu, 2008)

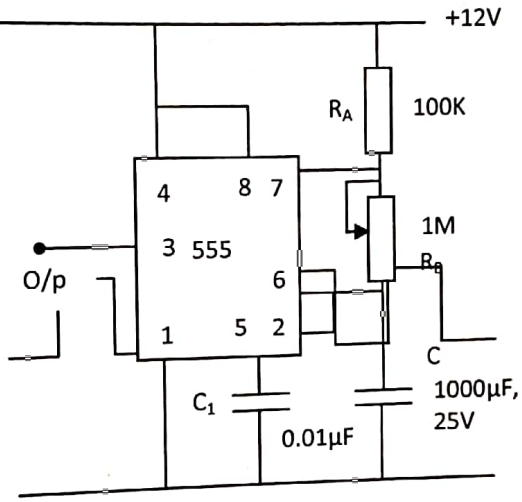


Fig.4. Output signal of the a stablemultivibrator

The Counter Stage

This is an arrangement of a four-stage binary counter based on J-K bistables. Each stage successfully divides the clock input signal by a factor of two; meaning that two cycles of the clock input signal to flip-flop D leads to one cycle of the clock input signal to flip-flop C, and so on (Tooley, 2006). This type of counter is referred to as ripple or asynchronous counter.

Furthermore, the counter circuit was arranged this way with the following facts as guide:

- That the maximum count a single flip-flop can make is 2.
- That when a number of flip-flops are cascaded from the output of one to the clock input of the next, a ripple (asynchronous) counter results whose total count is given by 2^n, where n is the number of flip-flops used to realize the counter.
- That the first flip-flop to be clocked generates the least significant bit (LSB) while the last generates the most significant bit (MSB).
- That there is no need for a NOT gate to realize the inverse of the letters – A, B, C and D which are the outputs of the flip-flops – since their complementary

outputs ($\bar{Q}_A$, $\bar{Q}_B$, $\bar{Q}_C$ *and* $\bar{Q}_D$) perform the task of inversion automatically. Figure 5 below is the circuit diagram of the counter stage.

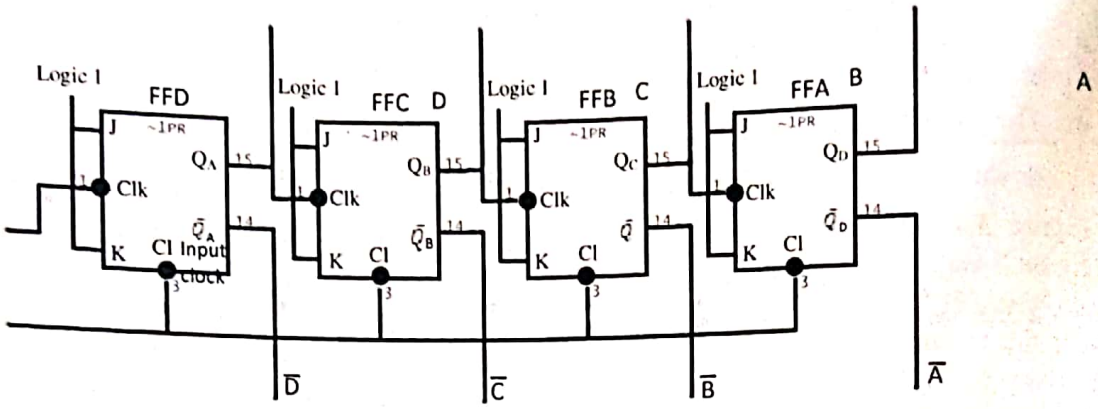


Fig.5. Counter Stage (adapted from Ihemadu,

The clock input of flip-flop D receives the pulse signal from the pulse generator circuit. As a result, flip-flop D output changes state most frequently, of the four flip-flops. Each complete input pulse produces a change in its output state. Therefore two input pulses produce one complete pulse at its output. In the same vein two pulses at the output of flip-flop D (that is, clock input of flip-flop C) produce one complete pulse at the output of flip-flop C (that is, clock input of flip-flop B) and so on. Following this sequence therefore, to produce a change of state at the output of flip-flop A, 8 cycles of the pulse signal must be introduced to the clock input of flip-flop D, and to produce one complete cycle of signal at the output of flip-flop A, 16 cycles of the pulse signal must be introduced to the clock input of flip-flop D. Therefore the counter is a modulo-16 (that is, hexadecimal) counter. This agrees with the formula 2^n, which is 2^4 or 16 counts.

It could be seen that all the clear (cl) terminals are linked together. This is to facilitate synchronous clearing of all the flip-flops and hence, resetting the counter. The circuit that operates the resetting is shown below.

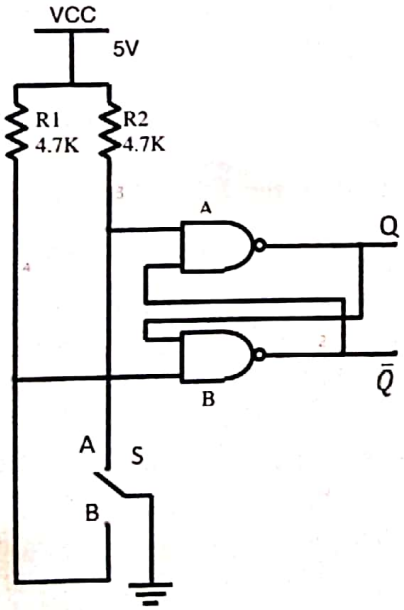


Fig.6. Cross-coupled NAND circuit (adapted from Kleitz, 2005)

The above circuit operates on the basis that the NAND gate produces an output of logic 1 if at least one of its inputs receives logic 0 (see table 1).

Table 1. Truth Table of NAND Gate

A	B	O/P
0	0	1
0	1	1
1	0	1
1	1	0

The circuit is operated with a switch S, which is a 2-way push button. A single push on the button causes the striker to move from point A to point B and then back to point A and relax. Because the striker is tied to ground, wherever it touches means introduction of logic 0. Therefore, a strike on point B means that NAND gate B would receive logic 0 at its only free input through R_1 and produce logic 1 at $\bar{Q}$. At this time, NAND gate A would receive logic 1 at its only free input through R_2 and supply logic 0 at Q. On releasing the button of S, the striker returns to point A thereby introducing logic 0 to gate A to produce logic 1 at Q. This time, gate B receives logic 1 (that is +5V) through R_1 to produce logic 0 at $\bar{Q}$. Therefore a single push of the button of switch S, leads to the production of one complete but momentary clock pulse. This makes it possible for the circuit to act as a clear pulse generator. Output Q is the preferable feeder to the clear (cl) terminals of the flip-flops.

The Decoder Stage

This section of the gadget is responsible for receiving the binary bits released by the counter circuit and deciding which lamps should come ON, with the aid of the bit pattern from the counter at each count. It does the work of a translator, translating bit patterns to take decision on which lamps should be permitted to glow at each point in time. The circuit was realized by first distributing the 16 counts of the hexadecimal counter among the 3 lamps. Meanwhile, it should be recalled that the traffic light is going to be mounted on a junction and there are two arms of roads passing through the junction. Therefore, subscript 1 has been used to denote road 1 while subscript 2 is for road 2 (see table 2).

Table 2. Count Distribution

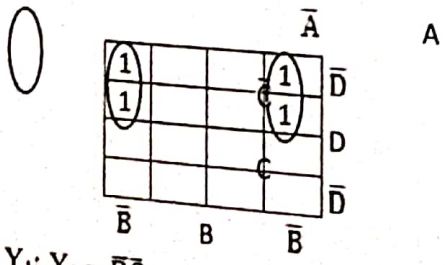
	COUNTER OUTPUT				LAMPS					
HEX	A	B	C	D	Y_1	Y_2	G_1	R_2	G_2	R_1
0	0	0	0	0	1	1	0	0	0	0
1	0	0	0	1	1	1	0	0	0	0
2	0	0	1	0	0	0	1	1	0	0
3	0	0	1	1	0	0	1	1	0	0

4	0	1	0	0	0	0	1	1	0	0
5	0	1	0	1	0	0	1	1	0	0
6	0	1	1	0	0	0	1	1	0	0
7	0	1	1	1	0	0	1	1	0	0
8	1	0	0	0	1	1	0	0	0	0
9	1	0	0	1	1	1	0	0	0	0
10	1	0	1	0	0	0	0	0	1	1
11	1	0	1	1	0	0	0	0	1	1
12	1	1	0	0	0	0	0	0	1	1
13	1	1	0	1	0	0	0	0	1	1
14	1	1	1	0	0	0	0	0	1	1
15	1	1	1	1	0	0	0	0	1	1

In the columns under the LAMPS section of the table above, logic 1 represents ON state of the lamps while logic 0 represents OFF state of the lamps.
Y means yellow light; G, green light and R, red light. Subscript 1 means that the light is serving the vehicles on road 1, while subscript 2 is for road 2.
By the distribution, the two yellow lights are the first to come on while others would stay OFF. The yellow lights would stay ON for counts 0 and 1 and go OFF. Immediately after count 1, the green light for road 1 and the red light for road 2 would come ON and stay for counts 2 to 7 (that is six consecutive counts). During this time, other lights would stay OFF. Immediately after count 7, the two yellow lights would come ON again and stay for counts 8 and 9, to warn the vehicles on road 1 to get ready to stop moving and those on road 2 to get ready to start moving. As usual, other lights would stay OFF for these two counts. Immediately after count 9, the green light for road 2 and the red light for road 1 would come ON and stay for counts 10 to 15 to complete the first cycle of lighting. During this period of counts, other lights remain OFF as well. This is another six counts just as in the case of green light 1 and red light 2. This cycle of lighting can continue indefinitely for as long as there is power supply. The above description is actually a design prospect of how the decoder circuit should work. To actually realize the decoder circuit, there is the need to minimize the logic 1 distributions to the different lights using karnaugh map as can be seen below.

Karnaugh Map Minimization

Y_1 and Y_2 would glow (that is, be on logic 1) when the counter output produces binary patterns 0000, 0001, 1000 and 1001 (that is, representing the variables $\bar{A}\bar{B}\bar{C}\bar{D}$, $\bar{A}\bar{B}\bar{C}D$, $A\bar{B}\bar{C}\bar{D}$ and $A\bar{B}\bar{C}D$ respectively). Below is the K-Map minimization of the binary patterns (or variables) of the counter output.
For Y_1; Y_2

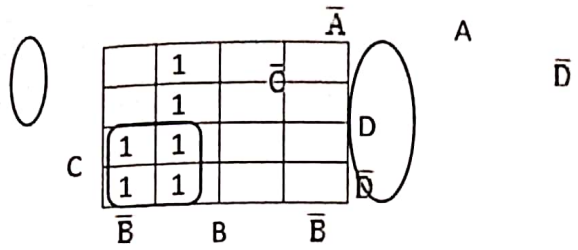


$Y_1; Y_2 = \bar{B}\bar{C}$ ---------- (i)

In the same vein, G_1 and R_2 would glow when the counter output produces binary patterns 0010, 0011, 0100, 0101, 0110 and 0111(that is, representing the variables

$\bar{A}\bar{B}C\bar{D}$, $\bar{A}\bar{B}CD$, $\bar{A}B\bar{C}\bar{D}$, $\bar{A}B\bar{C}D$, $\bar{A}BC\bar{D}$ and $\bar{A}BCD$). Below is the K-Map minimization of the binary patterns.

For G_1; R_2

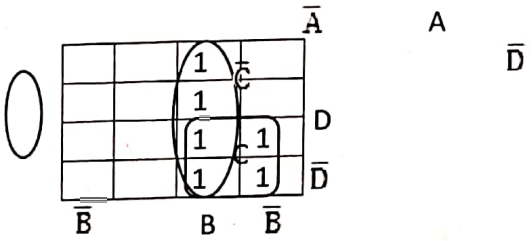


G_1; $R_2 = \bar{A}B + \bar{A}C$

$= \bar{A}(B + C)$---------- (ii)

Finally, G_2 and R_1 would glow when the counter output produces binary patterns 1010, 1011, 1100, 1101, 1110 and 1111(that is, representing the variables $A\bar{B}C\bar{D}$, $A\bar{B}CD$, $AB\bar{C}\bar{D}$, $AB\bar{C}D$, $ABC\bar{D}$ and $ABCD$). Below is the K-Map minimizations of the binary patterns.

For G_2; R_1



G_2; $R_1 = AB + AC$

$= A(B + C)$---------- (iii)

The Boolean expressions for the three different pairs of lights are then implemented as shown below.

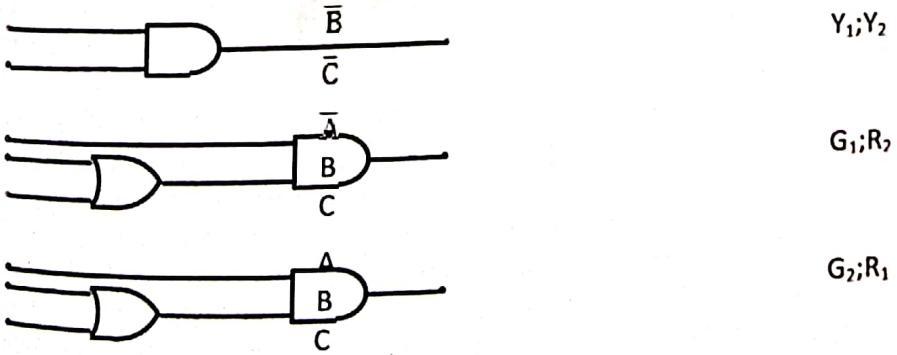


Fig.7. Decoder stage

Once again, during counts 0 and 1, $Y_1$and Y_2 would glow, while others would stay OFF; during counts 2 to 7, G_1 and R_2 would glow while others would stay OFF; during counts 8 and 9 Y_1 and Y_2 would glow again while others would stay OFF and

during counts 10 to 15 G_2 and R_1 would glow while others would stay OFF and the process keeps repeating itself.

The Lighting Circuit Stage

Meanwhile, the current supplied from the outputs of the above logic gates is d.c. and moreover, too small to light a filament bulb. It can only light a light-emitting diode (LED). Therefore, to make it light a 60-W bulb for instance, a modification is imperative using power transistors and relays as shown below

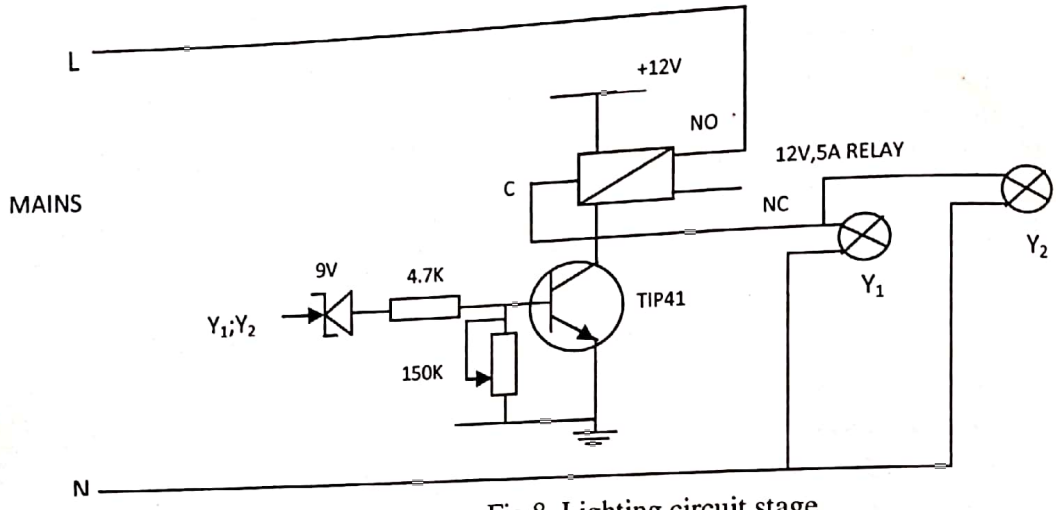


Fig.8. Lighting circuit stage

The idea behind this modification is to allow the supply of power from the mains to the 60-W bulbs. The live wire of the mains supply is connected to the normally open (NO) terminal of the relay while the common (C) terminal is connected to one of the terminals of the lamp (Rashid, 2010). The other terminal of the lamp is then connected to the neutral wire of the mains. Figure 8 shows the circuit for lighting yellow lights only. The same circuit is repeated for the other two pairs of lights, to make for a total of three of such a circuit. On the whole, there would be three 60-W bulbs on each arm of the cross roads thereby giving rise to a total of twelve 60-W bulbs.

Take the yellow lights for instance. When the AND gate for $Y_1;Y_2$ supplies an output, the current passes through the 9-V zener diode and 4.7K resistor to avoid surge into the base junction of the TIP41 power transistor. If there is still the need to further reduce the surge, the 150K preset resistor could be varied to reduce the resistance on that arm thereby allowing some more current to drain through the arm. The remaining current then reaches the transistor and triggers it into conduction. As a result, the currentfrom V_{cc}, which formerly could not flow through the relay, now begins to flow. It passes through the collector-emitter junction of the transistor and returns to ground. By this conduction, the relay is activated so that the normally open contact would then close. Current from the mains supply then flows through it to the common terminal, on to the 60-W bulb and back to the neutral. When once the $Y_1;Y_2$ gate stops supplying current to the base of the TIP41 transistor, the transistor is switched off; the relay is deactivated thereby disconnecting the normally open contact from the common terminal and the yellow light goes off.This process also holds exactly, for the other two pairs of lights in this unit.

CONCLUSION

The counter-gate method of realizing a traffic light is a workable and yet cheap method of achieving the circuit. According to appendix I, the total cost is about ₦12,000. When compared with the microcontroller method (for instance), it is much cheaper because programming the chip alone costs between ₦5,000 and ₦10,000 depending on the programmer. Adding the costs of other auxiliary components and materials would definitely shoot the total cost far above N30,000 at least.

Since economics is an important part of engineering production, this paper advises engineering practitioners to consider options like the counter-gate alternative of realizing traffic light more especially when the cash is not very much there. Engineering production always has cheap options and they should always be explored and subsequently put into consideration during design to ensure that workable gadgets are produced at minimum cost possible.

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Appendix I. Bill of Engineering Measurement and Evaluation

S/N	Description of Component	Quantity	Unit Cost(₦)	Total Cost(₦)
1	12-V Transformer	1	100	100
2	1N4001 diode	4	10	40
3	1000μF, 25V capacitor	4	50	200
4	LM7812CT voltage regulator	1	50	50
5	LM7805CT voltage regulator	1	50	50
6	NE555N timer IC	1	50	50
7	100K resistor	1	10	10
8	1M preset resistor	1	30	30
9	0.01μF capacitor	1	15	15
10	SN7476N J-K flip flop	2	300	600
11	4.7K resistor	5	10	50
12	SN7400N NAND gate	1	150	150
13	Soft button switch	1	50	50
14	SN7408N AND gate	1	150	150
15	SN7432N OR gate	1	150	150
16	9V zener diode	3	20	60
17	150K preset resistor	3	30	90
18	TIP41 transistor	3	150	450
19	12V relay	3	250	750
20	60W electric bulb	12	50	600
21	Connecting wire	-	500	500
22	$1.5mm^2$ cable	-	1200	1200
23	Soldering lead	-	400	400
24	Vero board	-	500	500
25	Printed Circuit Board	-	500	500
26	Casing	-	2000	2000
27	Labour	-	1200	1200
28	Transport	-	2000	2000
	Total			**11,945**

The total cost for the construction of the traffic light was eleven thousand nine hundred and fourty five naira (₦11,945.00) only. This was the cost of the work as at August 2013.